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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	14	V
V_{id}	Differential input voltage(2)	±2	V
V_i	Input voltage(3)	±6	V
T_{oper}	Operating free air temperature range	-40 to +85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thjc}	Thermal resistance junction to case(4) SOT23-5 SO8 TSSOP8 TSSOP14	 80 28 37 32	°C/W
R_{thja}	Thermal resistance junction to ambient area SOT23-5 SO8 TSSOP8 TSSOP14	 250 157 130 110	°C/W
ESD	HBM: human body model(5) MM: machine model(6) CDM: charged device model(7)	2 0.2 1	kV

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non inverting input terminal with respect to the inverting terminal.
3. The magnitude of input and output must never exceed V_{CC} +0.3 V.
4. Short-circuits can cause excessive heating.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	4.5 to 12	V
V_{IC}	Common mode input voltage range	V_{CC}^- to $(V_{CC}^+ -1.1)$	V
Standby (pin 8)	Threshold on pin 8 for TSH81	(V_{CC}^-) to (V_{CC}^+)	V

2 Electrical characteristics

Table 3. $V_{CC}^+ = +5$ V, $V_{CC}^- =$ GND, $V_{ic} = 2.5$ V, $T_{amb} = 25$ °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\lvert V_{io} \rvert$	Input offset voltage	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$		1.1	10 12	mV
ΔV_{io}	Input offset voltage drift vs. temperature	$T_{min} < T_{amb} < T_{max}$		3		µV/°C
I_{io}	Input offset current	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$		0.1	3.5 5	µA
I_{ib}	Input bias current	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$		6	15 20	µA
C_{in}	Input capacitance			0.3		pF
I_{CC}	Supply current per operator	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$		8.2	10.5 11.5	mA
CMR	Common mode rejection ratio ($\delta V_{ic}/\delta V_{io}$)	$+0.1 < V_{ic} < 3.9$ V and $V_{out} = 2.5$ V $T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	72 70	97		dB
SVR	Supply voltage rejection ratio ($\delta V_{CC}/\delta V_{io}$)	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	68 65	75		dB
PSR	Power supply rejection ratio ($\delta V_{CC}/\delta V_{out}$)	Positive and negative rail		75		dB
A_{vd}	Large signal voltage gain	$R_L = 150\ \Omega$ connected to 1.5 V and $V_{out} = 1$ V to 4 V $T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	75 70	84		dB
I_o	|Source|	$V_{id} = +1$, V_{out} connected to 1.5 V $T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	35 28	55		mA
	Sink	$V_{id} = -1$, V_{out} connected to 1.5 V $T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	33 28	55		

Table 3. $V_{CC}^+ = +5$ V, $V_{CC}^- =$ GND, $V_{ic} = 2.5$ V, $T_{amb} = 25$ °C (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{oh}	High level output voltage	$T_{amb} = 25$ °C $R_L = 150\ \Omega$ connected to GND $R_L = 600\ \Omega$ connected to GND $R_L = 2$ kΩ connected to GND $R_L = 10$ kΩ connected to GND $R_L = 150\ \Omega$ connected to 2.5 V $R_L = 600\ \Omega$ connected to 2.5 V $R_L = 2$ kΩ connected to 2.5 V $R_L = 10$ kΩ connected to 2.5 V $T_{min} < T_{amb} < T_{max}$ $R_L = 150\ \Omega$ connected to GND $R_L = 150\ \Omega$ connected to 2.5 V	 4.2 4.60[1] 4.5 4.1 4.4	 4.36 4.85 4.90 4.93 4.66 4.90 4.92 4.93		V
V_{ol}	Low level output voltage	$T_{amb} = 25$ °C $R_L = 150\ \Omega$ connected to GND $R_L = 600\ \Omega$ connected to GND $R_L = 2$ kΩ connected to GND $R_L = 10$ kΩ connected to GND $R_L = 150\ \Omega$ connected to 2.5 V $R_L = 600\ \Omega$ connected to 2.5 V $R_L = 2$ kΩ connected to 2.5 V $R_L = 10$ kΩ connected to 2.5 V $T_{min} < T_{amb} < T_{max}$ $R_L = 150\ \Omega$ connected to GND $R_L = 150\ \Omega$ connected to 2.5 V		 48 54 55 56 220 105 76 61	 150 400 200 450	mV
GBP	Gain bandwidth product	F = 10 MHz $A_{VCL} = +11$ $A_{VCL} = -10$		 65 55		MHz
Bw	Bandwidth at -3 dB	$A_{VCL} = +1$ $R_L = 150\ \Omega$ connected to 2.5 V		87		MHz
SR	Slew rate	$A_{VCL} = +2$ $R_L = 150\ \Omega$ // C_L to 2.5 V $C_L = 5$ pF $C_L = 30$ pF	 60	 104 105		V/µs
ϕm	Phase margin	$R_L = 150\ \Omega$ // 30 pF to 2.5 V		40		° (degree)
en	Equivalent input noise voltage	F = 100 kHz		11		nV/$\sqrt{Hz}$
THD	Total harmonic distortion	$A_{VCL} = +2$, F = 4 MHz $R_L = 150\ \Omega$ // 30 pF to 2.5 V $V_{out} = 1V_{pp}$ $V_{out} = 2V_{pp}$		 -61 -54		dB
IM2	Second order intermodulation product	$A_{VCL} = +2$, $V_{out} = 2\ V_{pp}$ $R_L = 150\ \Omega$ connected to 2.5 V $F_{in1} = 180$ kHz, $F_{in2} = 280$ kHz spurious measurement at 100 kHz		-76		dBc

Table 3. V_{CC}^+ = +5 V, V_{CC}^- = GND, V_{ic} = 2.5 V, T_{amb} = 25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IM3	Third order intermodulation product	A_{VCL} = +2, V_{out} = 2 V_{pp} R_L = 150 Ω to 2.5 V F_{in1} = 180 kHz, F_{in2} = 280 kHz spurious measurement at 400 kHz		-68		dBc
ΔG	Differential gain	A_{VCL} = +2, R_L = 150 Ω to 2.5 V F = 4.5 MHz, V_{out} = 2 V_{pp}		0.5		%
Df	Differential phase	A_{VCL} = +2, R_L = 150 Ω to 2.5 V F = 4.5 MHz, V_{out} = 2 V_{pp}		0.5		° (degree)
Gf	Gain flatness	F = DC to 6 MHz, A_{VCL} = +2		0.2		dB
Vo1/Vo2	Channel separation	F = 1 MHz to 10 MHz		65		dB

1. Tested on the TSH80ILT device only.

Table 4. $V_{CC}^+ = +5$ V, $V_{CC}^- = -5$ V, V_{ic} = GND, $T_{amb} = 25$ °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\|V_{io}\|$	Input offset voltage	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$		0.8	10 12	mV
ΔV_{io}	Input offset voltage drift vs. temperature	$T_{min} < T_{amb} < T_{max}$		2		µV/°C
I_{io}	Input offset current	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$		0.1	3.5 5	µA
I_{ib}	Input bias current	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$		6	15 20	µA
C_{in}	Input capacitance			0.7		pF
I_{CC}	Supply current per operator	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$		9.8	12.3 13.4	mA
CMR	Common mode rejection ratio ($\delta V_{ic}/\delta V_{io}$)	$-4.9 < V_{ic} < 3.9$ V and V_{out} = GND $T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	 81 72	 106		dB
SVR	Supply voltage rejection ratio ($\delta V_{CC}/\delta V_{io}$)	$T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	71 65	77		dB
PSR	Power supply rejection ratio ($\delta V_{CC}/\delta V_{out}$)	Positive and negative rail		75		dB
A_{vd}	Large signal voltage gain	$R_L = 150\ \Omega$ connected to GND $V_{out} = -4$ to $+4$ $T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	 75 70	 86		dB
I_o	|Source|	$V_{id} = +1$, V_{out} connected to 1.5 V $T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	 35 28	 55		mA
	Sink	$V_{id} = -1$, V_{out} connected to 1.5 V $T_{amb} = 25$ °C $T_{min} < T_{amb} < T_{max}$	 30 28	 55		
V_{oh}	High level output voltage	$T_{amb} = 25$ °C $R_L = 150\ \Omega$ connected to GND $R_L = 600\ \Omega$ connected to GND $R_L = 2\ k\Omega$ connected to GND $R_L = 10\ k\Omega$ connected to GND $T_{min} < T_{amb} < T_{max}$ $R_L = 150\ \Omega$ connected to GND	 4.2 4.1	 4.36 4.85 4.9 4.93		V
V_{ol}	Low level output voltage	$T_{amb} = 25$ °C $R_L = 150\ \Omega$ connected to GND $R_L = 600\ \Omega$ connected to GND $R_L = 2\ k\Omega$ connected to GND $R_L = 10\ k\Omega$ connected to GND $T_{min} < T_{amb} < T_{max}$ $R_L = 150\ \Omega$ connected to GND		 -4.63 -4.86 -4.9 -4.93	 -4.4 -4.3	mV

Table 4. $V_{CC}^+ = +5$ V, $V_{CC}^- = -5$ V, V_{ic} = GND, $T_{amb} = 25$ °C (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
GBP	Gain bandwidth product	F = 10 MHz $A_{VCL} = +11$ $A_{VCL} = -10$		65 55		MHz
Bw	Bandwidth at -3 dB	$A_{VCL} = +1$ $R_L = 150\ \Omega$ // 30 pF to GND		100		MHz
SR	Slew rate	$A_{VCL} = +2$ $R_L = 150\ \Omega$ // C_L to GND $C_L = 5$ pF $C_L = 30$ pF	 68	 117 118		V/µs
ϕm	Phase margin	$R_L = 150\ \Omega$ connected to GND		40		° (degree)
en	Equivalent input noise voltage	F = 100 kHz		11		nV/√Hz
THD	Total harmonic distortion	$A_{VCL} = +2$, F = 4 MHz $R_L = 150\ \Omega$ // 30 pF to GND $V_{out} = 1\ V_{pp}$ $V_{out} = 2\ V_{pp}$		 -61 -54		dB
IM2	Second order intermodulation product	$A_{VCL} = +2$, $V_{out} = 2\ V_{pp}$ $R_L = 150\ \Omega$ to GND $F_{in1} = 180$ kHz, $F_{in2} = 280$ kHz spurious measurement at 100 kHz		-76		dBc
IM3	Third order intermodulation product	$A_{VCL} = +2$, $V_{out} = 2\ V_{pp}$ $R_L = 150\ \Omega$ to GND $F_{in1} = 180$ kHz, $F_{in2} = 280$ kHz spurious measurement at 400 kHz		-68		dBc
ΔG	Differential gain	$A_{VCL} = +2$, $R_L = 150\ \Omega$ to GND F = 4.5 MHz, $V_{out} = 2\ V_{pp}$		0.5		%
Df	Differential phase	$A_{VCL} = +2$, $R_L = 150\ \Omega$ to GND F = 4.5 MHz, $V_{out} = 2\ V_{pp}$		0.5		° (degree)
Gf	Gain flatness	F = DC to 6 MHz, $A_{VCL} = +2$		0.2		dB
Vo1/Vo2	Channel separation	F = 1 MHz to 10 MHz		65		dB

Table 5. Standby mode - V_{CC}^+, V_{CC}^-, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{low}	Standby low level		V_{CC}^-		$(V_{CC}^- +0.8)$	V
V_{high}	Standby high level		$(V_{CC}^- +2)$		(V_{CC}^+)	V
$I_{CC-STBY}$	Current consumption per operator when standby is active	Pin 8 (TSH81) to V_{CC}^-		20	55	µA
Z_{out}	Output impedance (R_{out}//C_{out})	R_{out} C_{out}		10 17		MΩ pF
T_{on}	Time from standby mode to active mode			2		µs
T_{off}	Time from active mode to standby mode	Down to $I_{CC-STBY}$ = 10 µA		10		µs

Table 6. TSH81 standby control pin status

TSH81 standby control pin 8 ($\overline{\text{STANDBY}}$)	Operator status
V_{low}	Standby
V_{high}	Active

Figure 1. Closed loop gain and phase vs. frequency (gain = +2, V_{CC} = ±2.5 V)

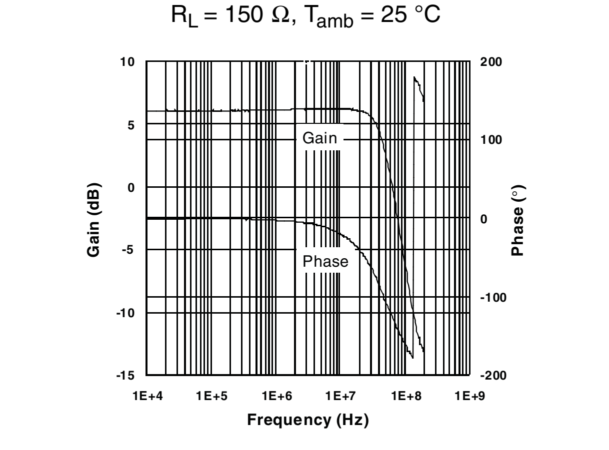


Figure 2. Overshoot vs. output capacitance (V_{CC} = ±2.5 V)

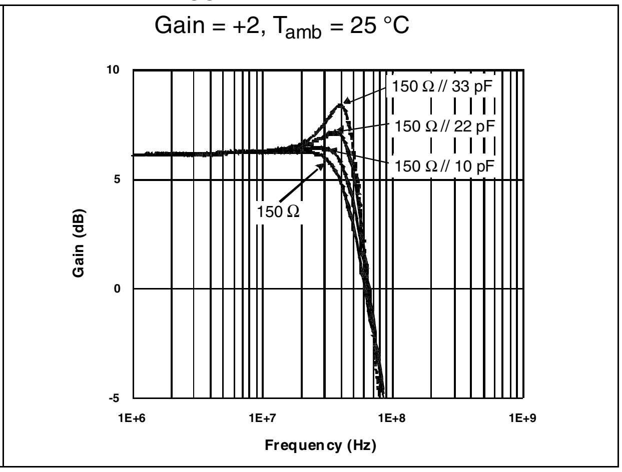


Figure 3. Closed loop gain and phase vs. frequency (gain = -10, V_{CC} = ±2.5 V)

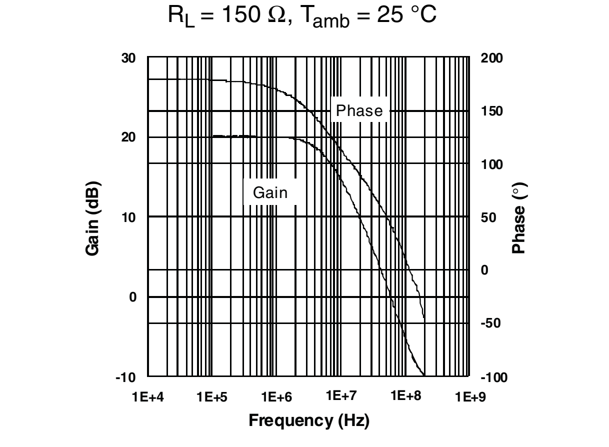


Figure 4. Closed loop gain and phase vs. frequency (gain = +11, V_{CC} = ±2.5 V)

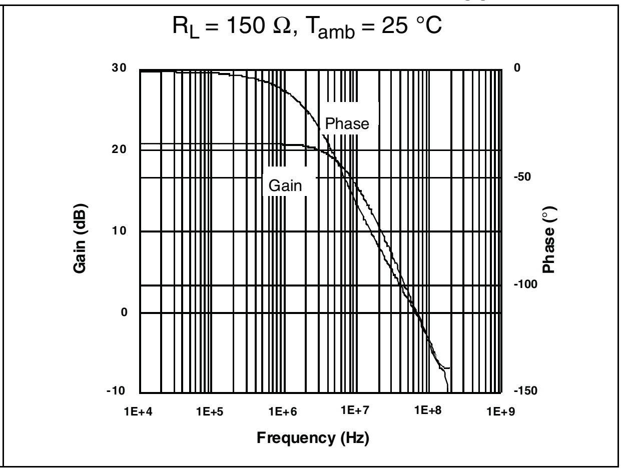


Figure 5. Large signal measurement – positive slew rate (V_{CC} = ±2.5 V)

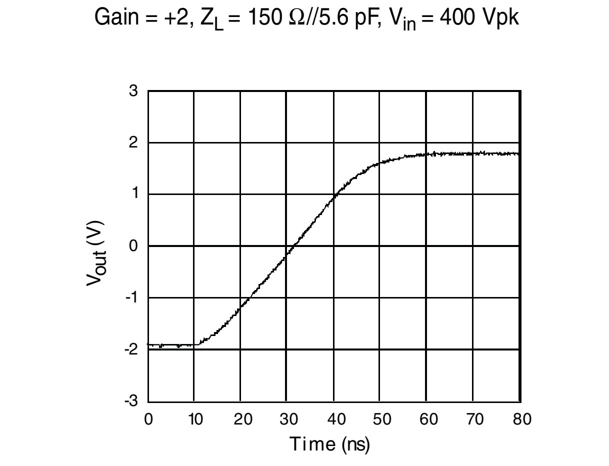


Figure 6. Large signal measurement – negative slew rate (V_{CC} = ±2.5 V)

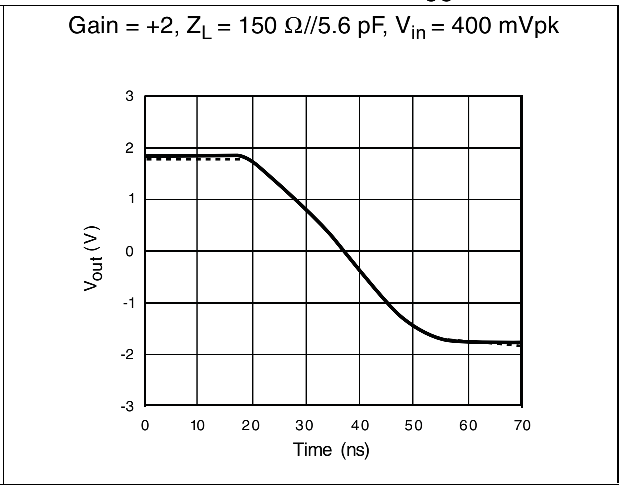


Figure 7. Small signal measurement – rise time (V_{CC} = ±2.5 V)

Gain = +2, R_L = 150 Ω, V_{in} = 400 mVpk

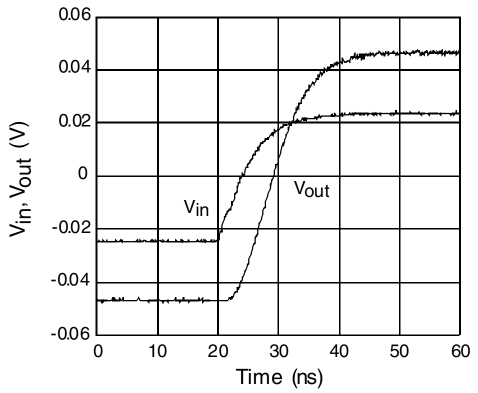


Figure 8. Small signal measurement – fall time (V_{CC} = ±2.5 V)

Gain = +2, R_L = 150 Ω, V_{in} = 400 mVpk

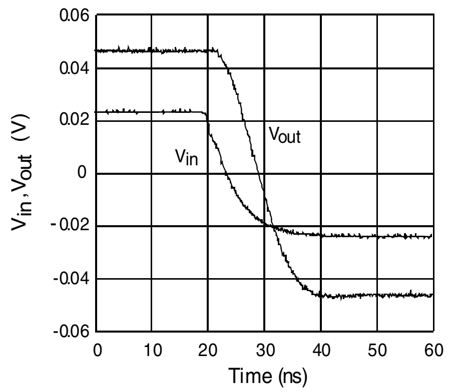


Figure 9. Channel separation (crosstalk) vs. frequency schematic (V_{CC} = ±2.5 V)

Measurement configuration: crosstalk = 20 log (V0/V1)

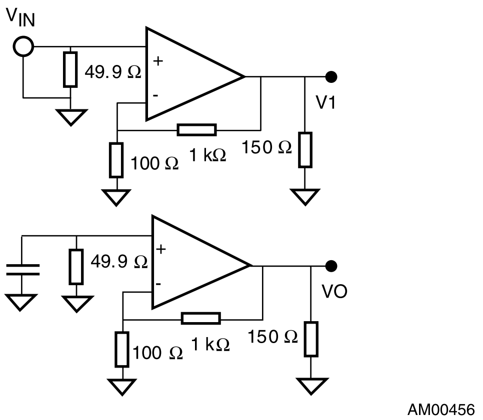


Figure 10. Channel separation (crosstalk) vs. frequency (V_{CC} = ±2.5 V)

Gain = +11, Z_L = 150 Ω//27 pF

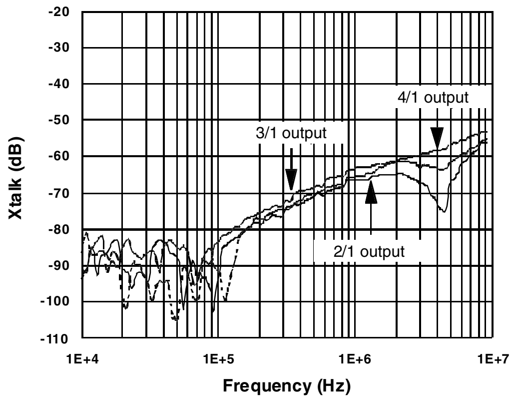


Figure 11. Equivalent input noise voltage (V_{CC} = ±2.5 V)

Gain = +100, no load

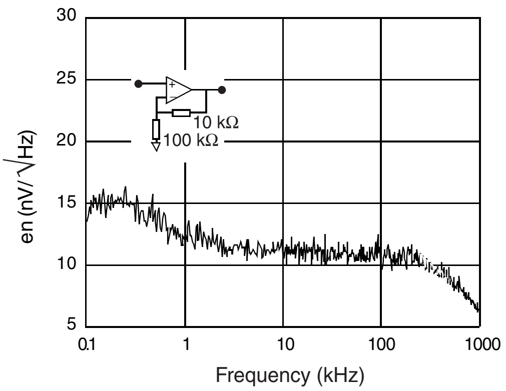


Figure 12. Maximum output swing (V_{CC} = ±2.5 V)

Gain = +11, R_L = 150 Ω

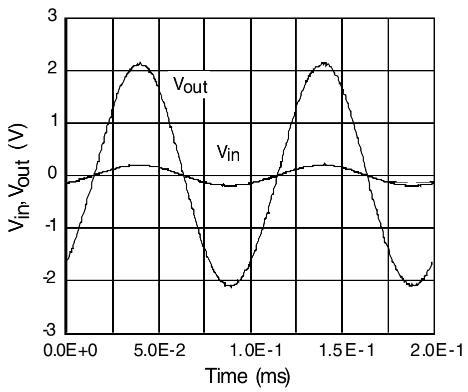


Figure 13. Standby mode - T_{on}, T_{off} (V_{CC} = ±2.5 V)

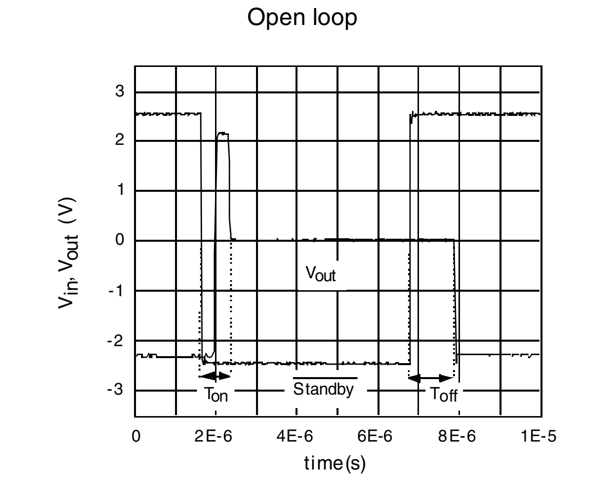
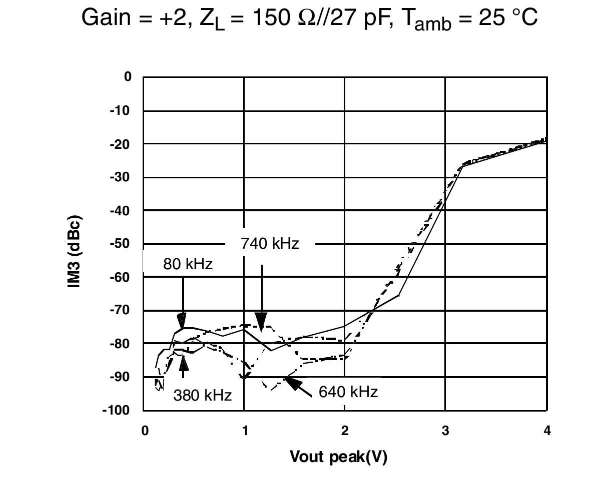


Figure 14. Third order intermodulation (V_{CC} = ±2.5 V)(1)



1. The IFR2026 synthesizer generates a two-tone signal (F1 = 180 kHz, F2 = 280 kHz), each tone having the same amplitude. The HP3585 spectrum analyzer measures the intermodulation products as a function of the output voltage. The generator and the spectrum analyzer are phase locked for better accuracy.

Figure 15. Group delay (V_{CC} = ±2.5 V)

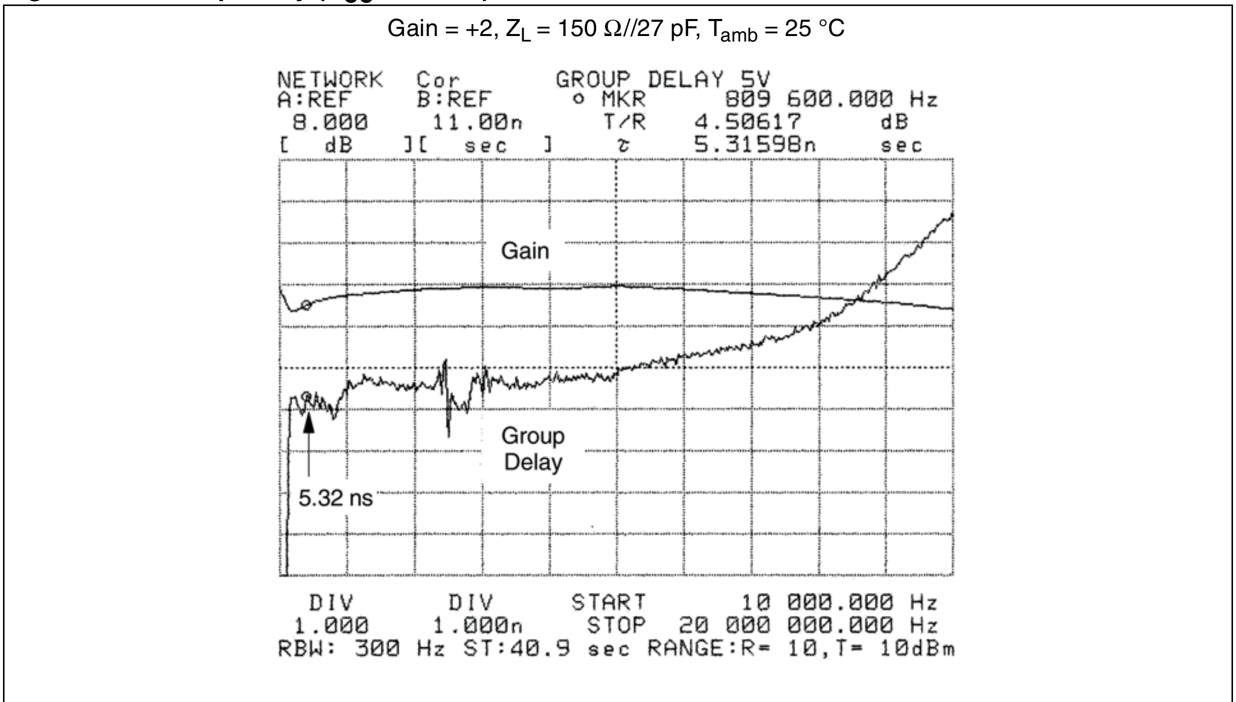


Figure 16. Closed loop gain and phase vs. frequency (gain = +2, V_{CC} = ±5 V)

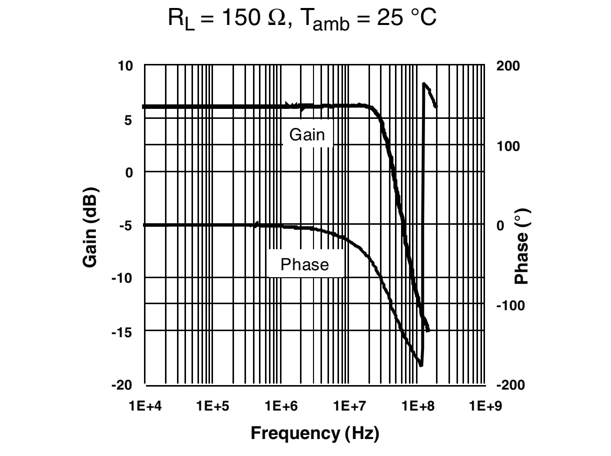


Figure 17. Overshoot vs. output capacitance (V_{CC} = ±5 V)

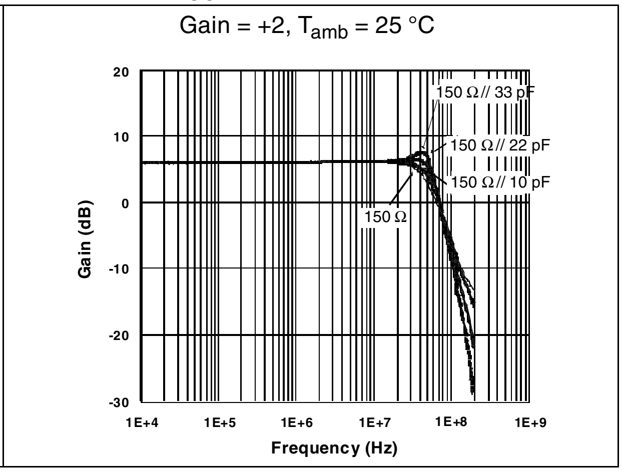


Figure 18. Closed loop gain and phase vs. frequency (gain = -10, V_{CC} = ±5 V)

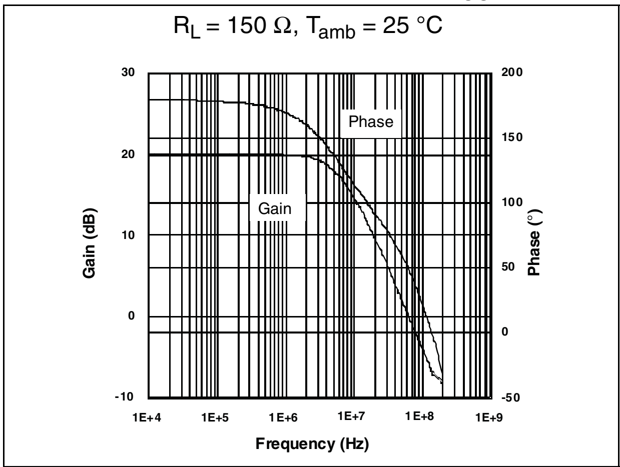


Figure 19. Closed loop gain and phase vs. frequency (gain = +11, V_{CC} = ±5 V)

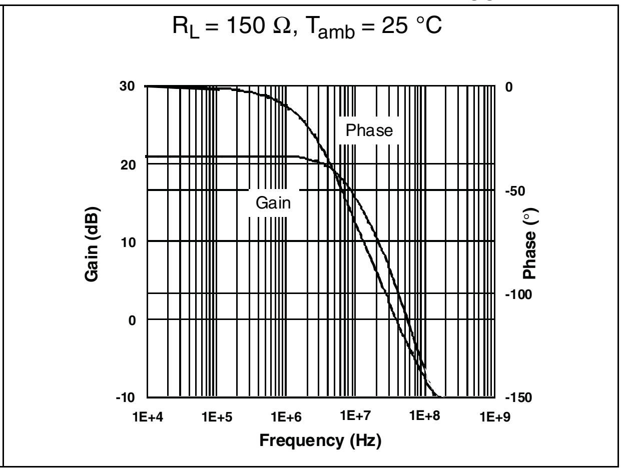


Figure 20. Large signal measurement - positive slew rate (V_{CC} = ±5 V)

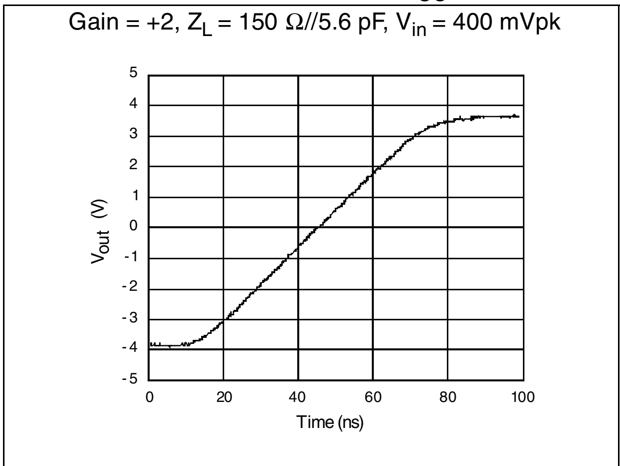


Figure 21. Large signal measurement - negative slew rate (V_{CC} = ±5 V)

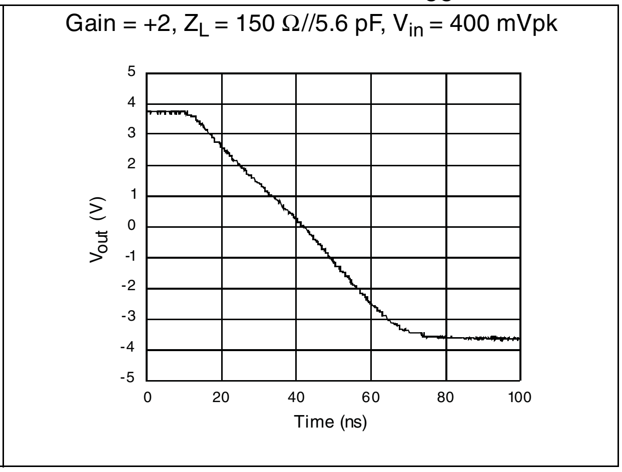


Figure 22. Small signal measurement – rise time (V_{CC} = ±5 V)

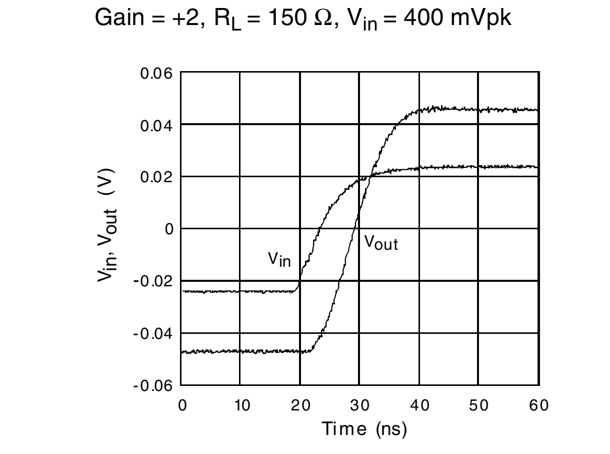


Figure 23. Small signal measurement – fall time (V_{CC} = ±5 V)

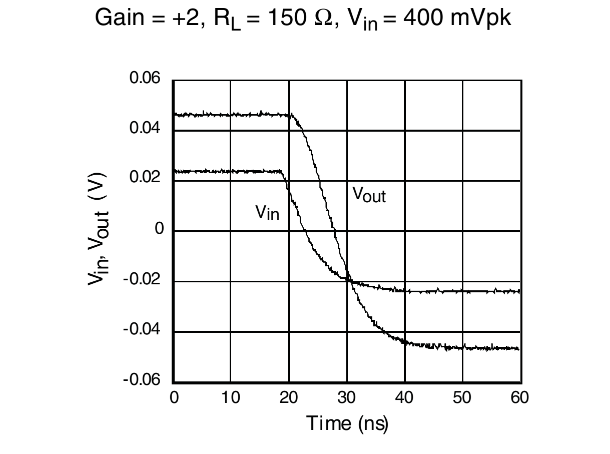


Figure 24. Channel separation (crosstalk) vs. frequency schematic (V_{CC} = ±5 V)

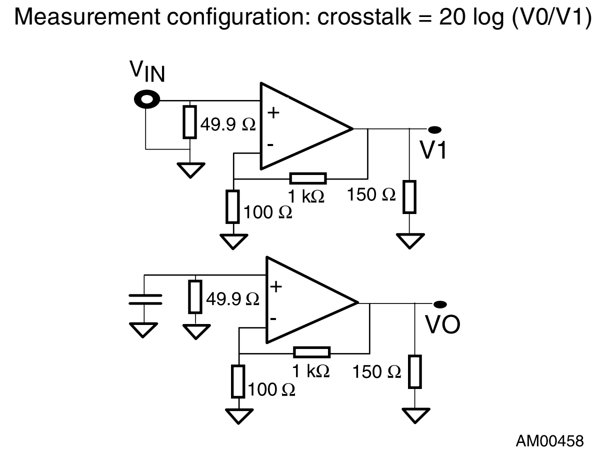


Figure 25. Channel separation (crosstalk) vs. frequency (V_{CC} = ±5 V)

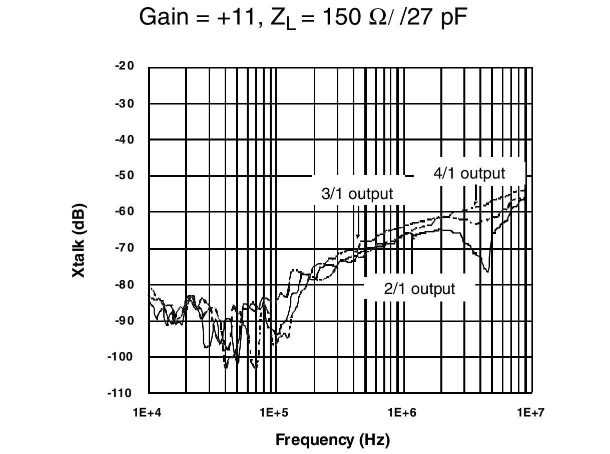


Figure 26. Equivalent input noise voltage (V_{CC} = ±5 V)

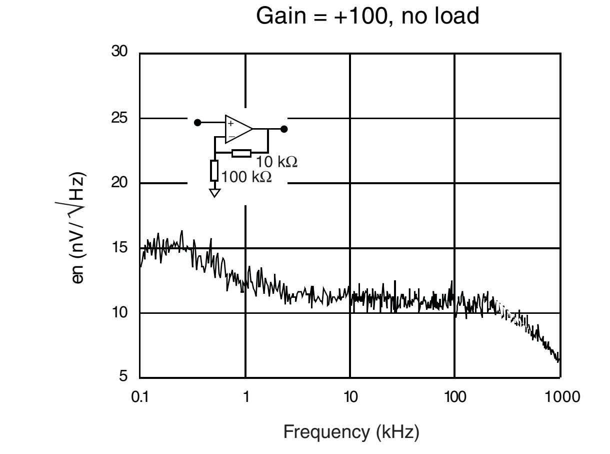


Figure 27. Maximum output swing (V_{CC} = ±5 V)

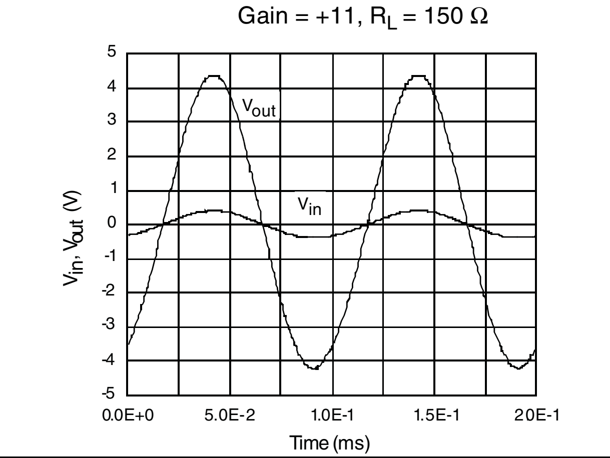


Figure 28. Standby mode - T_{on}, T_{off} (V_{CC} = ±5 V)

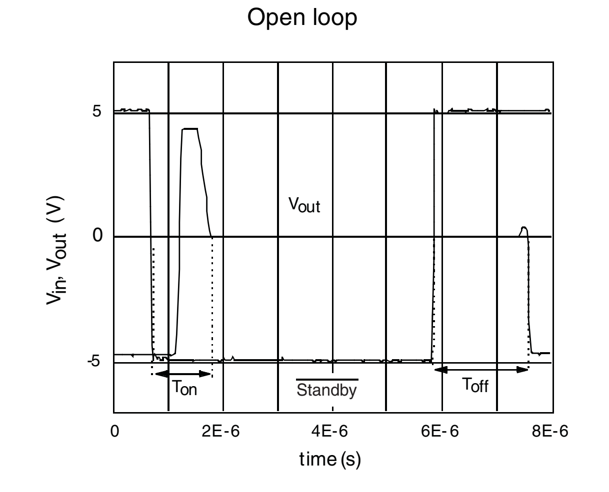
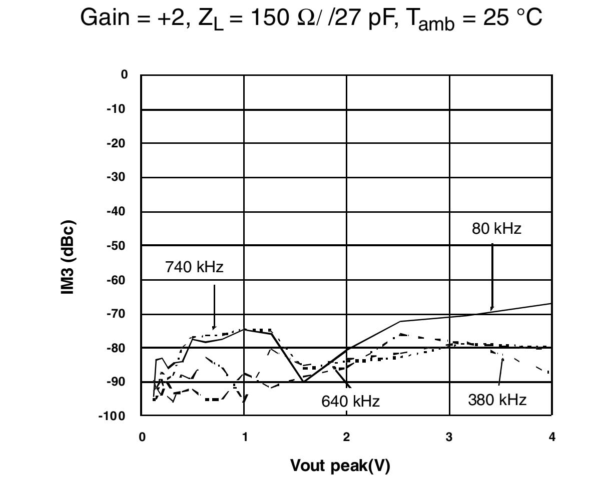
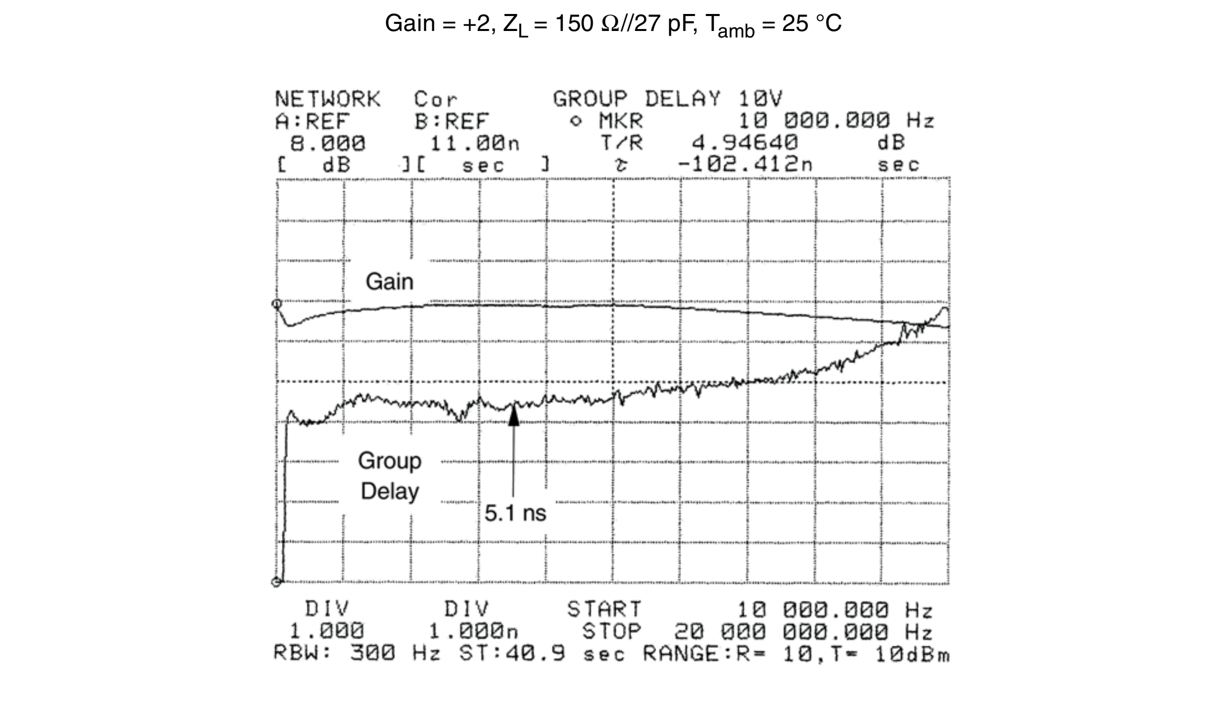


Figure 29. Third order intermodulation (V_{CC} = ±5 V)(1)



1. The IFR2026 synthesizer generates a two-tone signal (F1 = 180 kHz, F2 = 280 kHz), each tone having the same amplitude. The HP3585 spectrum analyzer measures the intermodulation products as a function of the output voltage. The generator and the spectrum analyzer are phase locked for better accuracy.

Figure 30. Group delay V_{CC} = ±5 V



3 Test conditions

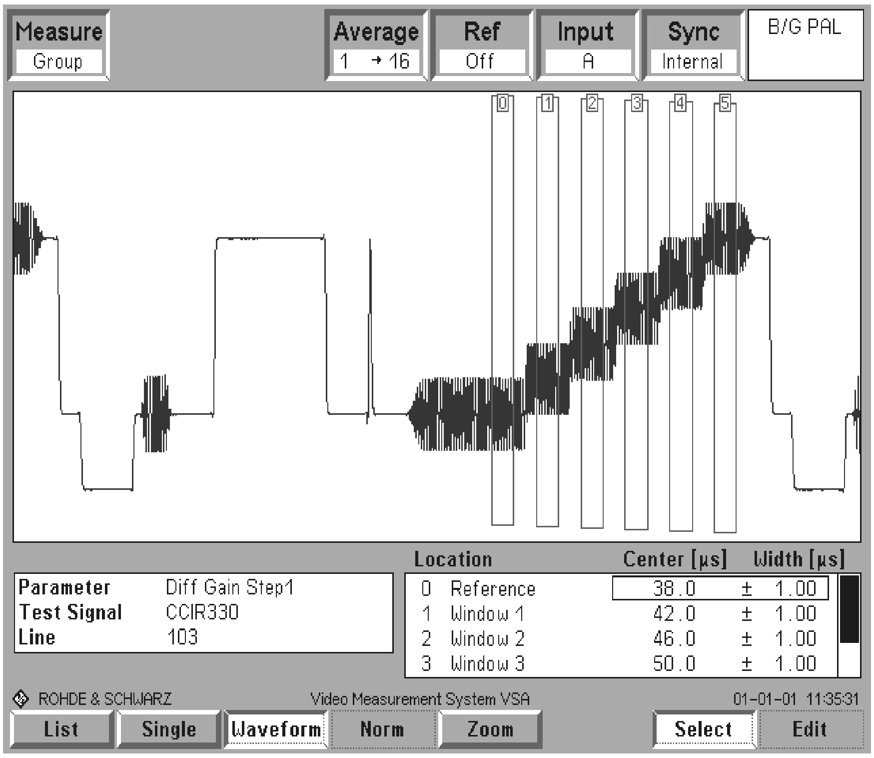
3.1 Layout precautions

To make the best use of the TSH8x circuits at high frequencies, some precautions have to be taken with regard to the power supplies.

- In high-speed circuit applications, the implementation of a proper ground plane on both sides of the PCB is mandatory to ensure low inductance and low resistance common return.
- Power supply bypass capacitors (4.7 µF and ceramic 100 pF) should be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion. The power supply capacitors must be incorporated for both the negative and positive pins.
- All inputs and outputs must be properly terminated with output resistors; thus, the amplifier load is resistive only and the stability of the amplifier will be improved.

  All leads must be wide and as short as possible especially for op-amp inputs and outputs in order to decrease parasitic capacitance and inductance.
- Time constants result from parasitic capacitance. To reduce time constants in lower-gain applications, use a low feedback resistance (under 1 kΩ).
- Choose the smallest possible component sizes (SMD).
- On the output, the load capacitance must be negligible to maintain good stability. You can put a serial resistance as close as possible to the output pin to minimize the effect of the load capacitance.

Figure 31. CCIR330 video line



3.2 Video capabilities

To characterize the differential phase and differential gain a CCIR330 video line is used.

The video line contains five (flat) levels of luminance onto which the chrominance signal is superimposed. The luminance gives various amplitudes which define the saturation of the signal. The chrominance gives various phases which define the color of the signal.

Differential phase (or differential gain) distortion is present if a signal chrominance phase (gain) is affected by the luminance level. The differential phase and gain represent the ability to uniformly process the high frequency information at all luminance levels.

When a differential gain is present, color saturation is not correctly reproduced.

The input generator is the Rohde & Schwarz CCVS. The output measurement is done by the Rohde and Schwarz VSA.

Figure 32. Measurement on Rohde and Schwarz VSA

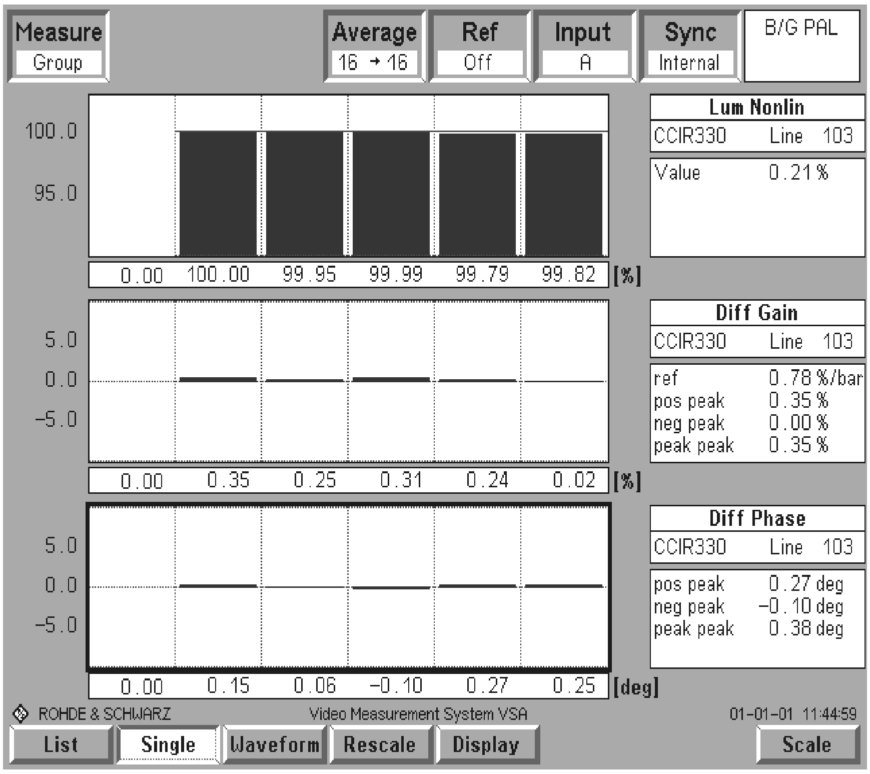


Table 7. Video results

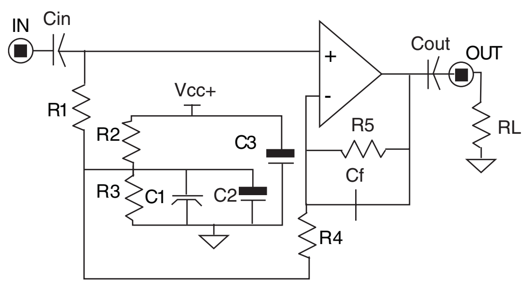
Parameter	Value (V_{CC} = ±2.5 V)	Value (V_{CC} = ±5 V)	Unit
Lum NL	0.1	0.3	%
Lum NL Step1	100	100	%
Lum NL Step2	100	99.9	%
Lum NL Step3	99.9	99.8	%
Lum NL Step4	99.9	99.9	%
Lum NL Step5	99.9	99.7	%
Diff Gain pos	0	0	%
Diff Gain neg	-0.7	-0.6	%
Diff Gain pp	0.7	0.6	%
Diff Gain Step1	-0.5	-0.3	%
Diff Gain Step2	-0.7	-0.6	%
Diff Gain Step3	-0.3	-0.5	%
Diff Gain Step4	-0.1	-0.3	%
Diff Gain Step5	-0.4	-0.5	%
Diff Phase pos	0	0.1	Degree
Diff Phase neg	-0.2	-0.4	Degree
Diff Phase pp	0.2	0.5	Degree
Diff Phase Step1	-0.2	-0.4	Degree
Diff Phase Step2	-0.1	-0.4	Degree
Diff Phase Step3	-0.1	-0.3	Degree
Diff Phase Step4	0	0.1	Degree
Diff Phase Step5	-0.2	-0.1	Degree

4 Precautions on asymmetrical supply operation

The TSH8x device can be used with either a dual or a single supply. If a single supply is used, the inputs are biased to the mid-supply voltage ($+V_{CC}/2$). This bias network must be carefully designed so as to reject any noise present on the supply rail.

As the bias current is 15 µA, you should use a high resistance R1 (approximately 10 kΩ) to avoid introducing an offset mismatch at the amplifier's inputs.

Figure 33. Asymmetrical supply schematic diagram



C1, C2, C3 are bypass capacitors intended to filter perturbations from V_{CC}. The following capacitor values are appropriate.

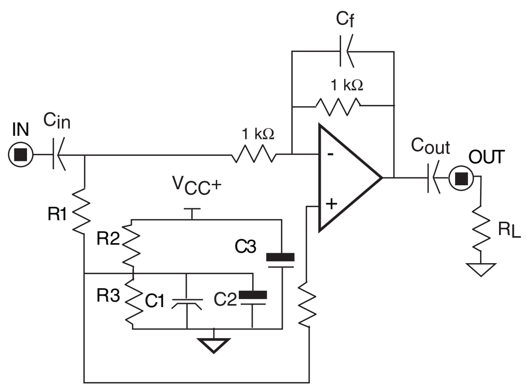
C1 = 100 nF and C2 = C3 = 100 µF

R2 and R3 are such that the current through them must be superior to 100 times the bias current. Therefore, you could use the following resistance values.

R2 = R3 = 4.7 kΩ

C_{in} and C_{out} are chosen to filter the DC signal by the low pass filters (R1, C_{in}) and (R_{out}, C_{out}). With R1 = 10 kΩ, $R_{out} = R_L = 150\ \Omega$, and $C_{in} = 2$ µF, $C_{out} = 220$ µF the cutoff frequency obtained is lower than 10 Hz.

Figure 34. Use of the TSH8x in a gain = -1 configuration



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.1 SOT23-5 package information

Figure 35. SOT23-5 package outline

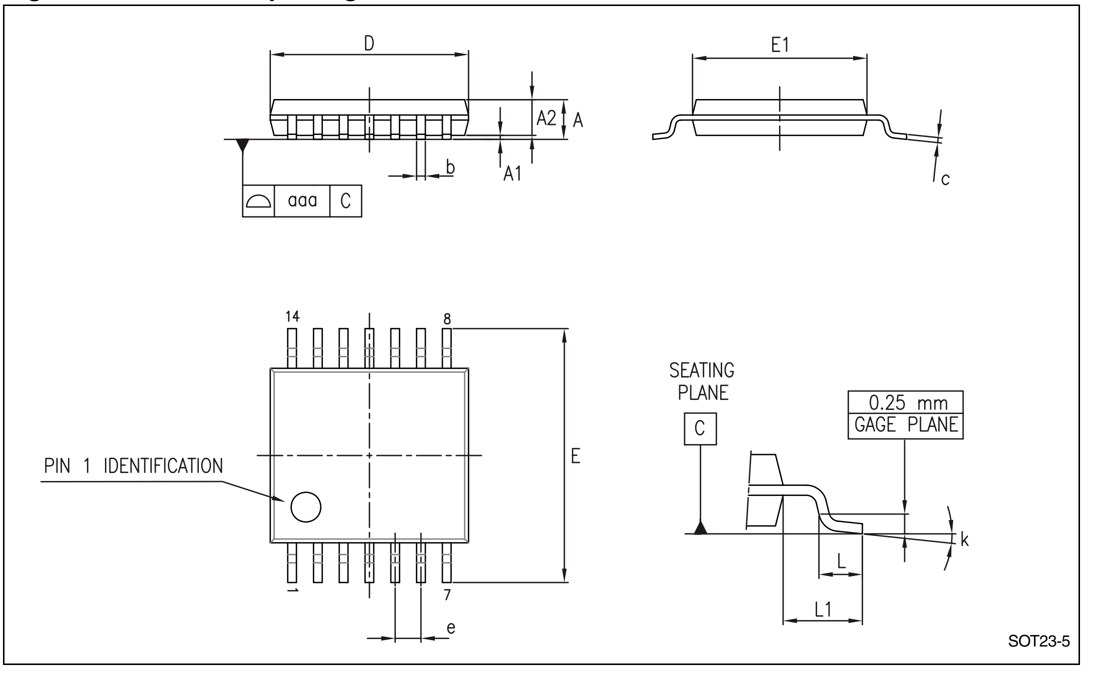


Table 8. SOT23-5 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0°		10°			

5.2 SO-8 package information

Figure 36. SO-8 package outline

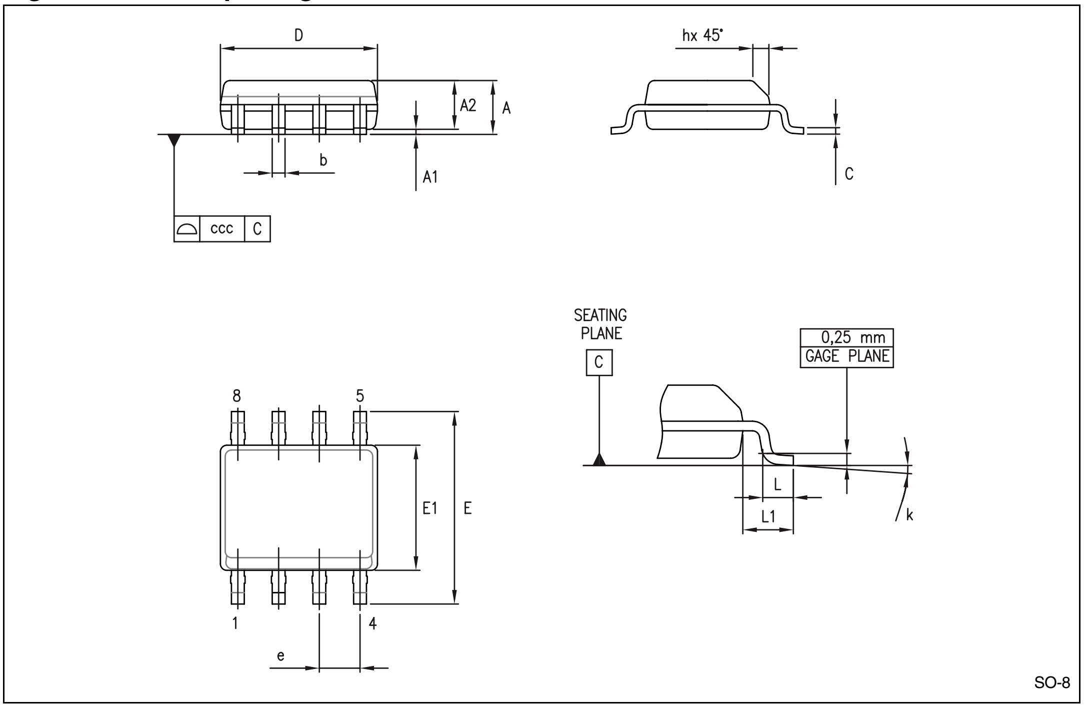


Table 9. SO-8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

5.3 TSSOP8 package information

Figure 37. TSSOP8 package outline

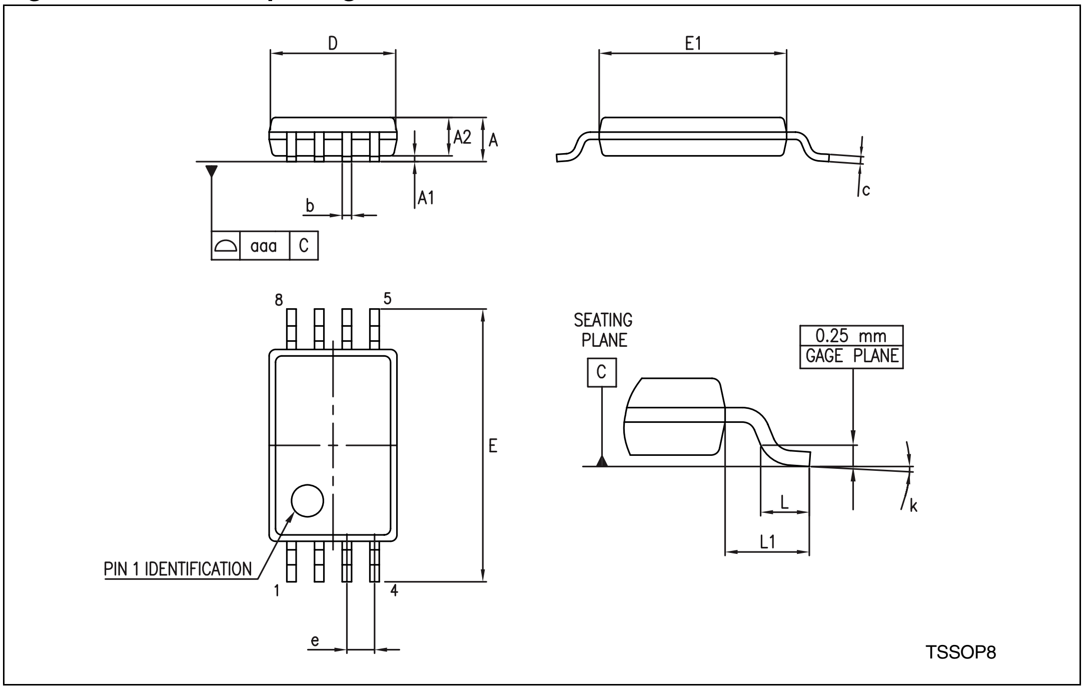


Table 10. TSSOP8 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa			0.10			0.004

5.4 TSSOP14 package information

Figure 38. TSSOP14 package outline

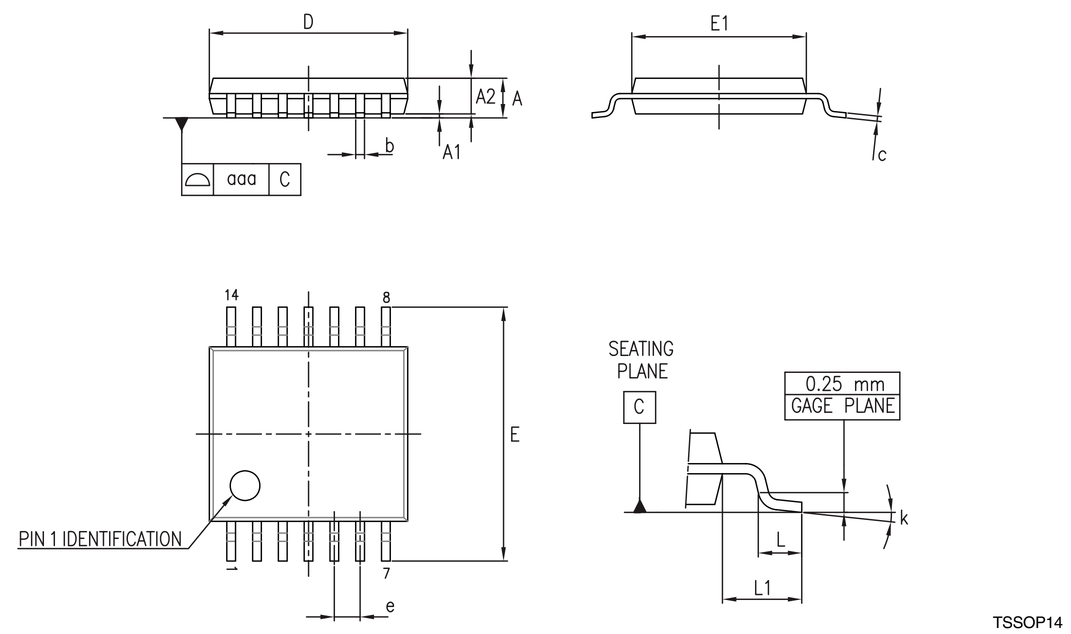


Table 11. TSSOP14 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

6 Ordering information

Table 12. Order codes

Type	Temperature range	Package	Packaging	Marking
TSH80ILT	-40 to +85 °C	SOT23-5	Tape and reel	K303
TSH80IYLT[1]		SOT23-5 (Automotive grade level)		K310
TSH80ID/DT		SO-8	Tube or tape and reel	TSH80I
TSH80IYD/IYDT[1]		SO-8 (Automotive grade level)		SH80IY
TSH81ID/DT		SO-8		TSH81I
TSH81IPT		TSSOP8	Tape and reel	SH81I
TSH82ID/DT		SO-8	Tube or tape and reel	TSH82I
TSH82IPT		TSSOP8	Tape and reel	SH82I
TSH84IPT		TSSOP14	Tape and reel	SH84I

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent are ongoing.

7 Revision history

Table 13. Document revision history

Date	Revision	Changes
1-Feb-2003	1	First release.
2-Aug-2005	2	PPAP references inserted in the datasheet, see *Table 12: Order codes on page 27*.
12-Apr-2007	3	Corrected temperature range for TSH80IYD/IYDT and TSH82IYD/IYDT order codes in *Table 12: Order codes on page 27*.
24-Oct-2007	4	TSH81IYPT PPAP references inserted in the datasheet, see *Table 12: Order codes on page 27*.
19-May-2009	5	Added data relating to the quad TSH84 device. Removed TSH81IYPT, TSH81IYD-IYDT, TSH82IYPT and TSH82IYD-IYDT order codes in *Table 12: Order codes*.
24-Jul-2012	6	Added TSSOP14 package to figure on page 1, updated titles of *Figure 1* to *Figure 30*, updated *Section 5: Package information*, removed TSH80ID-IDT, TSH80IYD, TSH81ID-IDT and TSH82ID order codes from *Table 12: Order codes*. Modified note 1 below *Table 12: Order codes*, minor corrections throughout document.