Absolute Maximum Ratings (Ta = 25°C)

Characteristics			Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating (Ta≥ 85 °C)		IF/°C	-1.6	mA/°C
	Pulse forward current	(Note 1)	I_{FP}	40	mA
	Peak transient forward current	(Note 2)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Diode power dissipation		PD	40	mW
	Diode power dissipation derating (Ta ≥ 85°C)		△PD/°C	-1.0	mW/°C
Detector	Output current		I_O	25	mA
	Output voltage		V_O	7	V
	Supply voltage (60 s maximum)		V_{CC}	7	V
	Output power dissipation		P_O	40	mW
	Output power dissipation derating (Ta≥ 85 °C)		Po/°C	-5.7	mW/°C
Operating temperature range			T_{opr}	−40 to 85	°C
Storage temperature range			T_{stg}	−55 to 125	°C
Lead solder temperature (10 s)			T_{sol}	260	°C
Isolation voltage (AC, 60 s., RH ≤ 60 %)		(Note 3)	BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 50 % duty cycle, 1 ms pulse width.

Note 2: Pulse width≤ 1 μs, 300 pps.

Note 3: This device is regarded as a two terminal device: pins 1 and 3 are shorted together, as are pins 4, 5 and 6.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input voltage, low level	V_{FL}	−3	0	1.0	V
Input current, high level	I_{FH}	13*	16	20	mA
Supply voltage**	V_{CC}	4.5	5	5.5	V
Fan out (TTL load)	N	—	—	8	—
Operating temperature	T_{opr}	0	—	70	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

* 13mA is a guard banded value which allows for at least 20 % CTR degradation.
Initial input current threshold value is 10 mA or less.

**This item denotes operating ranges, not meaning of recommended operating conditions.

Electrical Characteristics(unless otherwise specified, Ta=0 to 70°C, V_{CC}=4.5 to 5.5V, V_{FL}≤ 1.0V)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Forward voltage	V_F	I_F = 10 mA, Ta = 25 °C	—	1.65	1.80	V
Forward voltage temperature coefficient	$\Delta V_F/\Delta Ta$	I_F = 10 mA	—	−2	—	mV / °C
Reverse current	I_R	V_R = 5 V, Ta = 25 °C	—	—	10	μA
Capacitance between terminals	C_T	V_F = 0 V, f = 1 MHz, Ta = 25 °C	—	45	—	pF
High level output current	I_{OH}	V_F = 1.0 V, V_O = 5.5 V	—	—	250	μA
		V_F = 1.0 V, V_O = 5.5 V, Ta = 25 °C	—	0.5	10	
Low level output voltage	V_{OL}	I_F = 10 mA I_{OL} = 13 mA(sinking)	—	0.4	0.6	V
"H level output→ L level output" input current	I_{FH}	I_{OL} = 13 mA(sinking) V_{OL} = 0.6 V	—	—	10	mA
High level supply current	I_{CCH}	V_{CC} = 5.5 V, I_F = 0 mA	—	7	15	mA
Low level supply current	I_{CCL}	V_{CC} = 5.5 V, I_F = 16 mA	—	12	18	mA
Input−output insulation leakage current	I_S	V_S = 3540 V, t = 5 s Ta = 25 °C (Note 1)	—	—	100	μA
Isolation resistance	R_S	R.H. ≤ 60 %, V_S = 500 VDC Ta = 25 °C (Note 1)	5×10^{10}	10^{14}	—	Ω
Stray capacitance between input to output	C_S	V_S = 0 V, f = 1 MHz Ta = 25 °C (Note 1)	—	0.8	—	pF

* All typical values are V_{CC} = 5 V, Ta = 25 °C

Note1: Device considered a two−terminal device: Pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.

Switching Characteristics (V_{CC}=5V, Ta=25°C)

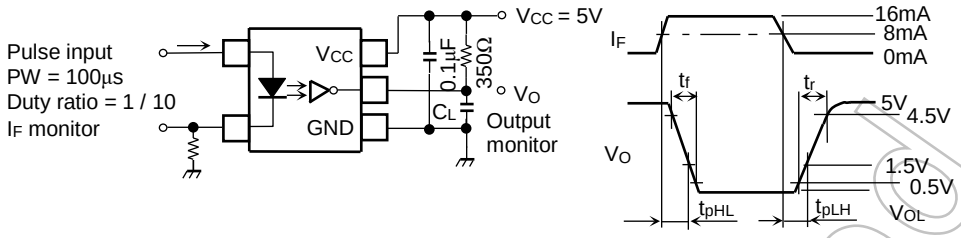
Characteristics	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time (H→L)	t_{pHL}	1	I_F = 0→16 mA C_L = 15 pF, R_L = 350 Ω	—	60	120	ns
Propagation delay time (L→H)	t_{pLH}	1	I_F = 16→0 mA C_L = 15 pF, R_L = 350 Ω	—	60	120	ns
Output rise−fall time (10−90%)	t_r, t_f	1	R_L = 350 Ω, C_L = 15 pF I_F = 0 ⇄ 16 mA	—	30	—	ns
Common mode transient immunity at high output level	CM_H	2	I_F = 0 mA, V_{CM} = 200V $_{p-p}$ $V_{O(min)}$ = 2 V, R_L = 350 Ω	—	200	—	V / μs
Common mode transient immunity at low output level	CM_L	2	I_F = 16 mA, V_{CM} = 200 V_{p-p} $V_{O(max)}$ = 0.8 V, R_L = 350 Ω	—	−500	—	V / μs

Note: The V_{CC} supply voltage to each TLP113 isolator must be bypassed by 0.1 μF capacitor, this can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to package V_{CC} and GND pins of each device.

Note: CMH is the maximum rising common mode voltage waveform (voltage/time) that can keep high level (VO> 2.0 V)

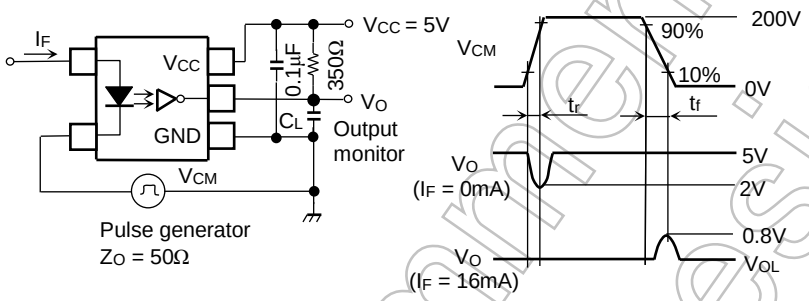
Note: CML is the maximum falling common mode voltage waveform (voltage/time) that can keep low level (VO <0.8 V).

Test Circuit 1: Switching Time Test Circuit



C_L is approximately 15pF which includes probe and stray wiring capacitance.

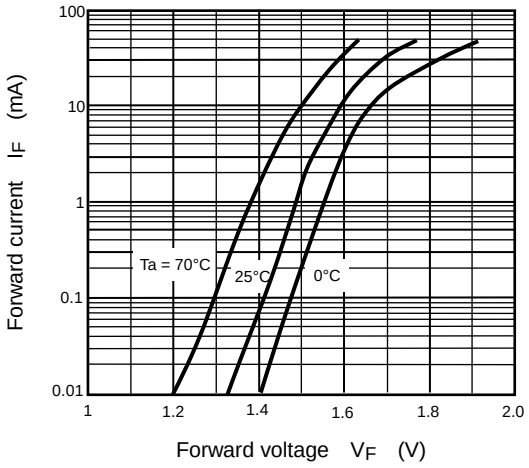
Test Circuit 2: Common Mode Transient Immunity Test Circuit



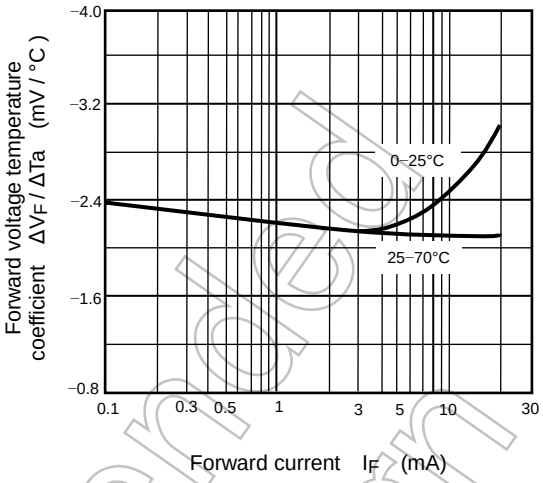
$$CM_H = \frac{160(V)}{t_r(\mu s)}, CM_L = \frac{160(V)}{t_f(\mu s)}$$

C_L is approximately 15pF which includes probe and stray wiring capacitance.

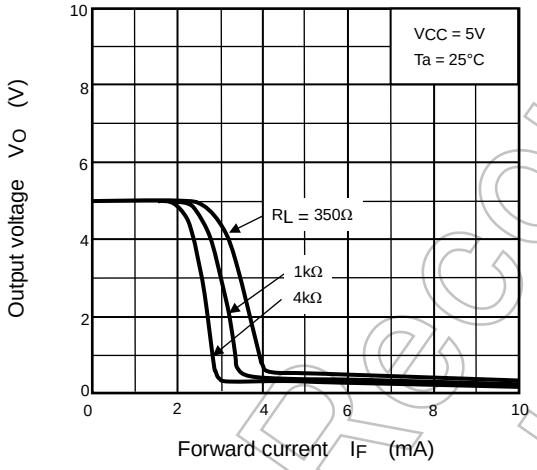
$I_F - V_F$



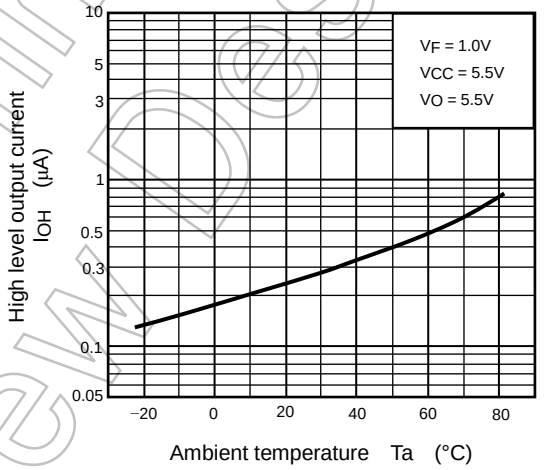
$\Delta V_F / \Delta Ta - I_F$



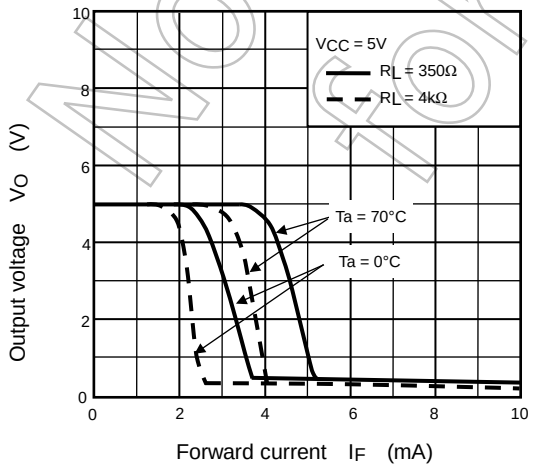
$V_O - I_F$



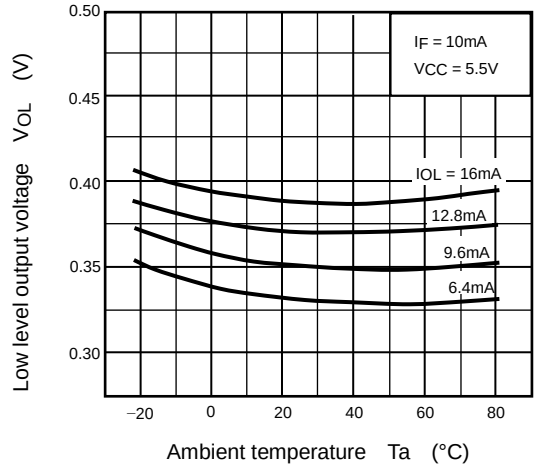
$I_{OH} - Ta$



$V_O - I_F$

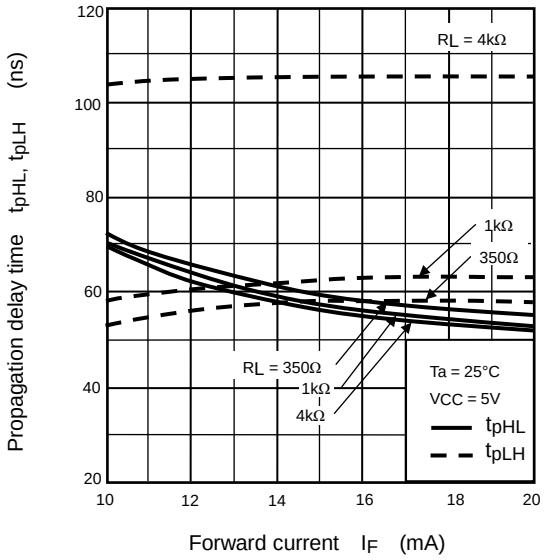


$V_{OL} - Ta$

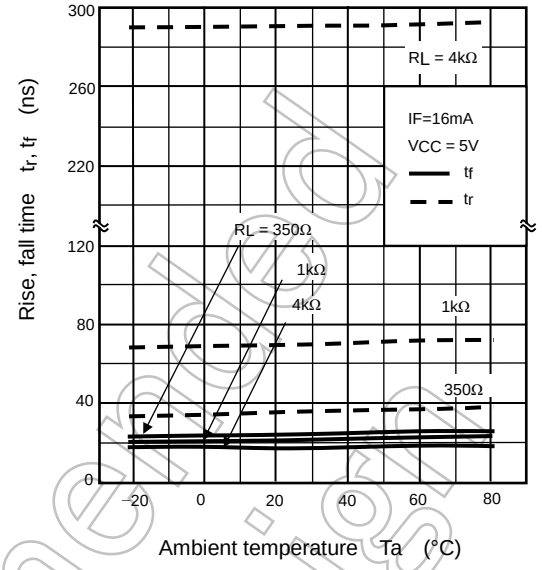


NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

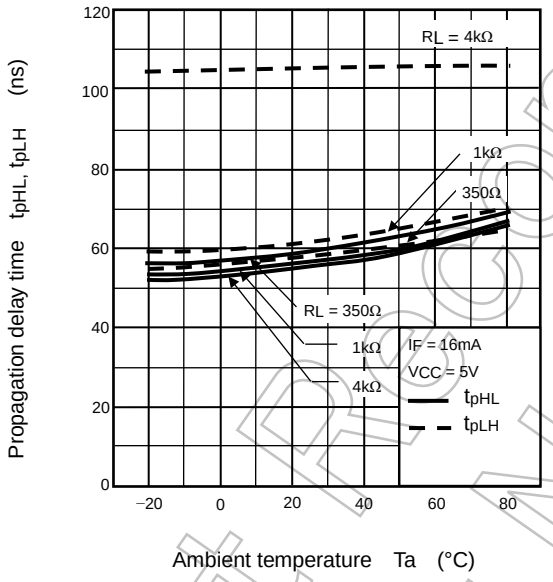
t_{pHL} , t_{pLH} – I_F



t_r, t_f – T_a



t_{pHL} , t_{pLH} – Ta



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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