- Intelligent DC-to-DC converter maximizes audio headroom from any supply level and limits current consumption at low battery voltages
- Compatible with standard Acoustic Echo Cancellers (AECs)
- High efficiency and low power dissipation
- Wide supply voltage range (fully operational from 2.8 V to 5.5 V)
- TDM audio interface configurable from 2 slots (I^2S) up to 16 slots
- I^2C-bus control interface (400 kHz)
- Dedicated speech mode with speech activity detector
- Speaker current and voltage monitoring (via the TDM-bus) for Acoustic Echo Cancellation (AEC) at the host
- Fully short-circuit proof across the load and to the supply lines
- Sample frequencies from 8 kHz up to 48 kHz supported
- Option to route TDM input direct to TDM output to allow a second TDM input slave device to be used in combination with the TFA9896
- Volume control
- Low RF susceptibility
- Input clock jitter insensitive interface
- Thermally protected
- Low ‘pop noise' at all mode transitions

3 Applications

- Mobile phones
- Tablets
- Portable gaming devices
- Portable Navigation Devices (PND)
- Notebooks/Netbooks
- MP3 players and portable media players

4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}	2.8	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
$V_{DD(IO)}$	input/output supply voltage	on pin $V_{DD(IO)}$	1.65	1.8	1.95	V
I_{BAT}	battery supply current	on pin V_{BAT} and in the DC-to-DC converter coil; Operating modes with load; DC-to-DC converter in Adaptive boost mode (no output signal)	-	1.75	-	mA
		on pin V_{BAT} and in the DC-to-DC converter coil; Power-down mode	-	-	1	µA
I_{DDD}	digital supply current	on pin V_{DDD}; Operating modes; SpeakerBoost protection activated	-	17	-	mA
		on pin V_{DDD}; Operating modes; CoolFlux DSP bypassed	-	6	-	mA
		on pin V_{DDD}; Power-down mode; BCK = FS = DIO = GAINIO = 0 V	-	10	-	µA
$I_{DD(IO)}$	input/output supply current	on pin $V_{DD(IO)}$; Operating modes; SpeakerBoost protection activated; I^2S configured TDM	-	100	-	µA
$P_{o(RMS)}$	RMS output power	R_L = 8 Ω	-	2.1	-	W
R_L	load resistance	of speaker	3.2	8	-	Ω

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9896UK	WLCSP30	wafer level chip-size package; 30 bumps; 2.06 × 2.72 × 0.50 mm	SOT1443-3
TFA9896BUK[1]			

[1] TFA9896BUK with backside coating

6 Block diagram

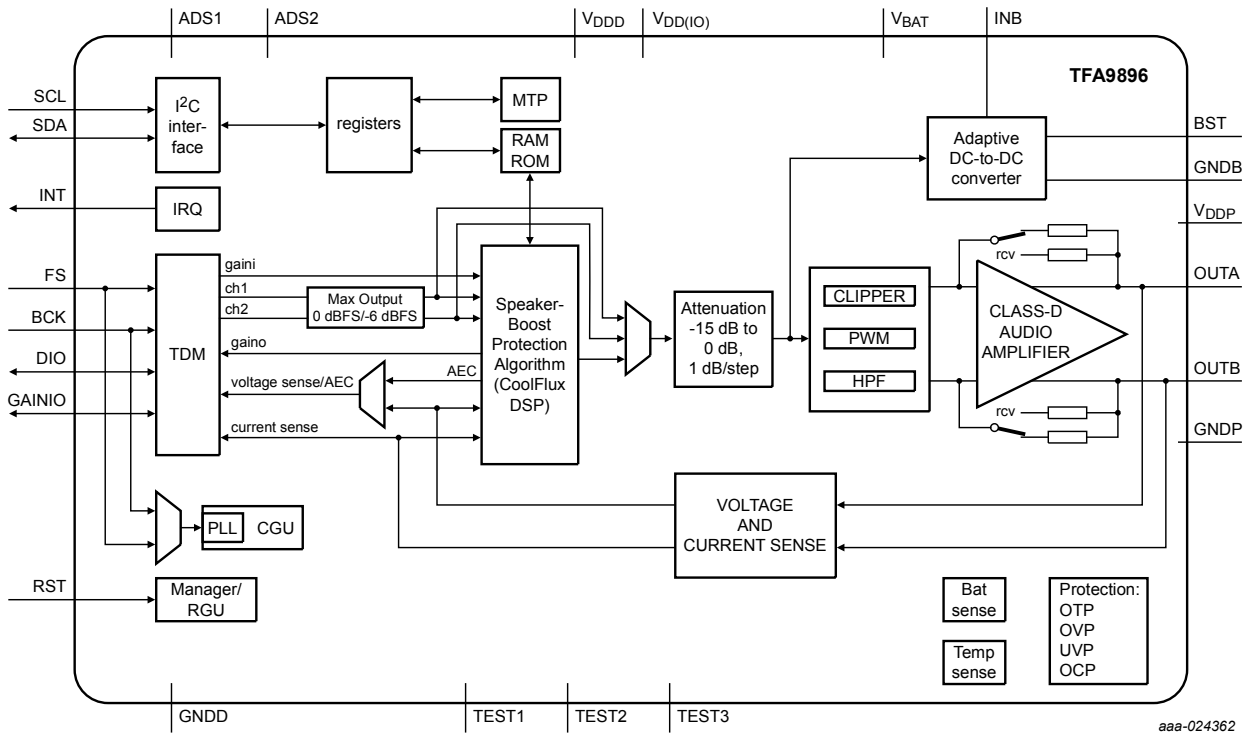
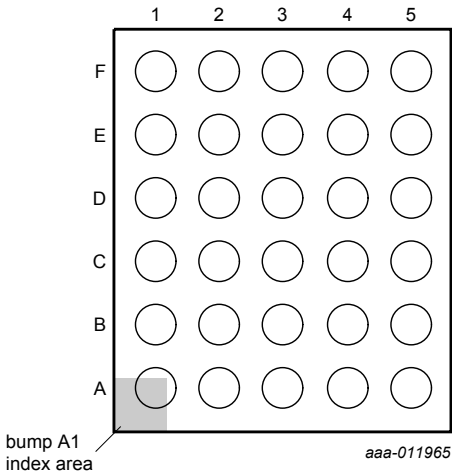


Figure 1. Block diagram

7 Pinning information

7.1 Pinning



Bottom view showing A1 marking

	1	2	3	4	5
A	SCL	SDA	BCK	FS	GAINIO
B	$V_{DD(IO)}$	ADS1	GNDD	INT	DIO
C	V_{DDD}	ADS2	GNDD	TEST3	RST
D	TEST1	TEST2	GNDD	GNDD	V_{BAT}
E	GNDB	GNDB	GNDD	GNDP	GNDD
F	INB	BST	OUTA	V_{DDP}	OUTB

aaa-011966

Bump mapping

Figure 2. Bump configuration

7.2 Pin description

Table 3. Pinning

Symbol	Pin	Type	Description
SCL	A1	I	I^2C-bus clock input
SDA	A2	I/O	I^2C-bus data input/output
BCK	A3	I	digital audio bit clock
FS	A4	I	word select or frame sync
GAINIO	A5	I/O	digital audio I/O; also used as gain sync for stereo
$V_{DD(IO)}$	B1	P	digital I/O supply
ADS1	B2	I	address select 1
GNDD	B3	P	digital ground
INT	B4	O	interrupt output configurable as push pull or open drain output
DIO	B5	I/O	digital audio IO also used as I^2S input
V_{DDD}	C1	P	digital core supply voltage
ADS2	C2	I	address select 2
GNDD	C3	P	digital ground
TEST3	C4	I	test signal input 3; for test purposes only, connect to PCB ground
RST	C5	I	reset input
TEST1	D1	I	test signal input 1; for test purposes only, connect to PCB ground
TEST2	D2	I	test signal input 2; for test purposes only, connect to PCB ground
GNDD	D3	P	digital ground
GNDD	D4	P	digital ground
V_{BAT}	D5	I	battery supply sense input
GNDB	E1	P	DC-to-DC booster ground
GNDB	E2	P	DC-to-DC booster ground
GNDD	E3	P	digital ground
GNDP	E4	P	class-D power ground
GNDD	E5	P	digital ground
INB	F1	P	DC-to-DC booster input
BST	F2	P	DC-to-DC booster output
OUTA	F3	O	non-inverting output
V_{DDP}	F4	P	class-D power supply
OUTB	F5	O	inverting output

8 Functional description

The TFA9896 is a highly efficient mono Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated SpeakerBoost protection algorithm. Figure 1 is a block diagram of the TFA9896.

The device contains two TDM input/output channels. The number of slots and number of bits per slot can be configured for each TDM channel and the channel can be configured as input or output. Typically, one TDM channel is configured as a standard I2S input while the other TDM channel is used for stereo sync, where gain information is transferred between the devices.

It is also possible to output current sense and voltage sense information on the TDM interface, which can be processed by the audio host.

The SpeakerBoost protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core, maximizes the acoustical output of the speaker while limiting membrane excursion and voice coil temperature to a safe level. The mechanical protection implemented guarantees that speaker membrane excursion never exceeds its rated limit, to an accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to an accuracy of ±10 °C. Furthermore, advanced signal processing ensures the audio quality remains acceptable at all times.

The protection algorithm implements an adaptive loudspeaker model that is used to predict the extent of membrane excursion. The model is continuously updated to ensure that the protection scheme remains effective even when speaker parameter values change or the acoustic enclosure is modified.

The SpeakerBoost protection algorithm boosts the output sound pressure level within given mechanical, thermal and quality limits. An optional Bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high quality music in quiet environments.

The frequency response of the TFA9896 can be modified via ten fully programmable cascaded second-order biquad filters. The first two biquads are processed with 48-bit double precision; biquads 3 to 8 are processed with 24-bit single precision.

A battery supply safeguard mechanism can be configured to reduce the gain at low battery voltage levels to limit battery current.

The output volume can be controlled by the SpeakerBoost protection algorithm or by the host application (external). In the latter case, the boost features of the SpeakerBoost protection algorithm must be disabled to avoid neutralizing external volume control.

The SpeakerBoost protection algorithm output is converted into two pulse width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

The adaptive DC-to-DC converter boosts the battery supply voltage in line with the output of the SpeakerBoost protection algorithm. It switches to Follower mode ($V_{BST} = V_{BAT}$; no boost) when the audio output voltage is lower than the battery voltage.

8.1 Protection mechanisms

The following protection circuits are included in the TFA9896:

- OverTemperature Protection (OTP)
- OverVoltage Protection (OVP)
- UnderVoltage Protection (UVP)
- OverCurrent Protection (OCP)

The reaction of the device to fault conditions differs depending on the protection circuit involved. The status of these protection circuits can be monitored via the relevant status bits in the System status register, which can be configured to generate interrupts.

8.1.1 OverTemperature Protection (OTP)

OTP prevents heat damage to the TFA9896. It is triggered when the junction temperature exceeds $T_{act(th\_prot)}$. The output stages are set floating. OTP is cleared automatically via an internal timer (approximately 200 ms), after which the output stages start to operate normally again. The overtemperature status can be monitored via the I^2C-bus.

8.1.2 Supply voltage protection (UVP and OVP)

If V_{BAT} drops below the undervoltage protection threshold, $V_{P(uvp)}$, UVP is activated, setting the outputs floating. The system is restarted approximately 200 ms after the supply voltage rises above $V_{P(uvp)}$ again.

If the power supply voltage (V_{DDP}) rises above the overvoltage protection threshold, $V_{P(ovp)}$, OVP is activated, setting the booster to Follower mode. The power stages are re-enabled as soon as the supply voltage drops below $V_{P(ovp)}$ again. The system will be restarted after approximately 200 ms. The undervoltage and overvoltage status can be monitored via the I^2C-bus.

8.1.3 OverCurrent Protection (OCP)

OCP detects a short circuit across the load or between one of the amplifier outputs and one of the supply lines. If the output current exceeds the overcurrent protection threshold ($I_{O(ocp)}$), it is limited to $I_{O(ocp)}$ while the amplifier outputs are switching (the amplifier is not powered down completely). The amplifier can distinguish between an impedance drop at the loudspeaker and a low-ohmic short circuit across the load or to one of the supply lines. The impedance threshold depends on which supply voltage is being used:

- In the event of a short circuit across the load or a short to one of the supply lines, the audio amplifier is switched off completely. It will try to restart again after approximately 200 ms at a sample rate, f_s, of 48 kHz. If the short-circuit condition is still present after this time, this cycle will be repeated. Average dissipation is low because of the short duty cycle.
- The same protection mechanism is activated in the event of an impedance drop (e.g. due to dynamic behavior of the loudspeaker). The maximum output current is again limited to $I_{O(ocp)}$, but the amplifier does not switch off completely (preventing audio holes from occurring). The result is a clipped output signal without artifacts.

9 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x	pin INB	-0.3	+7.3	V
		pins GAINIO, DIO, BCK, FS, INT, SCL, SDA, ADS1, ADS2 and RST	-0.3	+1.95	V
V_{BAT}	battery supply voltage	on pin VBAT	-0.3	+6	V
V_{DDP}	power supply voltage	on pin V_{DDP}	-0.3	+7.3	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	-0.3	+1.95	V
$V_{DD(IO)}$	input/output supply voltage	on pin $V_{DD(IO)}$	-0.3	+1.95	V
T_j	junction temperature		-	+150	°C
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
V_{ESD}	electrostatic discharge voltage	according to Human Body Model (HBM)	-2	+2	kV
		according to Charge Device Model (CDM)	-500	+500	V

10 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer application board positioned vertically in free air; dimensions: 30 × 19 × 1.6 mm; natural convection; copper coverage one each layer > 95 %; copper thickness outer/ inner layer 35 µm	60	K/W

11 Characteristics

11.1 DC characteristics

Table 6. DC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 6.1 V; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}	2.8	-	5.5	V
V_{DDP}	power supply voltage	on pin V_{DDP}	2.8	-	6.2	V
V_{DDD}	digital supply voltage	on pin V_{DDD}	1.65	1.8	1.95	V
$V_{DD(IO)}$	input/output supply voltage	on pin $V_{DD(IO)}$	1.65	1.8	1.95	V
I_{BAT}	battery supply current	on pin V_{BAT} and in the DC-to-DC converter coil; Operating modes with load; DC-to-DC converter in Adaptive boost mode (no output signal)	-	1.75	-	mA
		on pin V_{BAT} and in the DC-to-DC converter coil; Power-down mode	-	-	1	µA
I_{DDD}	digital supply current	on pin V_{DDD}; Operating modes; SpeakerBoost Protection activated	-	17	-	mA
		on pin V_{DDD}; Operating modes; CoolFlux DSP bypassed	-	6	-	mA
		on pin V_{DDD}; Power-down mode; BCK = FS = DIO = GAINIO = 0 V	-	10	-	µA
$I_{DD(IO)}$	input/output supply current	on pin $V_{DD(IO)}$; Operating modes; SpeakerBoost protection activated; I^2S configured TDM	-	100	-	µA
Pins BCK, FS, DIO, GAINIO, RESET, ADS1, ADS2, SCL, SDA						
V_{IH}	HIGH-level input voltage		$0.7V_{DD(IO)}$	-	1.95	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(IO)}$	V
C_i	input capacitance	[2]	-	-	3	pF
I_{LI}	input leakage current	1.8 V on input pin	-	-	0.1	µA
Pins DIO, GAINIO, INT						
V_{OH}	HIGH-level output voltage	-	$V_{DD(IO)}$ - 0.4	-	-	V
I_{LI}	input leakage current	1.8 V on input pin	-	-	0.1	µA
Pin SDA: open-drain output						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	400	mV
Pins OUTA, OUTB						
R_{DSon}	drain-source on-state resistance	V_{DDP} = 6.1 V	-	200	-	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Protection						
$T_{act(th\_prot)}$	thermal protection activation temperature		130	-	150	°C
$V_{P(ovp)}$	overvoltage protection supply voltage	protection on V_{DDP}	6.2	-	6.5	V
$V_{P(uvp)}$	undervoltage protection supply voltage	protection on V_{BAT}	2.5	-	2.8	V
$I_{O(ocp)}$	overcurrent protection output current		2.0	-	-	A
DC-to-DC converter						
$V_{O(BST)}$	output voltage on pin BST	DCVO2 = 111; Boost mode	6.0	6.1	6.2	V

[1] L_{BST} = boot converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production; value is guaranteed by design and checked during product validation.

11.2 AC characteristics

Table 7. AC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 6.1 V; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Amplifier						
$P_{o(RMS)}$	RMS output power	THD+N = 1 %; RCV = 0				
		R_L = 4 Ω; V_{BAT} = 4.0 V	-	3.2	-	W
		R_L = 8 Ω	-	2.1	-	W
		THD+N = 10 %; RCV = 0				
		R_L = 4 Ω; V_{BAT} = 4.0 V	-	4	-	W
		R_L = 8 Ω	-	2.55	-	W
		THD+N = 1 %; RCV = 1	-	0.68	-	W
R_L	load resistance	of speaker	3.2	8	-	Ω
$\|V_{O(offset)}\|$	output offset voltage	absolute value	-	-	1	mV
η_{po}	output power efficiency	including DC-to-DC converter; $P_{o(RMS)}$ = 2.1 W; V_{BAT} = 4.0 V [2]	-	83	-	%
THD+N	total harmonic distortion-plus-noise	$P_{o(RMS)}$ = 100 mW; R_L = 8 Ω; L_L = 44 µH [2]	-	0.03	0.1	%
$V_{n(o)}$	output noise voltage	A-weighted; DATAI1 = DATAI2 = 0 V				
		CoolFlux DSP disabled and bypassed	-	27	-	µV
		CoolFlux DSP enabled [2]	-	30	-	µV
		Receiver mode; V_{DDP} ≤ 4.3 V	-	18	-	µV
S/N	signal-to-noise ratio	V_O = 4.5 V (peak); A-weighted				
		CoolFlux DSP disabled and bypassed	-	103	-	dB
		CoolFlux DSP enabled [2]	-	100	-	dB
PSRR	power supply rejection ratio	V_{ripple} = 200 mV (RMS); f_{ripple} = 217 Hz	-	90	-	dB
Current-sensing performanceS/N						
S/N	signal-to-noise ratio	I_O = 1.2 A (peak); A-weighted	-	75	-	dB
$I_{sense(acc)}$	sense current accuracy	I_O = 0.5 A (peak)	-3	-	+3	%
B	bandwidth	[2]	-	-	3	kHz
Timing						
$t_{d(on)}$	turn-on delay time	PLL locked on BCK (IPLL = 0)				
		f_s = 32 kHz to 48 kHz	-	-	2	ms
		PLL locked on FS (IPLL = 1)				
		f_s = 48 kHz	-	-	6	ms
$t_{d(off)}$	turn-off delay time		-	-	10	µs
$t_{d(mute\_off)}$	mute off delay time		-	1	-	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(soft\_mute)}$	soft mute delay time		-	12	-	ms
t_{PD}	propagation delay	CoolFlux bypassed				
		f_s = 8 kHz	-	-	3.5	ms
		f_s = 48 kHz	-	-	600	µs
		SpeakerBoost protection mode, $t_{LookAhead}$ = 2 ms				
		f_s = 8 kHz	-	-	25	ms
		f_s = 48 kHz	-	-	4	ms

[1] L_{BST} = boot converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production; value is guaranteed by design and checked during product validation.

12 Application diagrams

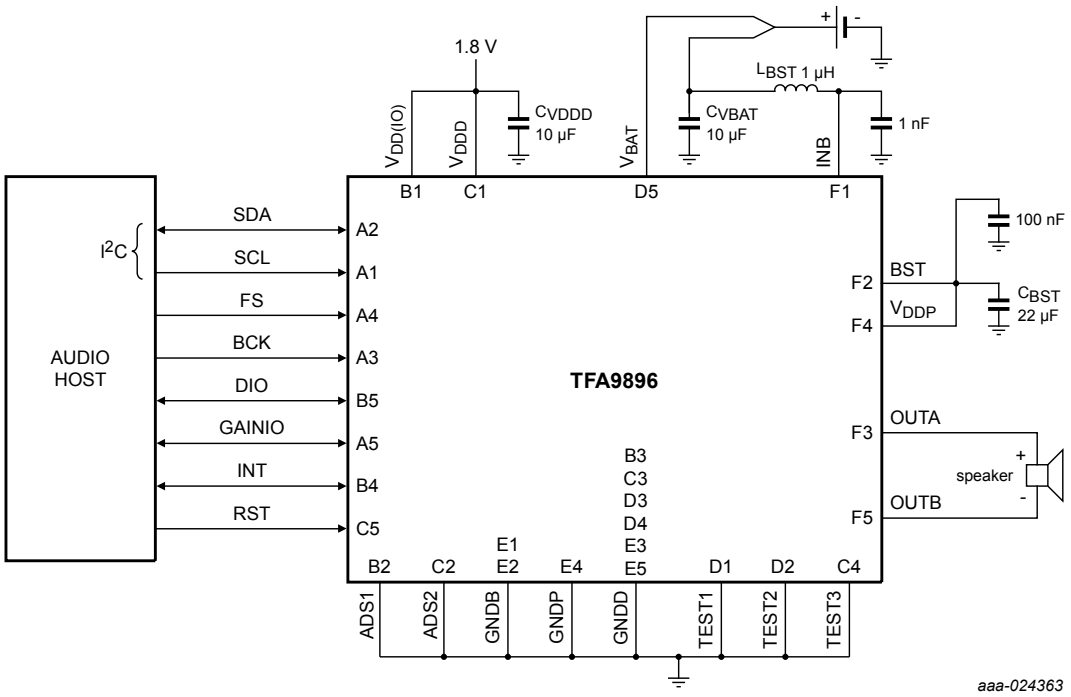


Figure 3. Typical mono application (simplified)

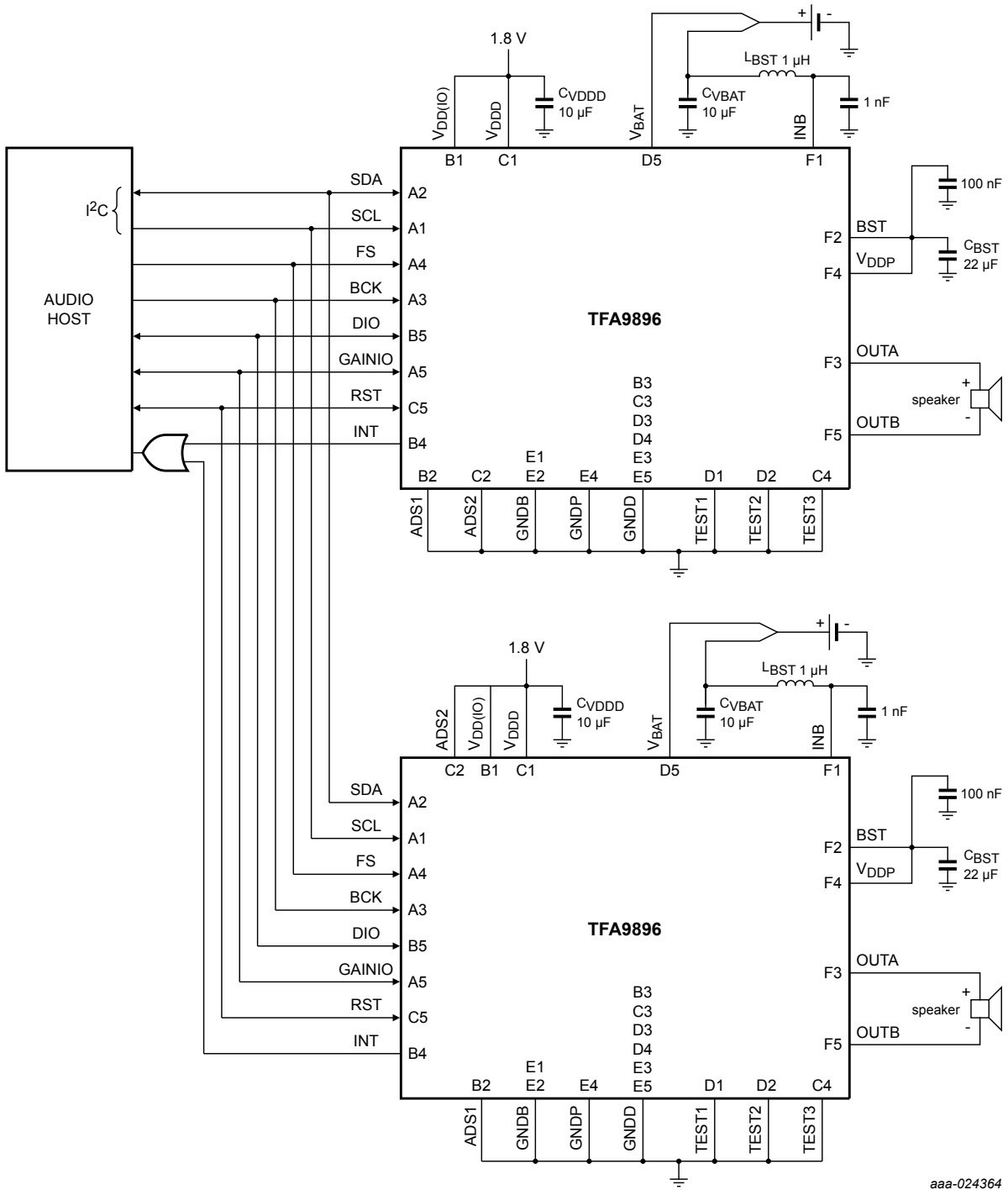
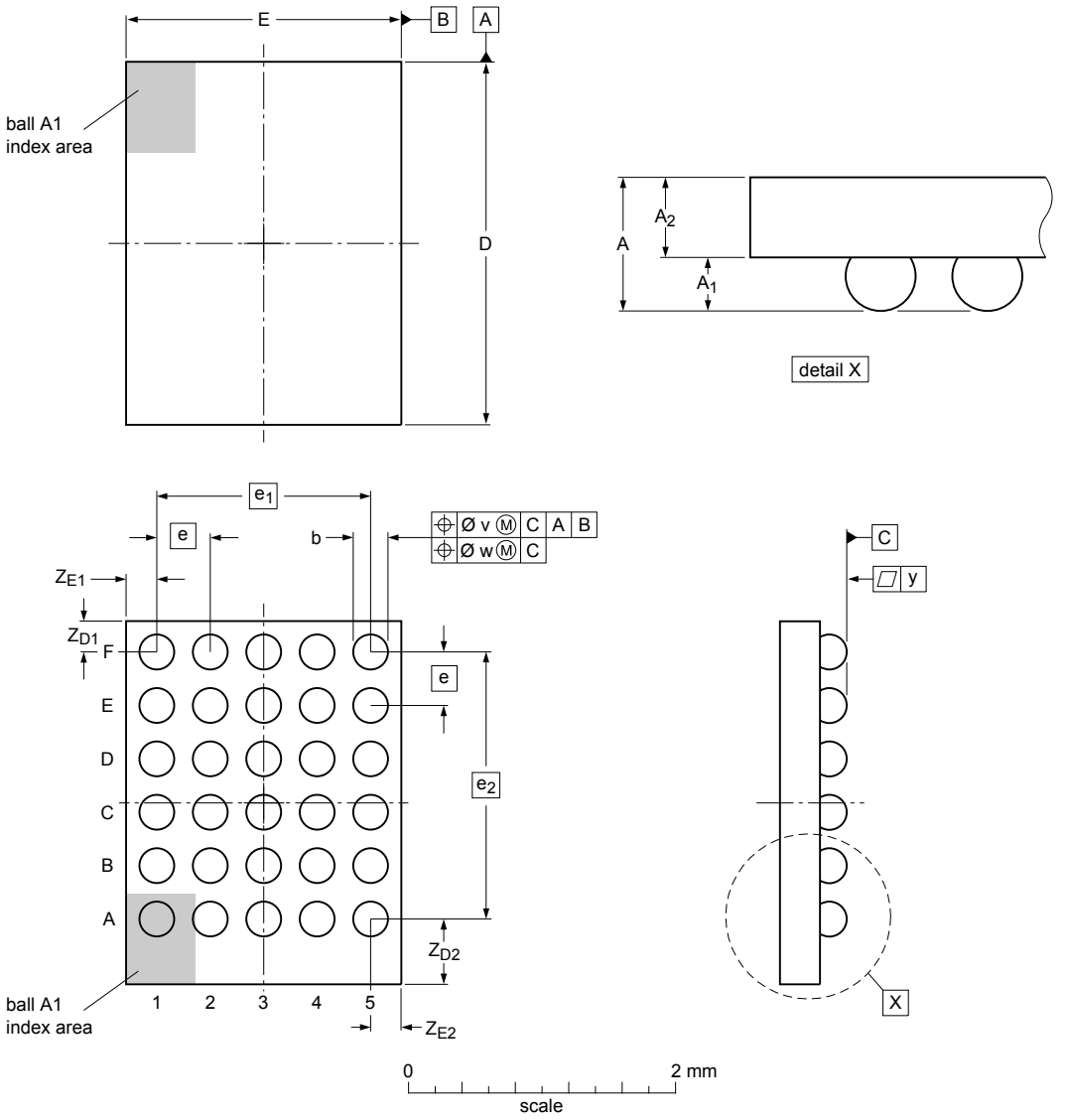


Figure 4. Typical stereo application (simplified)

13 Package outline

WLCSP30: wafer level chip-scale package; 30 bumps; 2.06 x 2.72 x 0.50 mm **SOT1443-1**



Dimensions (mm are the original dimensions)

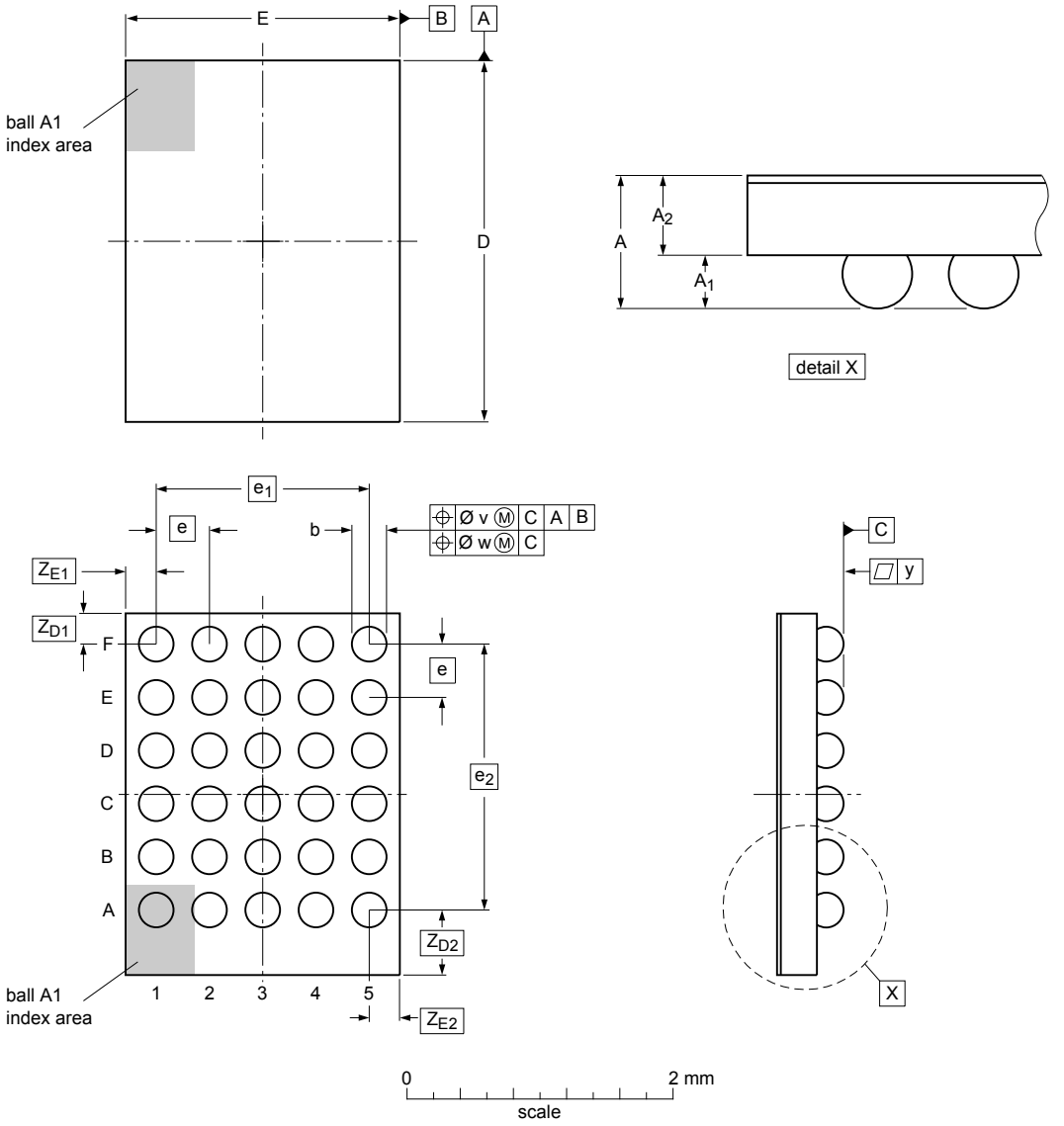
Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}	v	w	y
mm	max	0.54	0.23	0.325	0.28	2.75	2.09										
	nom	0.50	0.20	0.300	0.26	2.72	2.06	0.4	1.6	2.0	0.23	0.49	0.23	0.23	0.05	0.02	0.03
	min	0.46	0.17	0.275	0.24	2.69	2.03										

sot1443-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1443-1						~~16-01-25~~ 16-06-01

Figure 5. Package outline TFA9896UK (WLCSP30)

WLCSP30: wafer level chip-scale package; 30 bumps; 2.06 x 2.72 x 0.525 mm (backside coating included) **SOT1443-3**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	Z_{D1}	Z_{D2}	Z_{E1}	Z_{E2}	v	w	y
mm	max	0.565				2.75	2.09										
	nom	0.525	0.20	0.33	0.26	2.72	2.06	0.4	1.6	2.0	0.23	0.49	0.23	0.23	0.05	0.02	0.03
	min	0.485				2.69	2.03										

Note: Backside coating 25 µm

sot1443-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1443-3						~~15-03-13~~ 16-01-25

Figure 6. Package outline TFA9896BUK (WLCSP30)

14 Soldering of WLCSP packages

14.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

14.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

14.3 Reflow soldering

Key characteristics in reflow soldering are:

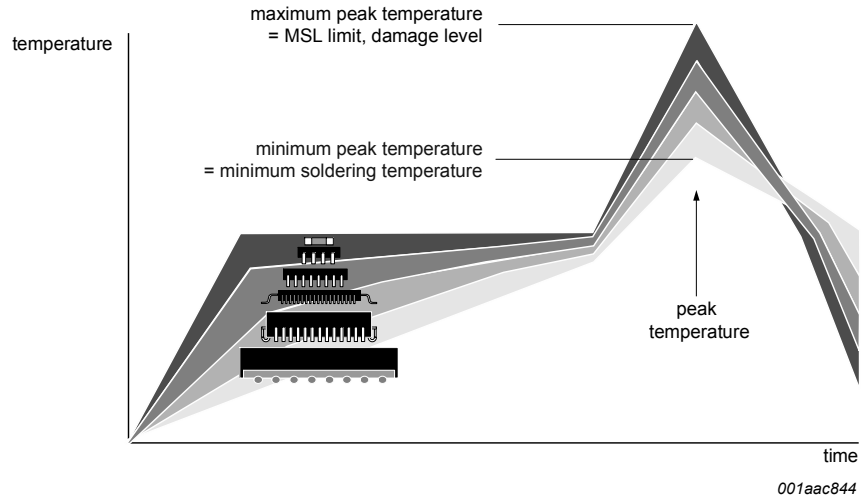
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 1) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8.

Table 8. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 1.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 7.



MSL: Moisture Sensitivity Level

Figure 7. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

14.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip
  The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

14.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

14.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description*".

14.3.4 Cleaning

Cleaning can be done after reflow soldering.

15 Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9896 v.1.0	20161222	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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