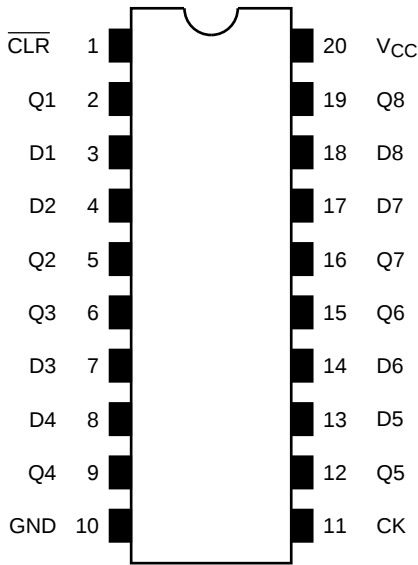
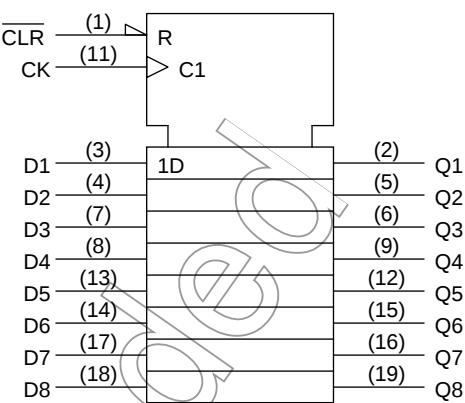


Pin Assignment (top view)



IEC Logic Symbol

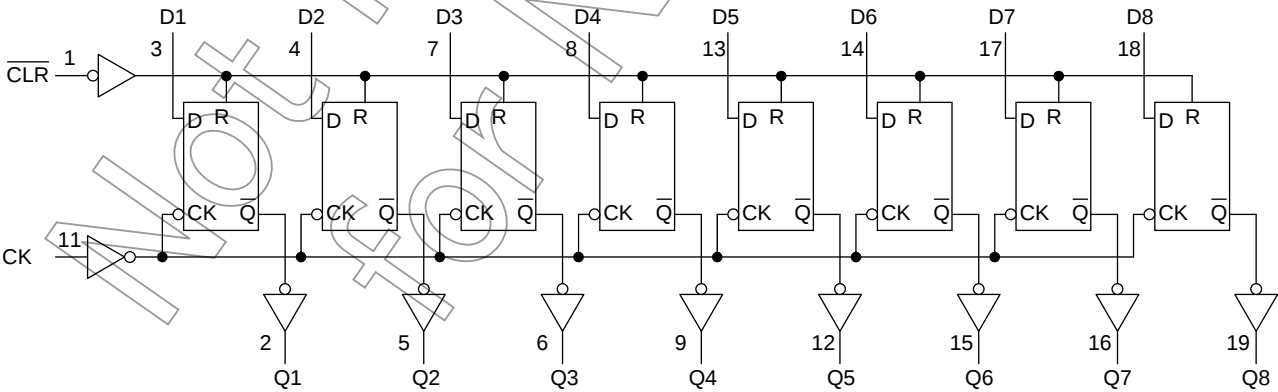


Truth Table

Inputs			Outputs	Function
CLR	D	CK	Q	
L	X	X	L	Clear
H	L		L	—
H	H		H	—
H	X		Q _n	No change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5~7.0	V
DC input voltage	V_{IN}	-0.5~7.0	V
DC output voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC} /ground current	I_{CC}	±75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0~5.5	V
Input voltage	V_{IN}	0~5.5	V
Output voltage	V_{OUT}	0~ V_{CC}	V
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~100 ($V_{CC} = 3.3 \pm 0.3$ V) 0~20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C			Ta = -40~85°C		Unit	
					VCC (V)	Min	Typ.	Max	Min		Max
Input voltage	“H” level	VIH	—	2.0	1.50	—	—	1.50	—	V	
				3.0~5.5	VCC × 0.7	—	—	VCC × 0.7	—		
	“L” level	VIL	—	2.0	—	—	0.50	—	0.50		
				3.0~5.5	—	—	VCC × 0.3	—	VCC × 0.3		
Output voltage	“H” level	VOH	VIN = VIH or VIL	IOH = -50 μA	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
				IOH = -4 mA	4.5	4.4	4.5	—	4.4	—	
					3.0	2.58	—	—	2.48	—	
				IOH = -8 mA	4.5	3.94	—	—	3.80	—	
					—	—	—	—	—	—	
	“L” level	VOL	VIN = VIH or VIL	IOL = 50 μA	2.0	—	0	0.1	—	0.1	
					3.0	—	0	0.1	—	0.1	
				IOL = 4 mA	4.5	—	0	0.1	—	0.1	
					3.0	—	—	0.36	—	0.44	
				IOL = 8 mA	4.5	—	—	0.36	—	0.44	
					—	—	—	—	—	—	
Input leakage current		IIN	VIN = 5.5 V or GND	0~5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current		ICC	VIN = VCC or GND	5.5	—	—	4.0	—	40.0	μA	

Timing Requirements (Input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40~85°C		Unit
			V _{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	t_w (L) t_w (H)	—	3.3 ± 0.3	—	5.5	6.5	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width ($\overline{\text{CLR}}$)	t_w (L)	—	3.3 ± 0.3	—	5.0	6.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	t_s	—	3.3 ± 0.3	—	5.5	6.5	ns
			5.0 ± 0.5	—	4.5	4.5	
Minimum hold time	t_h	—	3.3 ± 0.3	—	1.0	1.0	ns
			5.0 ± 0.5	—	1.0	1.0	
Minimum removal time ($\overline{\text{CLR}}$)	t_{rem}	—	3.3 ± 0.3	—	2.5	2.5	ns
			5.0 ± 0.5	—	2.0	2.0	

AC Characteristics (Input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit
			V _{CC} (V)	C _L (pF)	Min	Typ.	Max	
Propagation delay time (CK-Q)	t_{PLH} t_{PHL}	—	3.3 ± 0.3	15	—	8.7	13.6	ns
				50	—	11.2	17.1	
			5.0 ± 0.5	15	—	5.8	9.0	
				50	—	7.3	11.0	
Propagation delay time ($\overline{\text{CLR}}$ -Q)	t_{PHL}	—	3.3 ± 0.3	15	—	8.9	13.6	ns
				50	—	11.4	17.1	
			5.0 ± 0.5	15	—	5.2	8.5	
				50	—	6.7	10.5	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	75	120	—	MHz
				50	50	75	—	
			5.0 ± 0.5	15	120	165	—	
				50	80	110	—	
Output to output skew	t_{osLH}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	ns
	t_{osHL}		5.0 ± 0.5	50	—	—	1.0	
Input capacitance	C _{IN}	—	—	—	—	4	10	pF
Power dissipation capacitance	C _{PD}	(Note 2)	—	—	—	31	—	pF

Note 1: This parameter is guaranteed by design.

$$t_{\text{osLH}} = |t_{\text{PLHm}} - t_{\text{PLHn}}|, t_{\text{osHL}} = |t_{\text{PHLm}} - t_{\text{PHLn}}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}/8 \text{ (per F/F)}$$

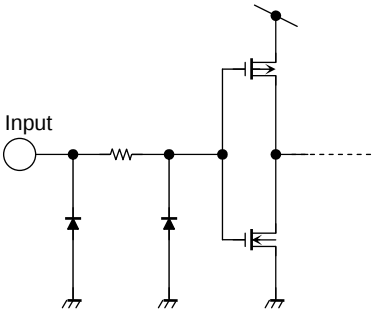
And the total C_{PD} when n pcs of flip-flop operate can be gained by the following equation:

$$C_{\text{PD (total)}} = 22 + 9 \cdot n$$

Noise Characteristics (Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			VCC (V)	Typ.	Limit	
Quiet output maximum dynamic VOL	VOLP	CL = 50 pF	5.0	0.5	0.8	V
Quiet output minimum dynamic VOL	VOLV	CL = 50 pF	5.0	-0.5	-0.8	V
Minimum high level dynamic input voltage VIH	VIHD	CL = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage VIL	VILD	CL = 50 pF	5.0	—	1.5	V

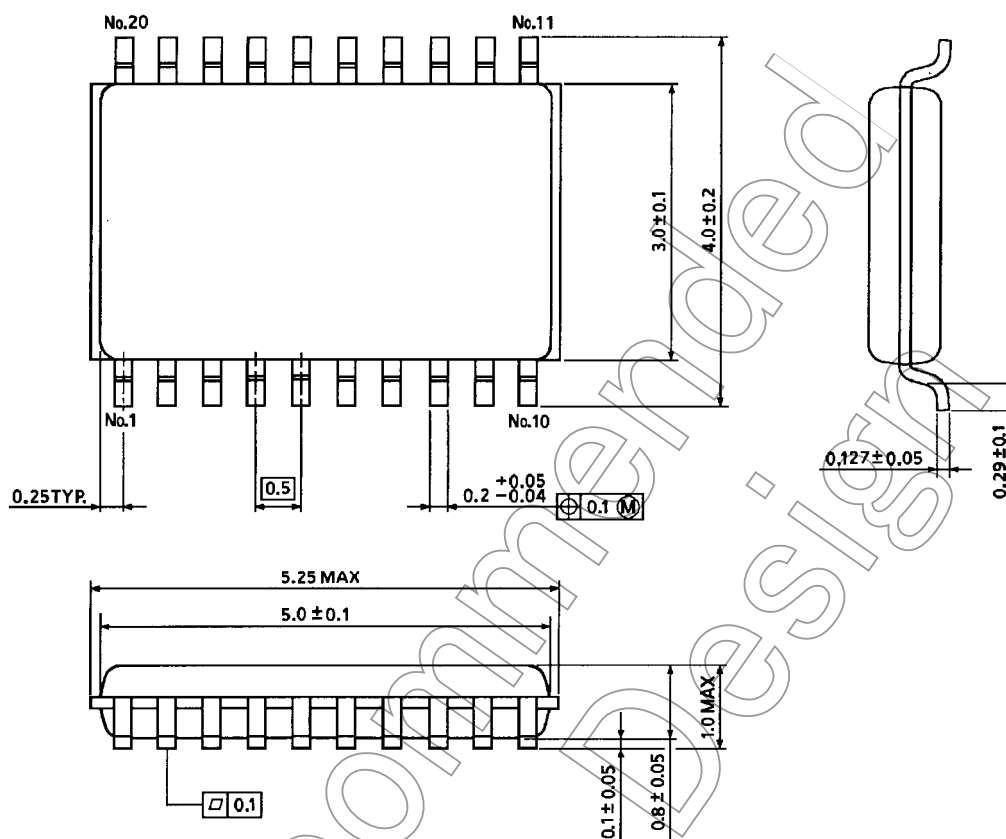
Input Equivalent Circuit



Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)

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