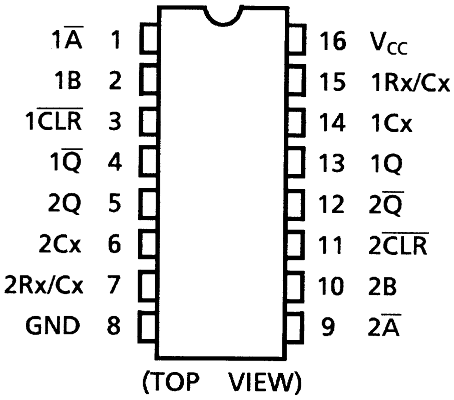
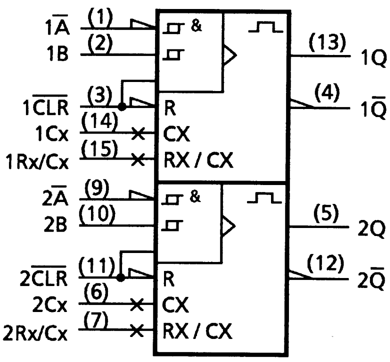
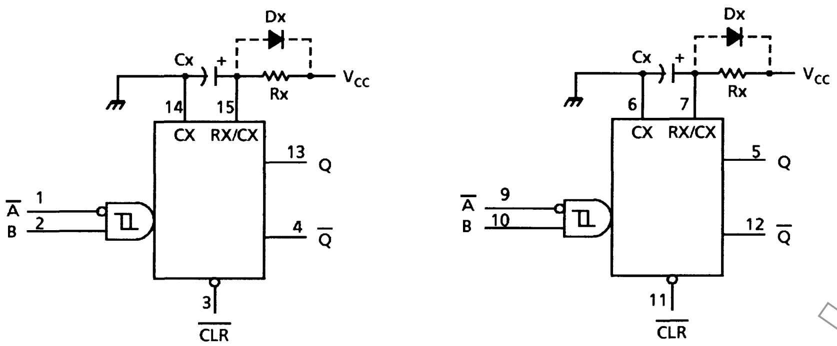
**Pin Assignment**




**IEC Logic Symbol**



## Block Diagram (Note 1)(Note 2)




Note 1: Cx, Rx, Dx are external capacitor, resistor, and diode, respectively.

Note 2: External clamping diode, Dx;

The external capacitor is charged to $V_{CC}$ level in the wait state, i.e. when no trigger is applied.
If the supply voltage is turned off, Cx is discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and $V_{CC}$ drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and $V_{CC}$ drops slowly, the in rush current is automatically limited and damage to the IC is avoided.
The maximum value of forward current through the parasitic diode is ±20 mA.
In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$t_f \geq (V_{CC} - 0.7)$ Cx/20 mA

(tf is the time between the supply voltage turn off and the supply voltage reaching 0.4 $V_{CC}$.)

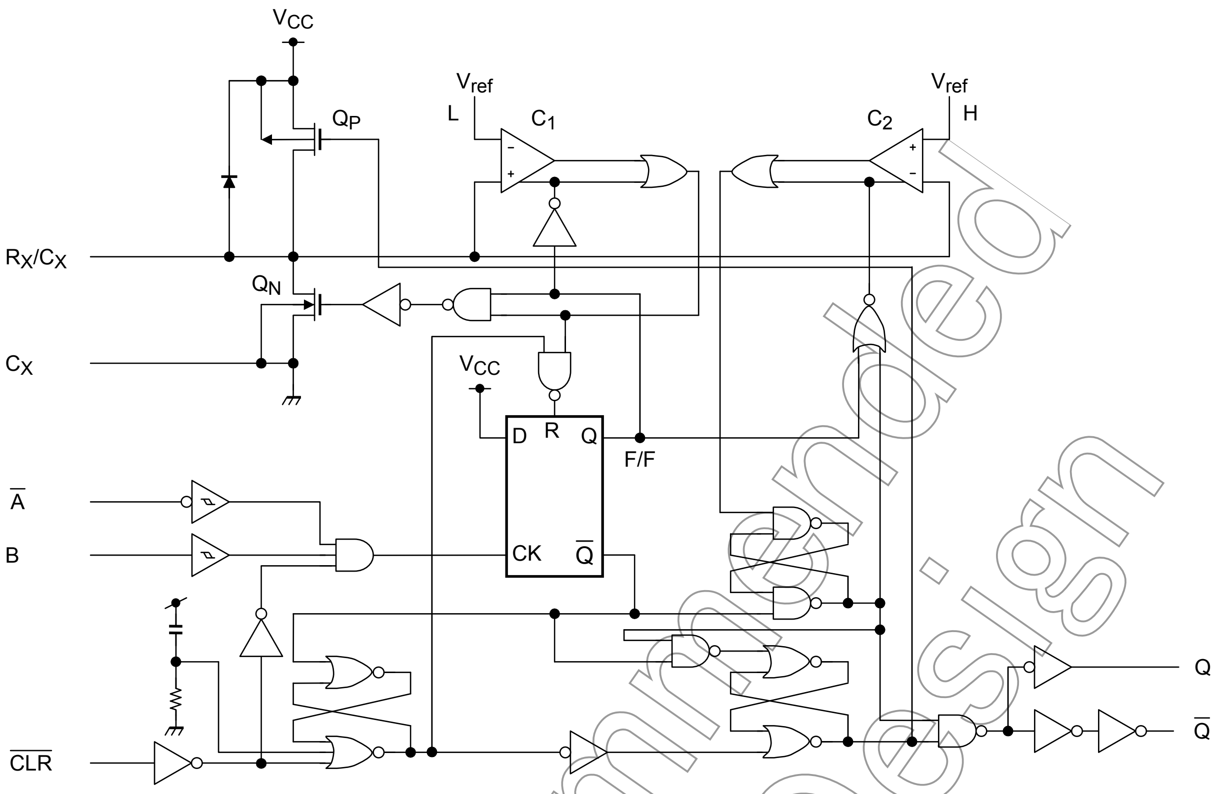
In the event a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from in rush current.

## Truth Table

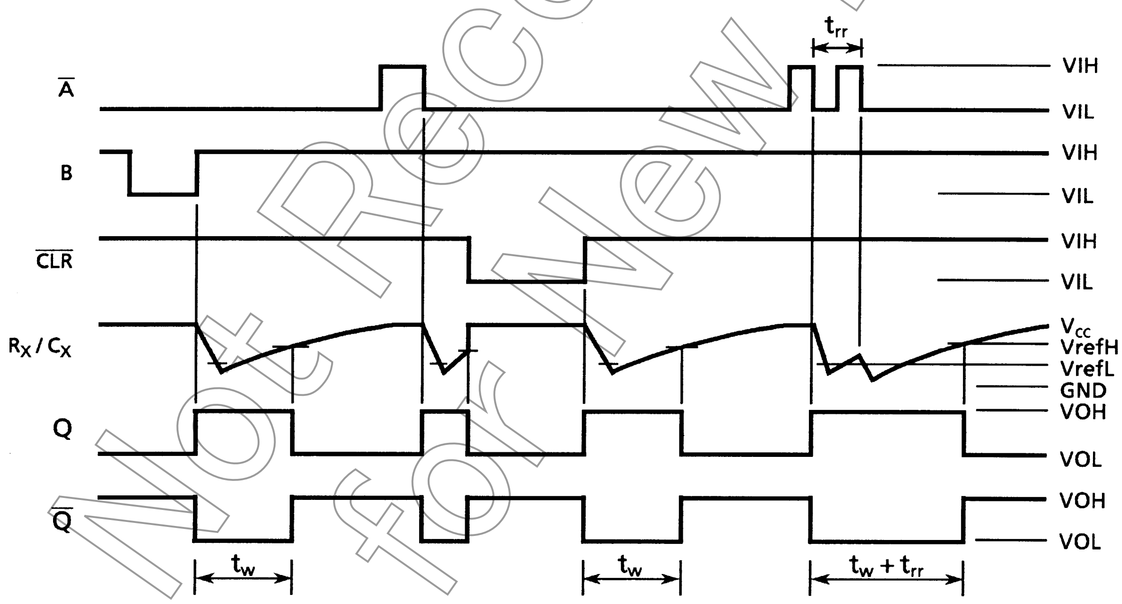
| Inputs | | | Outputs | | Function |
|---|---|---|---|---|---|
| Ā | B | CLR | Q | Q̄ | |
| ↓ | H | H | ⎍ | ⎎ | Output Enable |
| X | L | H | L | H | Inhibit |
| H | X | H | L | H | Inhibit |
| L | ↑ | H | ⎍ | ⎎ | Output Enable |
| L | H | ↑ | ⎍ | ⎎ | Output Enable |
| X | X | L | L | H | Inhibit |

X: Don't care

## System Diagram




## Timing Chart



## Functional Description

(1) Stand-by state

The external capacitor (Cx) is fully charged to $V_{CC}$ in the stand-by state. That means, before triggering, the $Q_P$ and $Q_N$ transistors which are connected to the Rx/Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is low, and the B input has a rising signal; second, where the B input is high, and the $\overline{A}$ input has a falling signal; and third, where the $\overline{A}$ input is low and the B input is high, and the $\overline{CLR}$ input has a rising signal.

After a trigger becomes effective, comparators C1 and C2 start operating, and $Q_N$ is turned on. The external capacitor discharges through $Q_N$. The voltage level at the Rx/Cx node drops. If the Rx/Cx voltage level falls to the internal reference voltage Vref L, the output of C1 becomes low. The flip-flop is then reset and $Q_N$ turns off. At that moment C1 stops but C2 continues operating.

After $Q_N$ turns off, the voltage at the Rx/Cx node starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.

Upon triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of Rx/Cx changes from falling to rising. When Rx/Cx reaches the internal reference voltage Vref H, the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the Rx/Cx node reaches Vref H, the IC returns to its MONOSTABLE state.

With large values of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, tw (OUT), is as follows:

$$t_w(OUT) = 1.0\ Cx\ Rx$$

(3) Retrigger operation

When a new trigger is applied to either input $\overline{A}$ or B while in the MONOSTABLE state, it is effective only if the IC is charging Cx. The voltage level of the Rx/Cx node then falls to Vref L level again. Therefore the Q output stays high if the next trigger comes in before the time period set by Cx and Rx.

If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2nd trigger, trr (Min.), depends on $V_{CC}$ and Cx.

(4) Reset operation

In normal operation, the $\overline{CLR}$ input is held high. If $\overline{CLR}$ is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also, $Q_P$ turns on and Cx is charged rapidly to $V_{CC}$.

This means if $\overline{CLR}$ is set low, the IC goes into a wait state.

## Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | −0.5 to 7 | V |
| DC input voltage | $V_{IN}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| DC output voltage | $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | ±20 | mA |
| Output diode current | $I_{OK}$ | ±20 | mA |
| DC output current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$/ground current | $I_{CC}$ | ±50 | mA |
| Power dissipation | $P_D$ | 180 | mW |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

## Operating Ranges (Note 1)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2 to 6 | V |
| Input voltage | $V_{IN}$ | 0 to $V_{CC}$ | V |
| Output voltage | $V_{OUT}$ | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | −40 to 85 | °C |
| Input rise and fall time ($\overline{CLR}$ only) | $t_r$, $t_f$ | 0 to 1000 ($V_{CC}$ = 2.0 V)<br>0 to 500 ($V_{CC}$ = 4.5 V)<br>0 to 400 ($V_{CC}$ = 6.0 V) | ns |
| External capacitor | Cx | No limitation (Note 2) | F |
| External resistor | Rx | ≥5 k ($V_{CC}$ = 2.0 V) (Note 2)<br>≥1 k ($V_{CC}$ ≥ 3.0 V) (Note 2) | Ω |

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Note 2: The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of TC74HC123A, and leakage due to board layout and surface resistance.

Susceptibility to externally induced noise signals may occur for Rx > 1 MΩ.

## Electrical Characteristics

### DC Characteristics

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Ta = 25°C Min | Ta = 25°C Typ. | Ta = 25°C Max | Ta = −40 to 85°C Min | Ta = −40 to 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 2.0 | 1.50 | — | — | 1.50 | — | V |
| | | | | 4.5 | 3.15 | — | — | 3.15 | — | |
| | | | | 6.0 | 4.20 | — | — | 4.20 | — | |
| Low-level input voltage | $V_{IL}$ | — | | 2.0 | — | — | 0.50 | — | 0.50 | V |
| | | | | 4.5 | — | — | 1.35 | — | 1.35 | |
| | | | | 6.0 | — | — | 1.80 | — | 1.80 | |
| High-level output voltage (Q, $\overline{Q}$) | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −20 μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | | 6.0 | 5.9 | 6.0 | — | 5.9 | — | |
| | | | $I_{OH}$ = −4 mA | 4.5 | 4.18 | 4.31 | — | 4.13 | — | |
| | | | $I_{OH}$ = −5.2 mA | 6.0 | 5.68 | 5.80 | — | 5.63 | — | |
| Low-level output voltage (Q, $\overline{Q}$) | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 6.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 4.5 | — | 0.17 | 0.26 | — | 0.33 | |
| | | | $I_{OL}$ = 5.2 mA | 6.0 | — | 0.18 | 0.26 | — | 0.33 | |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | — | ±0.1 | — | ±1.0 | μA |
| Rx/Cx terminal off-state current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | — | 4.0 | — | 40.0 | μA |
| Active-state supply current (Note) | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND, Rx/Cx = 0.5 $V_{CC}$ | | 2.0 | — | 45 | 200 | — | 260 | μA |
| | | | | 4.5 | — | 400 | 500 | — | 650 | μA |
| | | | | 6.0 | — | 0.7 | 1.0 | — | 1.3 | mA |

Note: Per circuit

## Timing Requirements (input: $t_r = t_f = 6$ ns)

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | Ta = –40 to 85°C | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | Typ. | Limit | Limit | |
| Minimum pulse width | $t_{W (L)}$ $t_{W (H)}$ | — | 2.0 | — | 75 | 95 | ns |
| | | | 4.5 | — | 15 | 19 | |
| | | | 6.0 | — | 13 | 16 | |
| Minimum clear width | $t_{W (L)}$ | — | 2.0 | — | 75 | 95 | ns |
| | | | 4.5 | — | 15 | 19 | |
| | | | 6.0 | — | 13 | 16 | |
| Minimum retrigger time | $t_{rr}$ | Rx = 1 kΩ Cx = 100 pF | 2.0 | 325 | — | — | ns |
| | | | 4.5 | 108 | — | — | |
| | | | 6.0 | 78 | — | — | |
| | | Rx = 1 kΩ Cx = 0.01 µF | 2.0 | 5.0 | — | — | µs |
| | | | 4.5 | 1.4 | — | — | |
| | | | 6.0 | 1.2 | — | — | |

## AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Output transition time | $t_{TLH}$ $t_{THL}$ | — | — | 4 | 8 | ns |
| Propagation delay time ( $\overline{A}$ , B-Q, $\overline{Q}$ ) | $t_{pLH}$ $t_{pHL}$ | — | — | 25 | 36 | ns |
| Propagation delay time ( $\overline{CLR}$ TRIGGER-Q, $\overline{Q}$ ) | $t_{pLH}$ $t_{pHL}$ | — | — | 26 | 41 | ns |
| Propagation delay time ( $\overline{CLR}$ -Q, $\overline{Q}$ ) | $t_{pLH}$ $t_{pHL}$ | — | — | 16 | 27 | ns |

## AC Characteristics ($C_L$ = 50 pF, input: $t_r = t_f$ = 6 ns)

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | Min | Typ. | Max | Min | Max | |
| Output transition time | $t_{TLH}$ $t_{THL}$ | — | 2.0 | — | 30 | 75 | — | 95 | ns |
| | | | 4.5 | — | 8 | 15 | — | 19 | |
| | | | 6.0 | — | 7 | 13 | — | 16 | |
| Propagation delay time ( $\overline{A}$ , B-Q, $\overline{Q}$ ) | $t_{pLH}$ $t_{pHL}$ | — | 2.0 | — | 102 | 210 | — | 265 | ns |
| | | | 4.5 | — | 29 | 42 | — | 53 | |
| | | | 6.0 | — | 22 | 36 | — | 45 | |
| Propagation delay time ( $\overline{CLR}$ TRIGGER-Q, $\overline{Q}$ ) | $t_{pLH}$ $t_{pHL}$ | — | 2.0 | — | 102 | 235 | — | 295 | ns |
| | | | 4.5 | — | 31 | 47 | — | 59 | |
| | | | 6.0 | — | 23 | 40 | — | 50 | |
| Propagation delay time ( $\overline{CLR}$ -Q, $\overline{Q}$ ) | $t_{pLH}$ $t_{pHL}$ | — | 2.0 | — | 68 | 160 | — | 200 | ns |
| | | | 4.5 | — | 20 | 32 | — | 40 | |
| | | | 6.0 | — | 16 | 27 | — | 34 | |
| Output pulse width | $tw_{OUT}$ | Cx = 28 pF | 2.0 | — | 700 | 2000 | — | 2500 | ns |
| | | Rx = 6 kΩ ($V_{CC}$ = 2 V) | 4.5 | — | 250 | 400 | — | 500 | |
| | | Rx = 2 kΩ ($V_{CC}$ = 4.5 V, 6 V) | 6.0 | — | 210 | 340 | — | 425 | |
| | | Cx = 0.01 μF | 2.0 | 90 | 110 | 130 | 90 | 130 | μs |
| | | Rx = 10 kΩ | 4.5 | 95 | 105 | 115 | 95 | 115 | |
| | | | 6.0 | 95 | 105 | 115 | 95 | 115 | |
| | | Cx = 0.1 μF | 2.0 | 0.9 | 1.0 | 1.2 | 0.9 | 1.2 | ms |
| | | Rx = 10 kΩ | 4.5 | 0.9 | 1.0 | 1.1 | 0.9 | 1.1 | |
| | | | 6.0 | 0.9 | 1.0 | 1.1 | 0.9 | 1.1 | |
| Output pulse width error between circuits (in same package ) | $\Delta tw_{OUT}$ | — | | — | ±1 | — | — | — | % |
| Input capacitance | $C_{IN}$ | — | | — | 5 | 10 | — | 10 | pF |
| Power dissipation capacitance | $C_{PD}$ (Note) | — | | — | 162 | — | — | — | pF |

Note: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

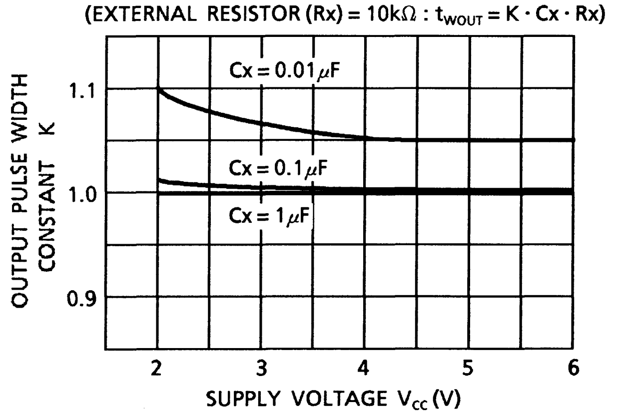
Average operating current can be obtained by the equation:

$I_{CC}$ (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot$ duty/100 + $I_{CC}$/2 (per circuit)

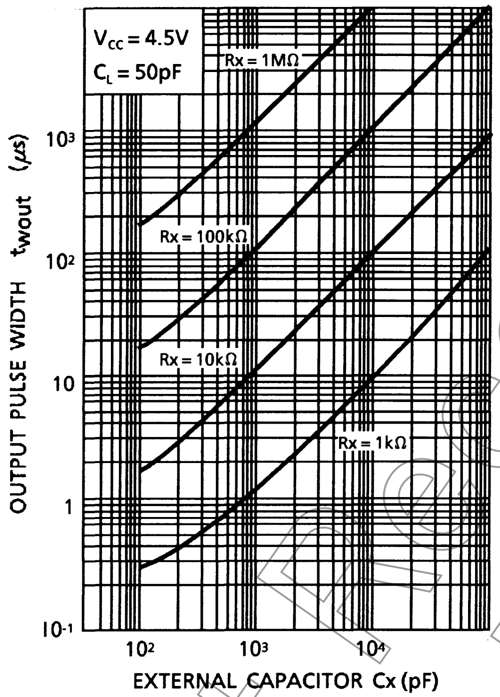
($I_{CC}'$: active supply current)

(duty. %)

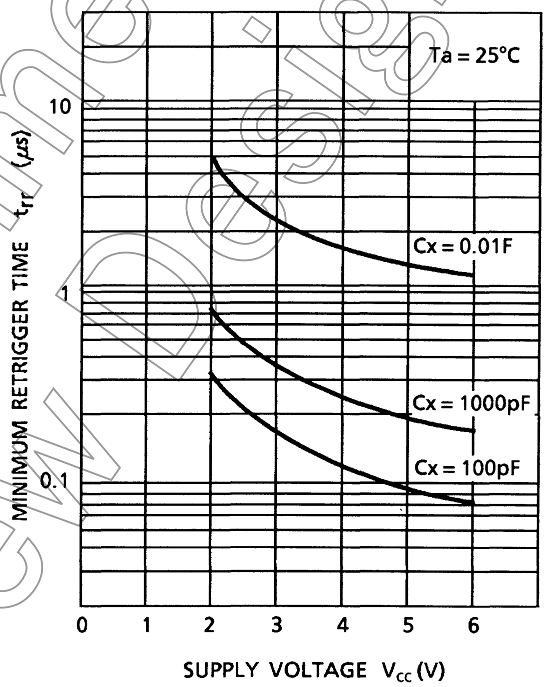
Output Pulse Width Constant K – Supply Voltage (typical)




tWOUT – Cx Characteristics (typ.)



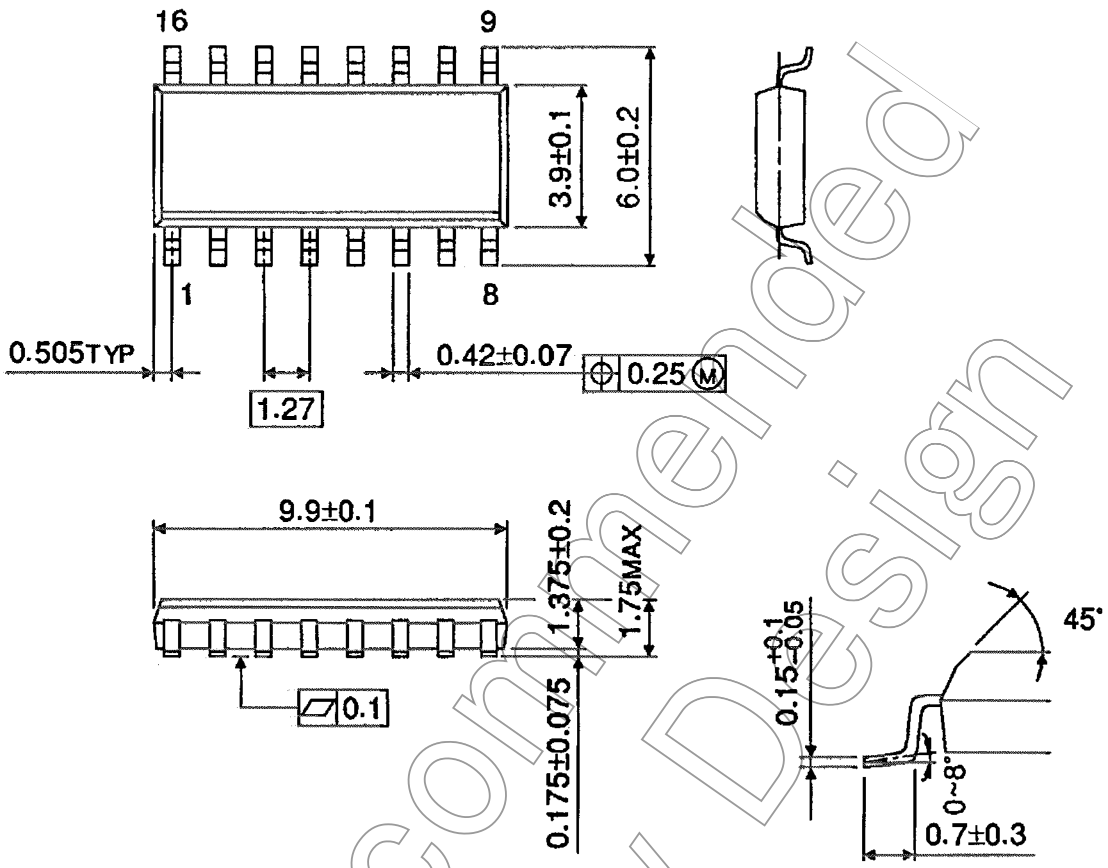

trr – VCC Characteristics (typ.)



## Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm




Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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