

1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Input Voltage	6.5V
Power Dissipation.....	Internally Limited (Note 7)
Operating Temperature	-40°C < T _J < 125°C
Storage Temperature.....	-65°C to +150°C
Maximum Voltage On Any Pin.....	V _{IN} + 0.3V to -0.3V

***Notice:** Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability

ELECTRICAL CHARACTERISTICS

V _{IN} = V _R + 1V, I _L = 100 µA, C _L = 1.0µF, $\overline{\text{SHDN}} > V_{IH}$, T _A = 25°C, unless otherwise noted. Boldface type specifications apply for junction temperatures of - 40°C to +125°C.						
Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Input Operating Voltage	V _{IN}	2.7	—	6.0	V	Note 1
Maximum Output Current	I _{OUTMAX}	80	—	—	mA	
Output Voltage	V _{OUT}	V_R - 2.5%	V _R ±0.5%	V_R + 2.5%	V	Note 2
V _{OUT} Temperature Coefficient	TCV _{OUT}	—	40	—	ppm/°C	Note 3
Line Regulation	(ΔV _{OUT} /ΔV _{IN})/V _R	—	0.01	0.2	%/V	(V _R + 1V) < V _{IN} < 6V
Load Regulation (Note 4)	ΔV _{OUT} /V _R	—	0.23	1	%	I _L = 0.1 mA to I _{OUTMAX}
Dropout Voltage (Note 5)	V _{IN} - V _{OUT}	—	2 100 150	— 200 300	mV	I _L = 100 µA I _L = 50 mA I _L = 80 mA
Supply Current	I _{IN}	—	53	90	µA	$\overline{\text{SHDN}} = V_{IH}$, I _L = 0
Shutdown Supply Current	I _{INSD}	—	0.05	0.5	µA	$\overline{\text{SHDN}} = 0V$
Power Supply Rejection Ratio	PSRR	—	58	—	dB	f = 1 kHz, I _L = 50 mA
Wake-Up Time (from Shutdown mode)	t _{WK}	—	10	—	µs	V _{IN} = 5V, I _L = 60 mA, C _{IN} = 1 µF, C _{OUT} = 1 µF, f = 100 Hz
Settling Time (from Shutdown Mode)	t _S	—	32	—	µs	V _{IN} = 5V, I _L = 60 mA, C _{IN} = 1 µF, C _{OUT} = 1 µF, f = 100 Hz
Output Short Circuit Current	I _{OUTSC}	—	120	—	mA	V _{OUT} = 0V
Thermal Regulation	V _{OUT} /P _D	—	0.04	—	V/W	Notes 6, 7
Thermal Shutdown Die Temperature	T _{SD}	—	160	—	°C	
Thermal Shutdown Hysteresis	ΔT _{SD}	—	10	—	°C	
Output Noise	eN	—	800	—	nV/√Hz	f = 10 kHz
SHDN Input High Threshold	V _{IH}	60	—	—	%V _{IN}	V _{IN} = 2.7V to 6.0V
SHDN Input Low Threshold	V _{IL}	—	—	15	%V _{IN}	V _{IN} = 2.7V to 6.0V

Note 1: The minimum V_{IN} has to meet two conditions: V_{IN} ≥ 2.7V and V_{IN} ≥ (V_R + 2.5%) + V_{DROPOUT}.
Note 2: V_R is the regulator voltage setting. For example: V_R = 1.8V, 2.7V, 2.8V, 3.0V.

$$3: TCV_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) \times 10^6}{V_{OUT} \times \Delta T}$$

- 4:** Regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the Thermal Regulation specification.
- 5:** Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value at a 1V differential.
- 6:** Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{max} at V_{IN} = 6V for t = 10 msec.
- 7:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see **Section 5.0 "Thermal Considerations"** of this data sheet for more details.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

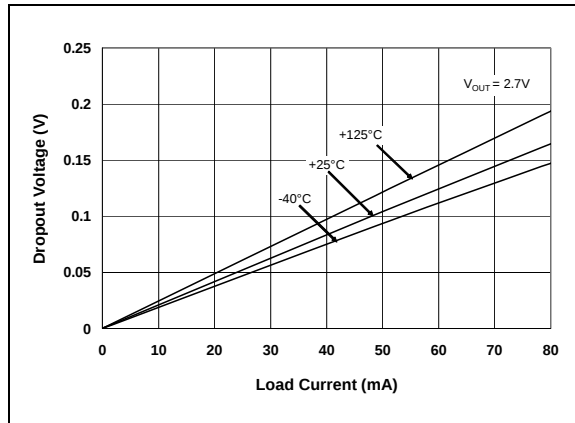


FIGURE 2-1: Dropout Voltage vs. Output Current.

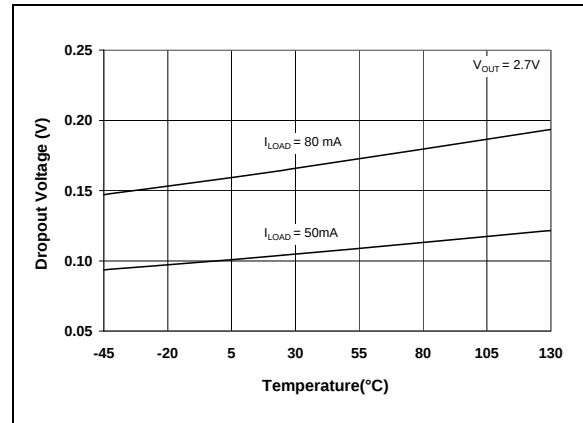


FIGURE 2-4: Dropout Voltage vs. Temperature.

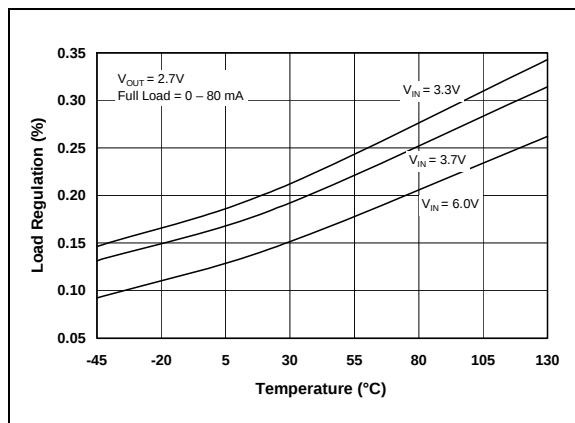


FIGURE 2-2: Load Regulation vs. Temperature.

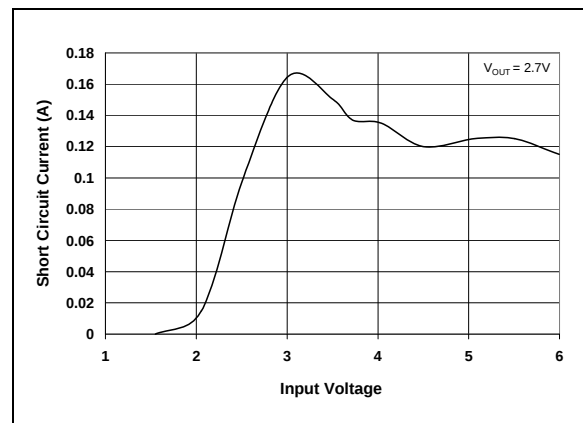


FIGURE 2-5: Short Circuit Current vs. Input Voltage.

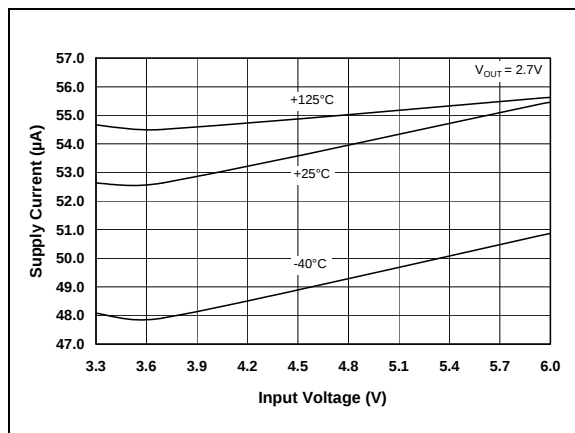


FIGURE 2-3: Supply Current vs. Input Voltage.

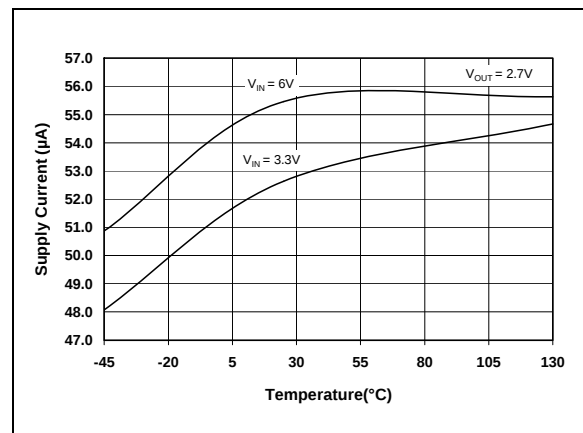


FIGURE 2-6: Supply Current vs. Temperature.

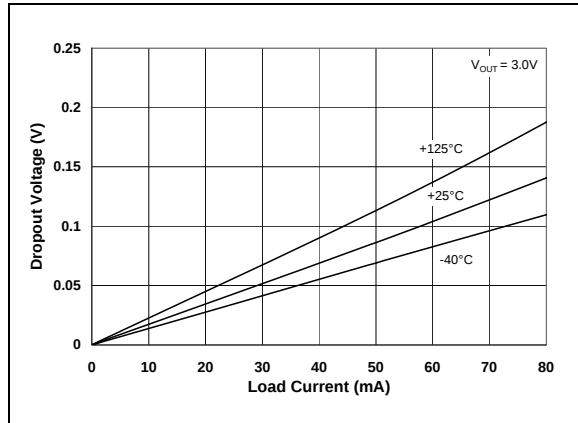


FIGURE 2-7: Dropout Voltage vs. Output Current.

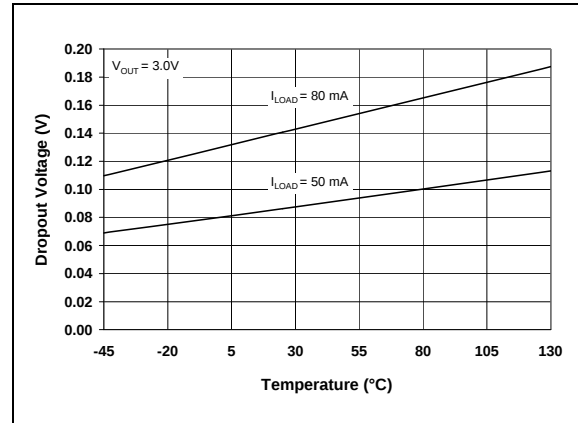


FIGURE 2-10: Dropout Voltage vs. Temperature.

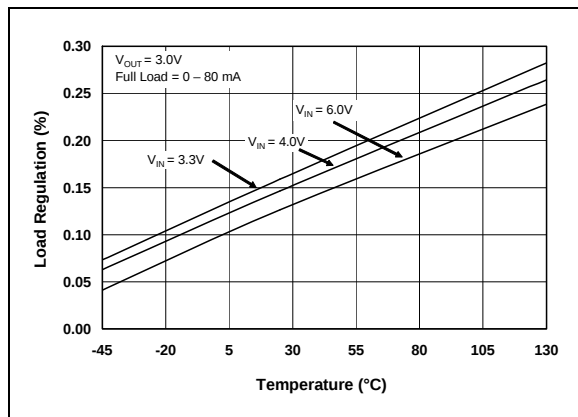


FIGURE 2-8: Load Regulation vs. Temperature.

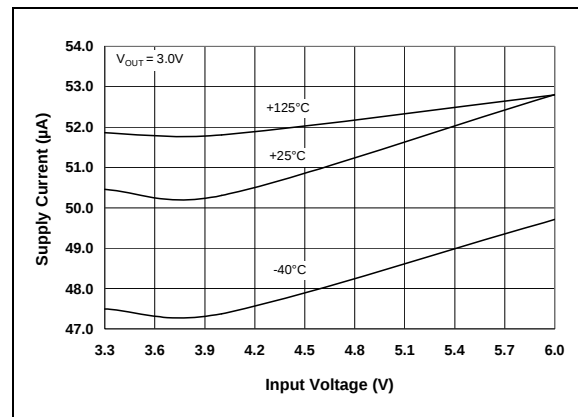


FIGURE 2-11: Supply Current vs. Input Voltage

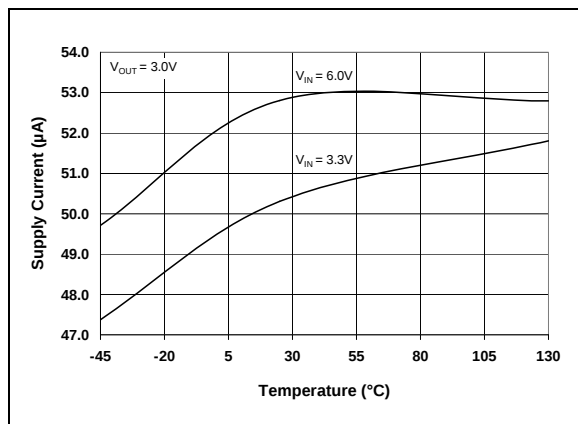


FIGURE 2-9: Supply Current vs. Temperature.

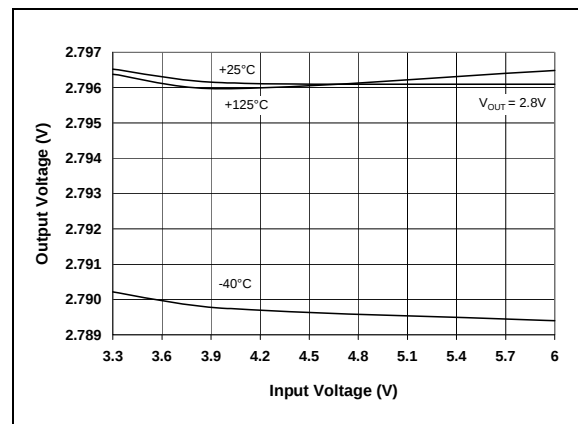


FIGURE 2-12: Output Voltage vs. Supply Voltage.

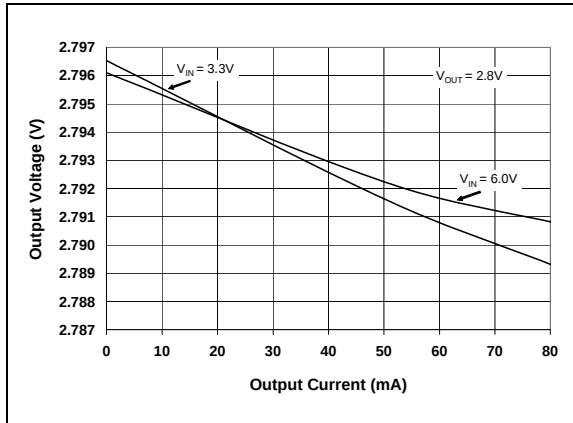


FIGURE 2-13: Output Voltage vs. Output Current.

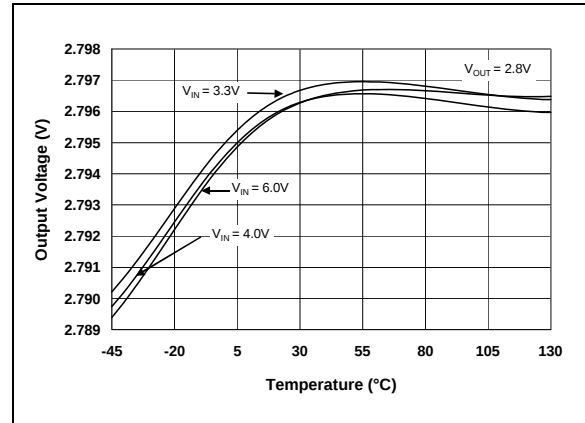


FIGURE 2-16: Output Voltage vs. Temperature.

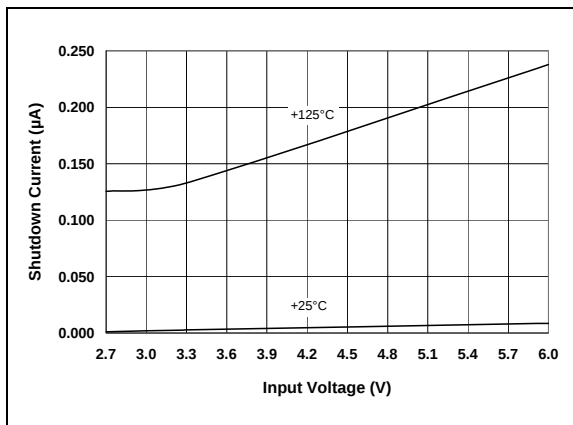


FIGURE 2-14: Shutdown Current vs. Input Voltage.

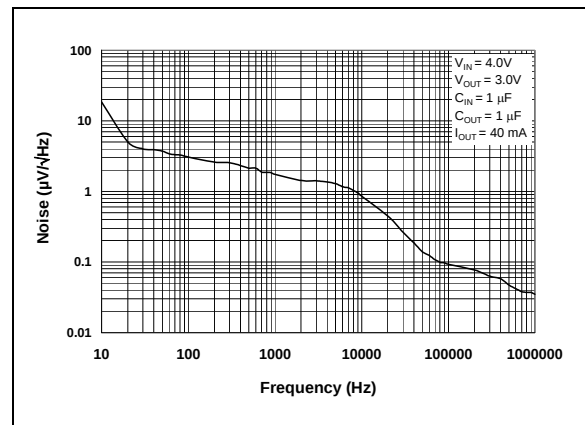


FIGURE 2-17: Output Noise vs. Frequency.

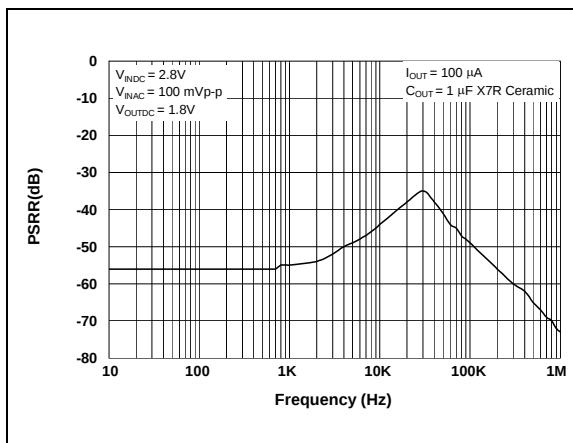


FIGURE 2-15: Power Supply Rejection Ratio vs. Frequency.

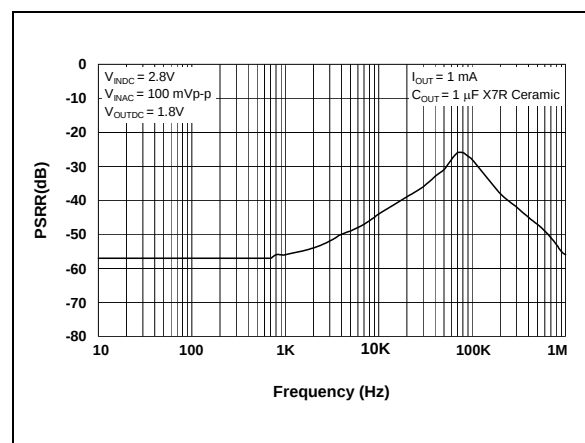


FIGURE 2-18: Power Supply Rejection Ratio vs. Frequency.

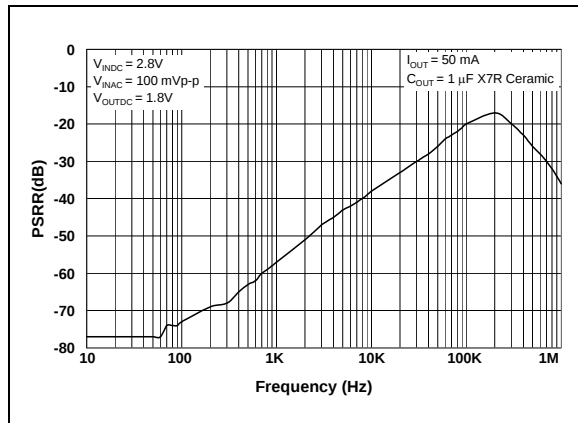


FIGURE 2-19: Power Supply Rejection Ratio vs. Frequency.

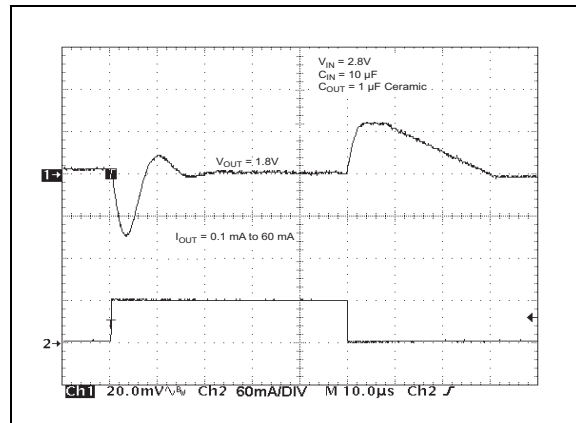


FIGURE 2-22: Load Transient Response.

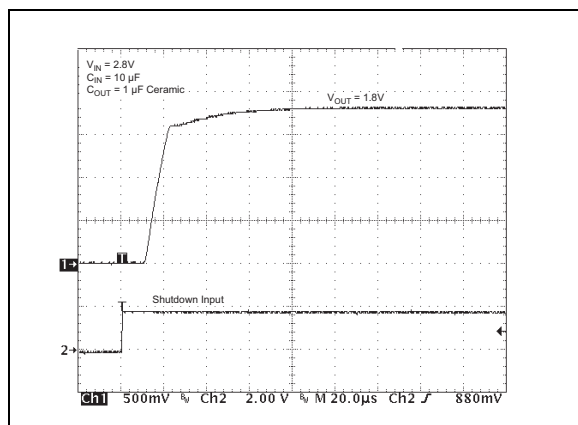


FIGURE 2-20: Wake-Up Response.

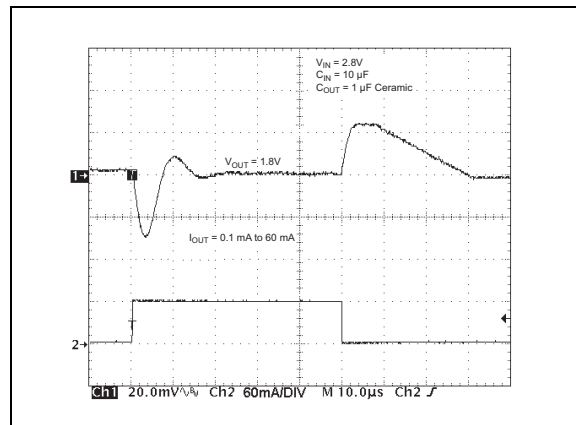


FIGURE 2-23: Load Transient Response.

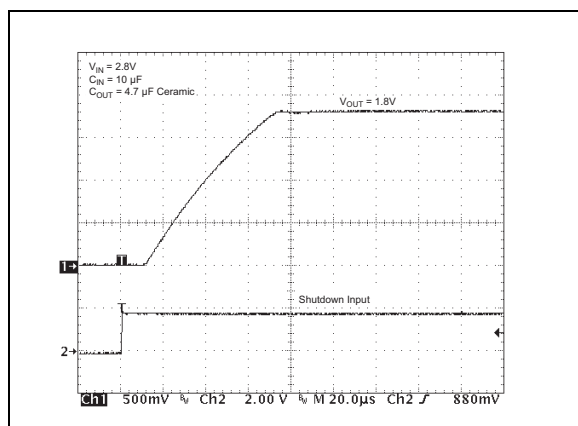


FIGURE 2-21: Wake-Up Response.

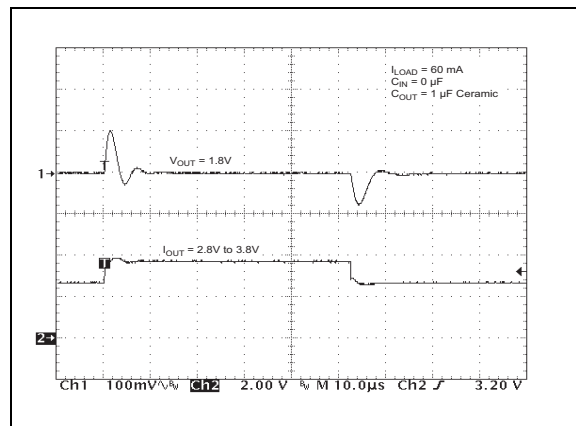


FIGURE 2-24: Line Transient Response.

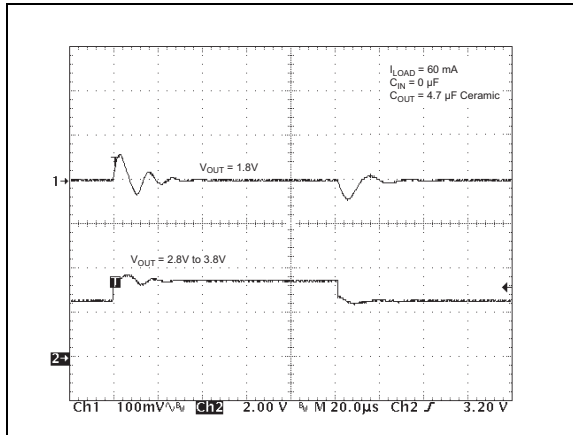


FIGURE 2-25: Line Transient Response.

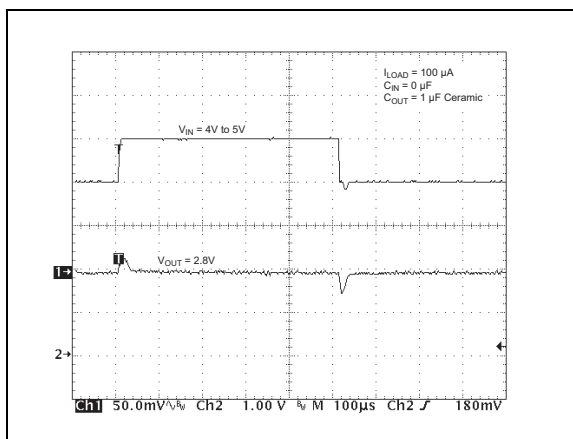


FIGURE 2-26: Line Transient Response.

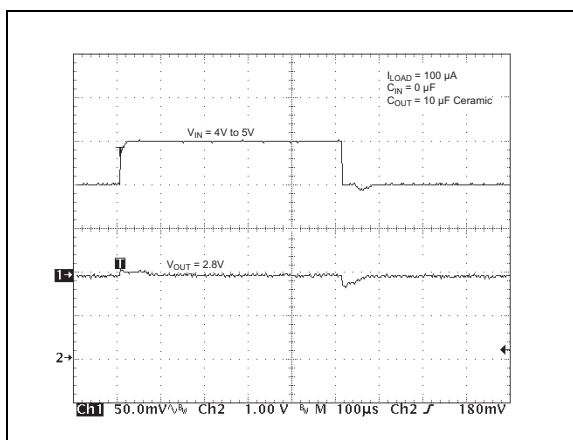


FIGURE 2-27: Line Transient Response.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

5-Pin SC-70	Pin No. 5-Pin SOT-23	Name	Function
1	3	$\overline{\text{SHDN}}$	Shutdown control input
2	4	NC	No connect
3	2	GND	Ground terminal
4	5	V_{OUT}	Regulated voltage output
5	1	V_{IN}	Unregulated supply input

3.1 Shutdown Control Input ($\overline{\text{SHDN}}$)

The regulator is fully enabled when a logic-high is applied to $\overline{\text{SHDN}}$. The regulator enters shutdown when a logic-low is applied to this input. During shutdown, the output voltage falls to zero and the supply current is reduced to 0.05 μA (typ.)

3.2 Ground Terminal (GND)

For best performance, it is recommended that the ground pin be tied to a ground plane.

3.3 Regulated Voltage Output (V_{OUT})

Bypass the regulated voltage output to GND with a minimum capacitance of 1 μF . A ceramic bypass capacitor is recommended for best performance.

3.4 Unregulated Supply Input (V_{IN})

The minimum V_{IN} has to meet two conditions in order to ensure that the output maintains regulation: $V_{\text{IN}} \geq 2.7\text{V}$ and $V_{\text{IN}} \geq [(V_{\text{R}} + 2.5\%) + V_{\text{DROPOUT}}]$. The maximum V_{IN} should be less than or equal to 6V. Power dissipation may limit V_{IN} to a lower potential in order to maintain a junction temperature below 125°C. Refer to **Section 5.0 “Thermal Considerations”**, for determining junction temperature.

It is recommended that V_{IN} be bypassed to GND with a ceramic capacitor.

4.0 DETAILED DESCRIPTION

The TC1016 is a precision, fixed-output, linear voltage regulator. The internal linear pass element is a P-channel MOSFET. As with all P-channel CMOS LDOs, there is a body drain diode, with the cathode connected to V_{IN} and the anode connected to V_{OUT} (Figure 4-1).

As shown in Figure 4-1, the output voltage of the LDO is sensed and divided down internally to reduce external component count. The internal error amplifier has a fixed, band gap reference on the inverting input, with the sensed output voltage on the non-inverting input. The error amplifier output will pull the gate voltage down until the inputs of the error amplifier are equal in order to regulate the output voltage.

By sensing the current in the P-channel MOSFET, the maximum current delivered to the load is limited to a typical value of 120 mA, preventing excessive current from damaging the Printed Circuit Board (PCB) in the event of a shorted or faulted load.

An internal thermal sensing device is used to monitor the junction temperature of the LDO. When the sensed temperature is over the set threshold of 160°C (typ.), the P-channel MOSFET is turned off. When the MOSFET is off, the power dissipation internal to the device is almost zero. The device cools until the junction temperature is approximately 150°C and the

MOSFET is turned on. If the internal power dissipation is still high enough for the junction to rise to 160°C, it will again shut off and cool. The maximum operating junction temperature of the device is 125°C. Steady-state operation at or near the 160°C overtemperature point can lead to permanent damage of the device.

The output voltage (V_{OUT}) remains stable over the entire input operating voltage range (2.7V to 6.0V), as well as the entire load range (0 mA to 80 mA). The output voltage is sensed through an internal resistor divider and compared with a precision internal voltage reference. Several fixed-output voltages are available by changing the value of the internal resistor divider.

Figure 4-2 shows a typical application circuit. The regulator is enabled anytime the shutdown input pin is at or above V_{IH} , and shutdown (disabled) anytime the shutdown input pin is below V_{IL} . For applications where the SHDN feature is not used, tie the SHDN pin directly to the input supply voltage source. While in shutdown, the supply current decreases to 0.05 μ A (typ.) and the P-channel MOSFET is turned off.

As shown in Figure 4-2, batteries have internal source impedance. An input capacitor is used to lower the input impedance of the LDO. In some applications, high input impedance can cause the LDO to become unstable. Adding more input capacitance can compensate for this.

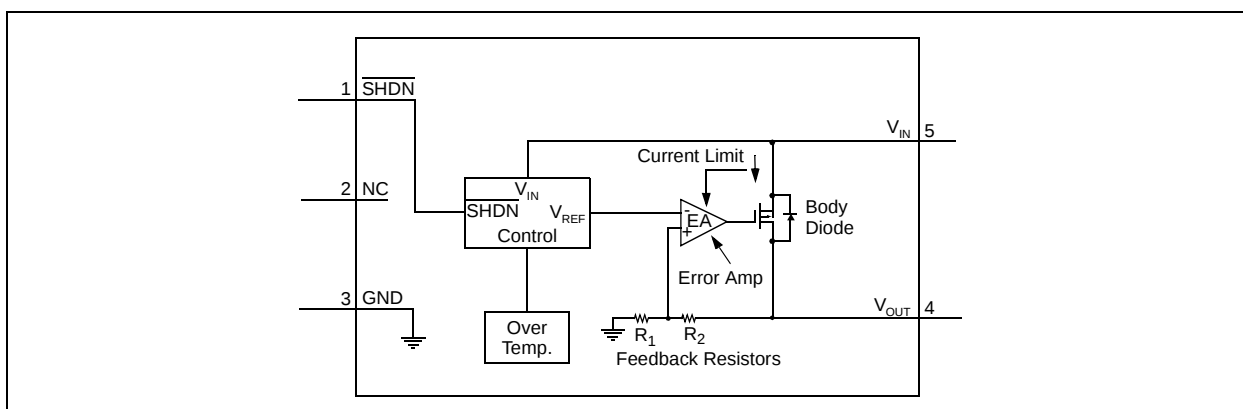


FIGURE 4-1: TC1016 Block Diagram.

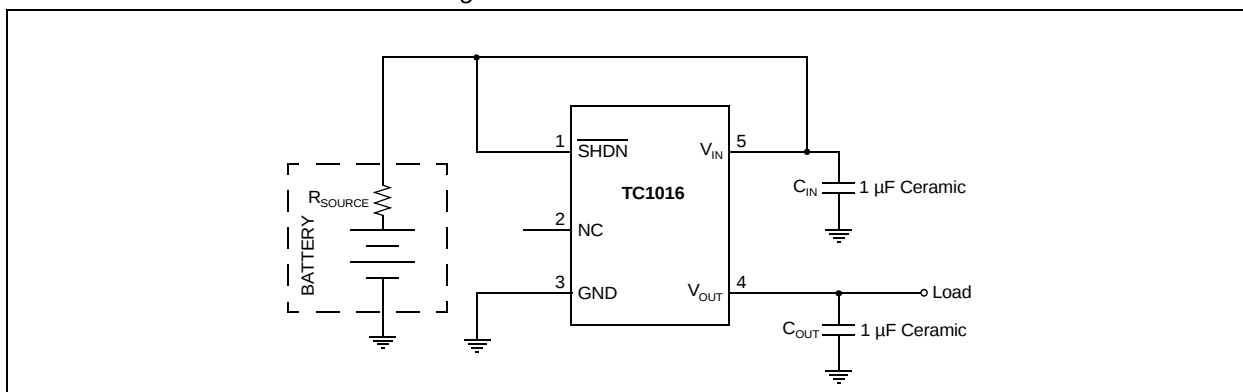


FIGURE 4-2: Typical Application Circuit.

4.1 Input Capacitor

Low input source impedance is necessary for the LDO to operate properly. When operating from batteries, or in applications with long lead length (> 10") between the input source and the LDO, some input capacitance is required. A minimum of 0.1 μF is recommended for most applications and the capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will help reduce the input impedance and further reduce any high-frequency noise on the input and output of the LDO.

4.2 Output Capacitor

A minimum output capacitance of 1 μF for the TC1016 is required for stability. The ESR requirements on the output capacitor are between 0 and 2 ohms. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 μF X5R 0805 capacitor has an ESR of 50 milli-ohms. Larger output capacitors can be used with the TC1016 to improve dynamic behavior and input ripple rejection performance.

Ceramic, aluminum electrolytic or tantalum capacitor types can be used. Since many aluminum electrolytic capacitors freeze at approximately -30°C , ceramic or solid tantalums are recommended for applications operating below -25°C . When operating from sources other than batteries, supply noise rejection and transient response can be improved by increasing the value of the input and output capacitors, and by employing passive filtering techniques.

4.3 Turn-On Response

The turn on response is defined as two separate response categories, Wake-up Time (t_{WK}) and Settling Time (t_{S}).

The TC1016 has a fast t_{WK} (10 μsec , typ.) when released from shutdown. Figure 4-3 provides the TC1016's t_{WK} . The t_{WK} is defined as the time it takes for the output to rise to 2% of the V_{OUT} value after being released from shutdown.

The total turn-on response is defined as the t_{S} (see Figure 4-3). The t_{S} (inclusive with t_{WK}) is defined as the condition when the output is within 98% of its fully enabled value (42 μsec , typ.) when released from shutdown. The settling time of the output voltage is dependent on load conditions and output capacitance on V_{OUT} (RC response).

Table 4-1 demonstrates the typical turn-on response timing for different input voltage power-up frequencies: $V_{\text{OUT}} = 2.8\text{V}$, $V_{\text{IN}} = 5.0\text{V}$, $I_{\text{OUT}} = 60\text{ mA}$ and $C_{\text{OUT}} = 1\text{ }\mu\text{F}$.

TABLE 4-1: TYPICAL TURN-ON RESPONSE TIMING

Frequency	Typical (t_{WK})	Typical (t_{S})
1000 Hz	5.3 μsec	14 μsec
500 Hz	5.9 μsec	16 μsec
100 Hz	9.8 μsec	32 μsec
50 Hz	14.5 μsec	52 μsec
10 Hz	17.2 μsec	77 μsec

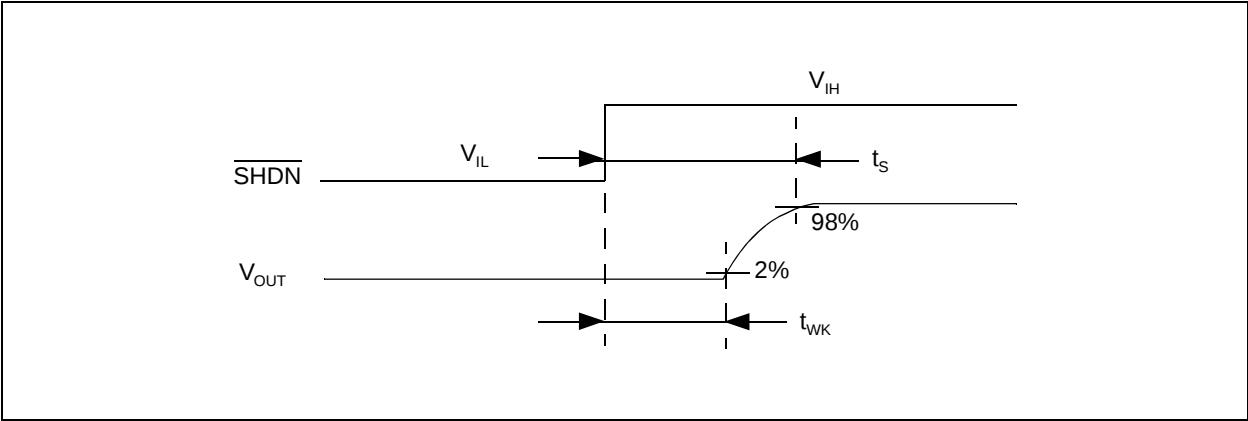


FIGURE 4-3: Wake-Up Time from Shutdown.

5.0 THERMAL CONSIDERATIONS

5.1 Thermal Shutdown

Integrated thermal-protection circuitry shuts the regulator off when die temperature exceeds approximately 160°C. The regulator remains off until the die temperature drops to approximately 150°C.

5.2 Power Dissipation

The TC1016 is available in the SC-70 package. The thermal resistance for the SC-70 package is approximately 450°C/W when the copper area used in the PCB layout is similar to the JEDEC J51-7 high thermal conductivity or Semi G42-88 standards. For applications with larger or thicker copper areas, the thermal resistance can be lowered. See AN792 "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application" (DS00792), for a method to determine the thermal resistance for a particular application.

The TC1016 power dissipation capability is dependant upon several variables: input voltage, output voltage, load current, ambient temperature and maximum junction temperature. The absolute maximum steady-state junction temperature is rated at 125°C. The power dissipation within the device is equal to:

EQUATION 5-1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD} + V_{IN} \times I_{GND}$$

The $V_{IN} \times I_{GND}$ term is typically very small when compared to the $(V_{IN} - V_{OUT}) \times I_{LOAD}$ term simplifying the power dissipation within the LDO to be:

EQUATION 5-2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

To determine the maximum power dissipation capability, the following equation is used:

EQUATION 5-3:

$$P_{D_{MAX}} = \frac{(T_{J_{MAX}} - T_{A_{MAX}})}{R\theta_{JA}}$$

Where:

$T_{J_{MAX}}$ = maximum junction temperature allowed

$T_{A_{MAX}}$ = the maximum ambient temperature allowed

$R\theta_{JA}$ = the thermal resistance from junction-to-air

Given the following example:

$$V_{IN} = 3.0V \text{ to } 4.1V$$

$$V_{OUT} = 2.8V \pm 2.5\%$$

$$I_{LOAD} = 60 \text{ mA (output current)}$$

$$T_{A_{MAX}} = 55^\circ\text{C (max. ambient temp.)}$$

Find:

1. Internal power dissipation:

$$\begin{aligned} P_{D_{MAX}} &= (V_{IN_{MAX}} - V_{OUT_{MIN}}) \times I_{LOAD} \\ &= (4.1V - 2.8 \times (0.975)) \times 60\text{mA} \\ &= 82.2\text{mW} \end{aligned}$$

2. Junction temperature:

$$\begin{aligned} T_{J_{MAX}} &= P_{D_{MAX}} \times R\theta_{JA} \\ &= 82.2\text{mWatts} \times 450^\circ\text{C/W} + T_{A_{MAX}} \\ &= 37^\circ\text{C} + 55^\circ\text{C} \\ &= 92^\circ\text{C} \end{aligned}$$

3. Maximum allowable dissipation:

$$\begin{aligned} P_D &= \frac{T_{J_{MAX}} - T_{A_{MAX}}}{R\theta_{JA}} \\ &= \frac{125^\circ\text{C} - 55^\circ\text{C}}{450^\circ\text{C/W}} \\ &= 155\text{mW} \end{aligned}$$

In this example, the TC1016 dissipates approximately 82.2 mW and the junction temperature is raised 37°C over the 55°C ambient to 92°C. The absolute maximum power dissipation is 155 mW when given a maximum ambient temperature of 55°C.

Input voltage, output voltage or load current limits can also be determined by substituting known values in Equation 5-2 and Equation 5-3.

5.3 Layout Considerations

The primary path for heat conduction out of the SC-70 package is through the package leads. Using heavy, wide traces at the pads of the device will facilitate the removal of heat within the package, thus lowering the thermal resistance $R\theta_{JA}$. By lowering the thermal resistance, the maximum internal power dissipation capability of the package is increased.

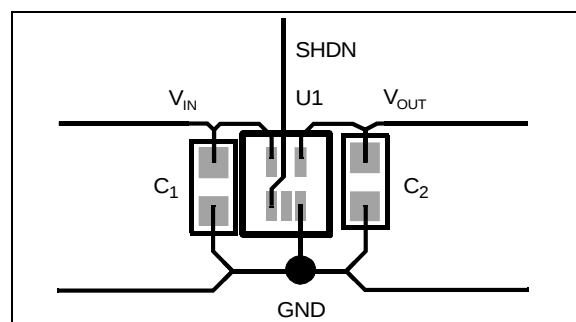
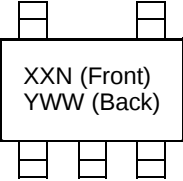


FIGURE 5-1: Suggested layout

6.0 PACKAGE INFORMATION

6.1 Package Marking Information

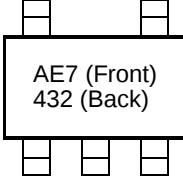
5-Lead SC-70



XXN (Front)
YWW (Back)

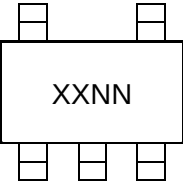
Part Number	Code
TC1016 – 1.8VLT	AE
TC1016 – 1.85VLT	AW
TC1016 – 2.6VLT	AF
TC1016 – 2.7VLT	AG
TC1016 – 2.8VLT	AH
TC1016 – 2.85VLT	AJ
TC1016 – 2.9VLT	AK
TC1016 – 3.0VLT	AL
TC1016 – 3.3VLT	AM
TC1016 – 4.0VLT	AP

Example:



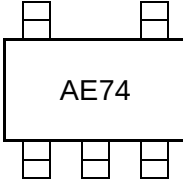
AE7 (Front)
432 (Back)

5-Lead SC-70



XXNN

Example:



AE74

Legend:

XX...X Customer-specific information*

Y Year code (last digit of calendar year)

YY Year code (last 2 digits of calendar year)

WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

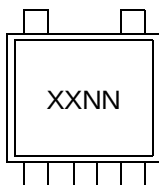
(e3) Pb-free JEDEC designator for Matte Tin (Sn)

* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

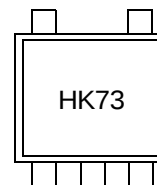
6.1 Package Marking Information (Continued)

5-Lead SOT-23



Part Number	Code
TC1016 – 1.8VCT	HK
TC1016 – 1.85VCT	HW
TC1016 – 2.6VCT	HL
TC1016 – 2.7VCT	HM
TC1016 – 2.8VCT	HP
TC1016 – 2.85VCT	HQ
TC1016 – 2.9VCT	HR
TC1016 – 3.0VCT	HS
TC1016 – 3.3VCT	HT
TC1016 – 4.0VCT	HU

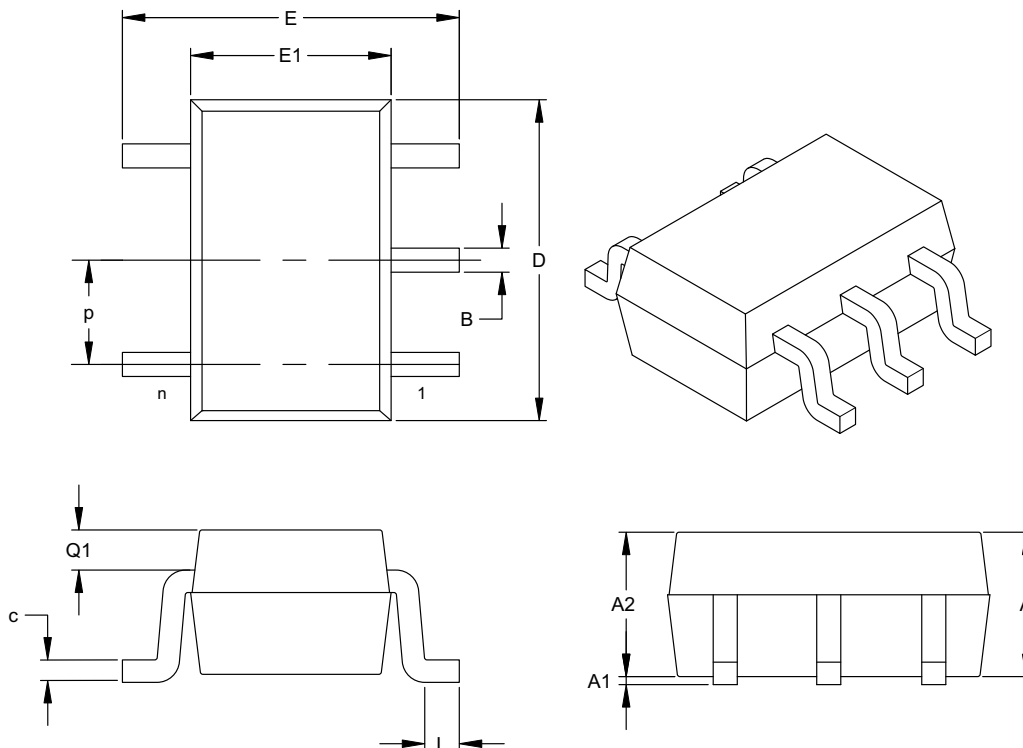
Example



TC1016

5-Lead Plastic Small Outline Transistor (LT) (SC-70)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	5			5		
Pitch	p	.026 (BSC)			0.65 (BSC)		
Overall Height	A	.031		.043	0.80		1.10
Molded Package Thickness	A2	.031		.039	0.80		1.00
Standoff	A1	.000		.004	0.00		0.10
Overall Width	E	.071		.094	1.80		2.40
Molded Package Width	E1	.045		.053	1.15		1.35
Overall Length	D	.071		.087	1.80		2.20
Foot Length	L	.004		.012	0.10		0.30
Top of Molded Pkg to Lead Shoulder	Q1	.004		.016	0.10		0.40
Lead Thickness	c	.004		.007	0.10		0.18
Lead Width	B	.006		.012	0.15		0.30

*Controlling Parameter

Notes:

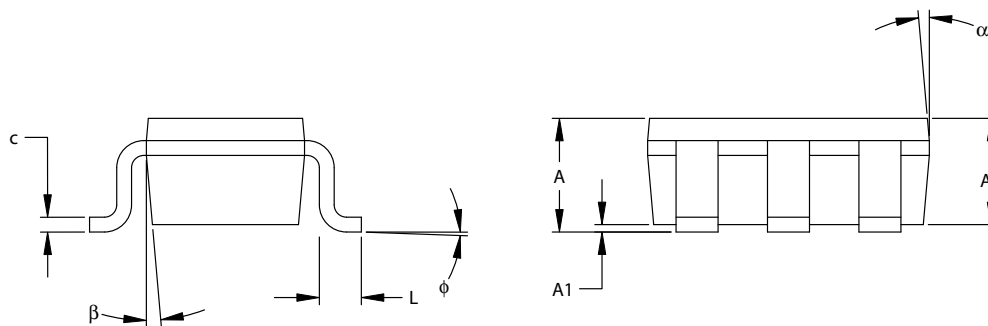
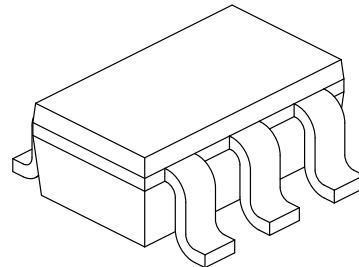
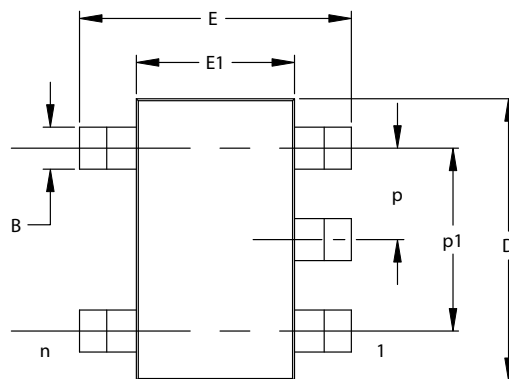
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (EIAJ) Standard: SC-70

Drawing No. C04-061

5-Lead Plastic Small Outline Transistor (OT) (SOT-23)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	5			5		
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	phi	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	alpha	0	5	10	0	5	10
Mold Draft Angle Bottom	beta	0	5	10	0	5	10

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

EIAJ Equivalent: SC-74A

Drawing No. C04-091

TC1016

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (December 2012)

- Added a note to each package outline drawing.

Revision B (March 2005)

- Updated **Section 6.0 “Package Information”** to include old and new packaging examples, as well as replaced SC-70 package diagram with up-to-date version. Added additional voltage options
- Added SOT-23 package and voltage options.
- Applied new template and rearranged sections to be consistent with current documentation.

.Revision A (October 2001)

- Original Release of this Document.

TC1016

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X.XX</u>	<u>X</u>	<u>XXXX</u>
Device	Voltage Options	Temperature Range	Package
Device:	TC1016: 80 mA Tiny CMOS LDO with Shutdown		
Voltage Options*: (Standard)	1.8V 1.85V 2.6V 2.7V 2.8V 2.85V 2.9V 3.0V 3.3V 4.0V		
	* Other voltage options available. Please contact your local Microchip sales office for details.		
Temperature Range:	V = -40°C to +125°C		
Packages:	LTTR = 5-pin SC-70 (Tape and Reel) CTTR = 5-pin SOT-23 (Tape and Reel)		
Examples: a) TC1016-1.8VCTTR: 80 mA Tiny CMOS LDO with Shutdown, SOT-23 Package. a) TC1016-1.8VLTTR: 80 mA Tiny CMOS LDO with Shutdown, SC-70 Package. b) TC1016-1.85VCTTR: 80 mA Tiny CMOS LDO with Shutdown, SOT-23 Package. c) TC1016-1.85VLTTR: 80 mA Tiny CMOS LDO with Shutdown, SC-70 Package. d) TC1016-2.6VCTTR: 80 mA Tiny CMOS LDO with Shutdown, SOT-23 Package. e) TC1016-2.6VLTTR: 80 mA Tiny CMOS LDO with Shutdown, SC-70 Package. f) TC1016-2.7VCTTR: 80 mA Tiny CMOS LDO with Shutdown, SOT-23 Package. g) TC1016-2.7VLTTR: 80 mA Tiny CMOS LDO with Shutdown, SC-70 Package. h) TC1016-2.8VCTTR: 80 mA Tiny CMOS LDO with Shutdown, SOT-23 Package. i) TC1016-2.8VLTTR: 80 mA Tiny CMOS LDO with Shutdown, SC-70 Package. j) TC1016-2.85VLTTR: 80 mA Tiny CMOS LDO with Shutdown, SC-70 Package.			

TC1016

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELoQ, KEELoQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICTail, REAL ICE, rLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2001-2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 9781620768891

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820