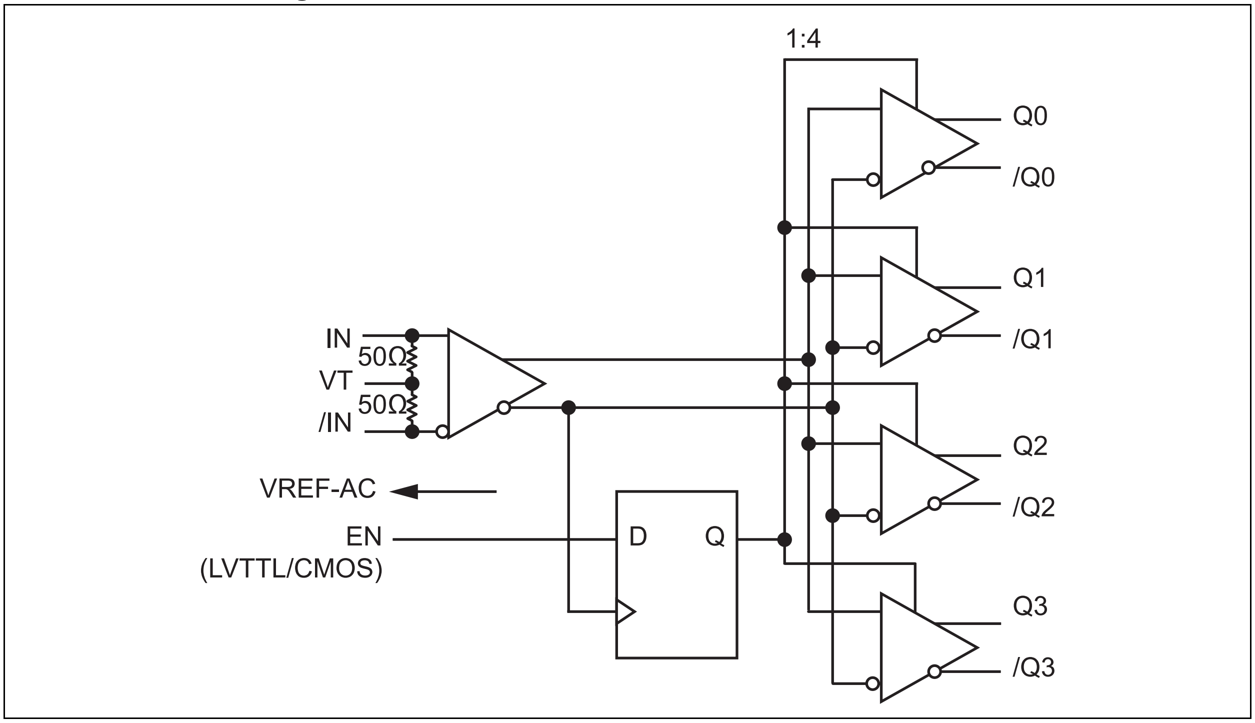
Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC} + 0.3V
LVDS Output Current (I_{OUT}) .... +10 mA
Input Current Source or Sink Current on (I_{VT}) .... ±2 mA

Operating Ratings ‡

Supply Voltage Range .... +3.0V to +3.6V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = –40°C to +85°C, unless otherwise stated. (**Note 1**).

Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
V_{CC}	Power Supply Voltage Range	3.0	3.3	3.6	V	—
I_{CC}	Power Supply Current	—	75	100	mA	—
R_{IN}	Input Resistance (IN-to-V_T)	45	50	55	Ω	—
$R_{DIFF\text{-}IN}$	Differential Input Resistance (IN-to-/IN)	90	100	110	Ω	—
V_{IH}	Input High Voltage (IN-to-/IN)	0.1	—	V_{CC} + 0.3	V	—
V_{IL}	Input Low Voltage (IN-to-/IN)	–0.3	—	V_{IH} - 0.1	V	—
V_{IN}	Input Voltage Swing (IN-to-/IN)	0.1	—	V_{CC}	V	Note 2, see Figure 5-3
V_{DIFF_IN}	Differential Input Voltage	0.2	—	—	V	Note 2, see Figure 5-4
$\lvert I_{IN} \rvert$	Input Current (IN, /IN)	—	—	45	mA	Note 2
$V_{REF\text{-}AC}$	Reference Voltage	V_{CC} - 1.525	V_{CC} - 1.425	V_{CC} - 1.325	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

2: Due to the internal termination, the input current depends on the applied voltages at IN, /IN, and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±10%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C. (Note 1)

Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
V_{OUT}	Output Voltage Swing	250	325	—	mV	see Figure 5-3
V_{DIFF_OUT}	Differential Output Voltage Swing	500	650	—	mV	see Figure 5-4
V_{OCM}	Output Common-Mode Voltage	1.125	—	1.275	V	—
ΔV_{OCM}	Change in Common-Mode Voltage	–50	—	50	mV	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C. (Note 1)

Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V	—
V_{IL}	Input Low Voltage	0	—	0.8	V	—
I_{IH}	Input High Current	–125	—	30	V	—
I_{IL}	Input Low Current	–300	—	—	mV	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 3.3V ±10%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C unless otherwise stated. (Note 1)

Symbol	Parameters	Min.	Typ.	Max.	Units	Conditions
f_{MAX}	Maximum Frequency	2.0	—	—	GHz	V_{OUT} ≥ 200 mV
t_{pd}	Propagation Delay (IN-to-Q)	400	500	600	ps	V_{IN} < 400 mV
		330	440	530	ps	V_{IN} ≥ 400 mV
t_{SKEW}	Within-Device Skew	—	5	20	ps	Note 2
	Part-to-Part Skew	—	—	200	ps	Note 3
t_S	Set-Up Time (EN to IN, /IN)	300	—	—	ps	Note 4
t_H	Hold Time (IN, /IN to EN)	500	—	—	ps	Note 4
t_{JITTER}	Additive Phase Jitter, RMS	—	96	—	fs	622.08 MHz @ 3.3V, Integration Range: 12 kHz to 20 MHz
t_r/t_f	Output Rise/Fall Times (20% to 80%)	60	110	190	ps	At Full Output Swing

Note 1: High-frequency AC parameters are guaranteed by design and characterization.

2: Within device skew is measured between two different outputs under identical input transitions.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

4: Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	—	—	+125	°C	Note 1
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20s
Package Thermal Resistances (Note 2)						
16-pin 3 mm x 3 mm VQFN (Still-Air)	θ_{JA}	—	60	—	°C/W	—
16-pin 3 mm x 3 mm VQFN	Ψ_{JB}	—	33	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. Ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 3.3V, GND = 0V, V_{IN} = 400 mV, R_L = 100Ω across the outputs; T_A = +25°C unless otherwise stated.

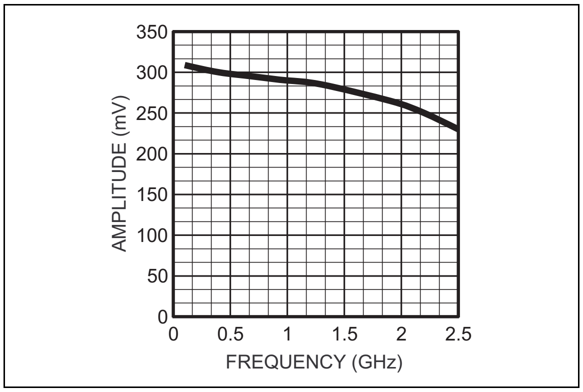


FIGURE 2-1: *Output Swing vs. Frequency.*

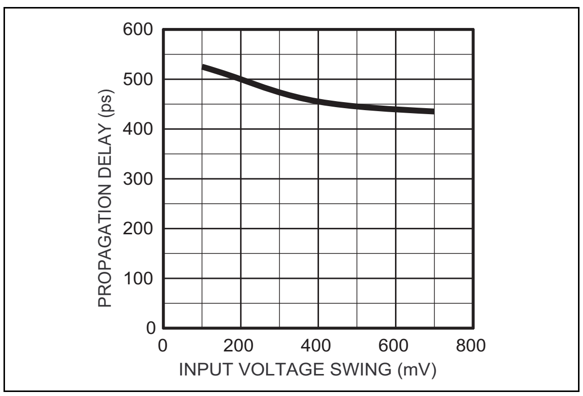


FIGURE 2-2: *Propagation Delay vs. Input Voltage Swing.*

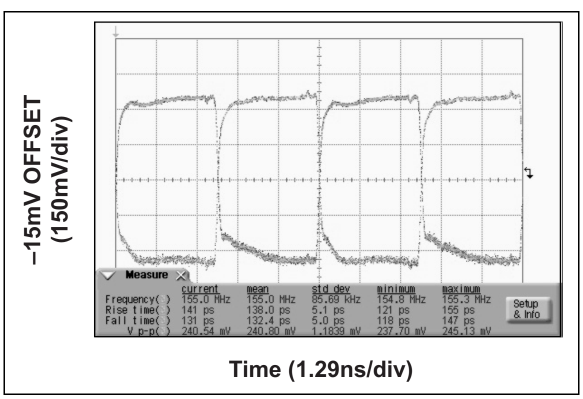


FIGURE 2-3: *155 MHz Output.*

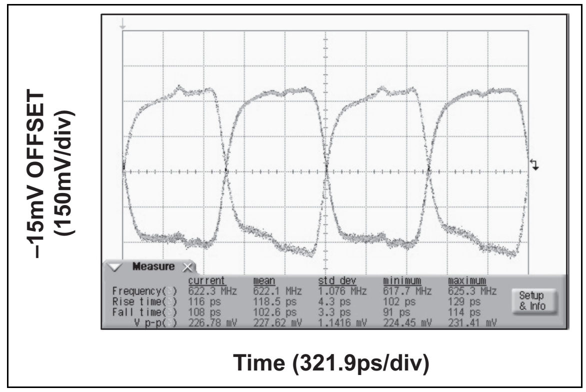


FIGURE 2-4: *622 MHz Output.*

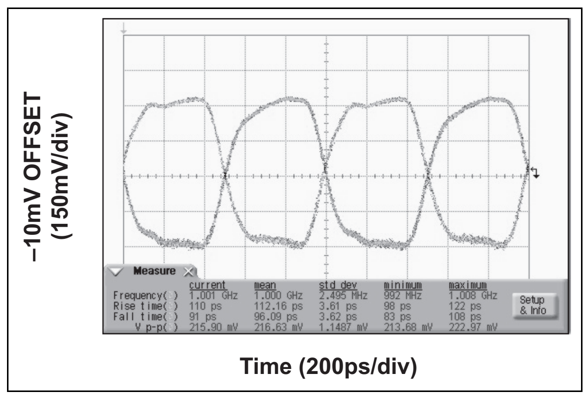


FIGURE 2-5: *1 GHz Output.*

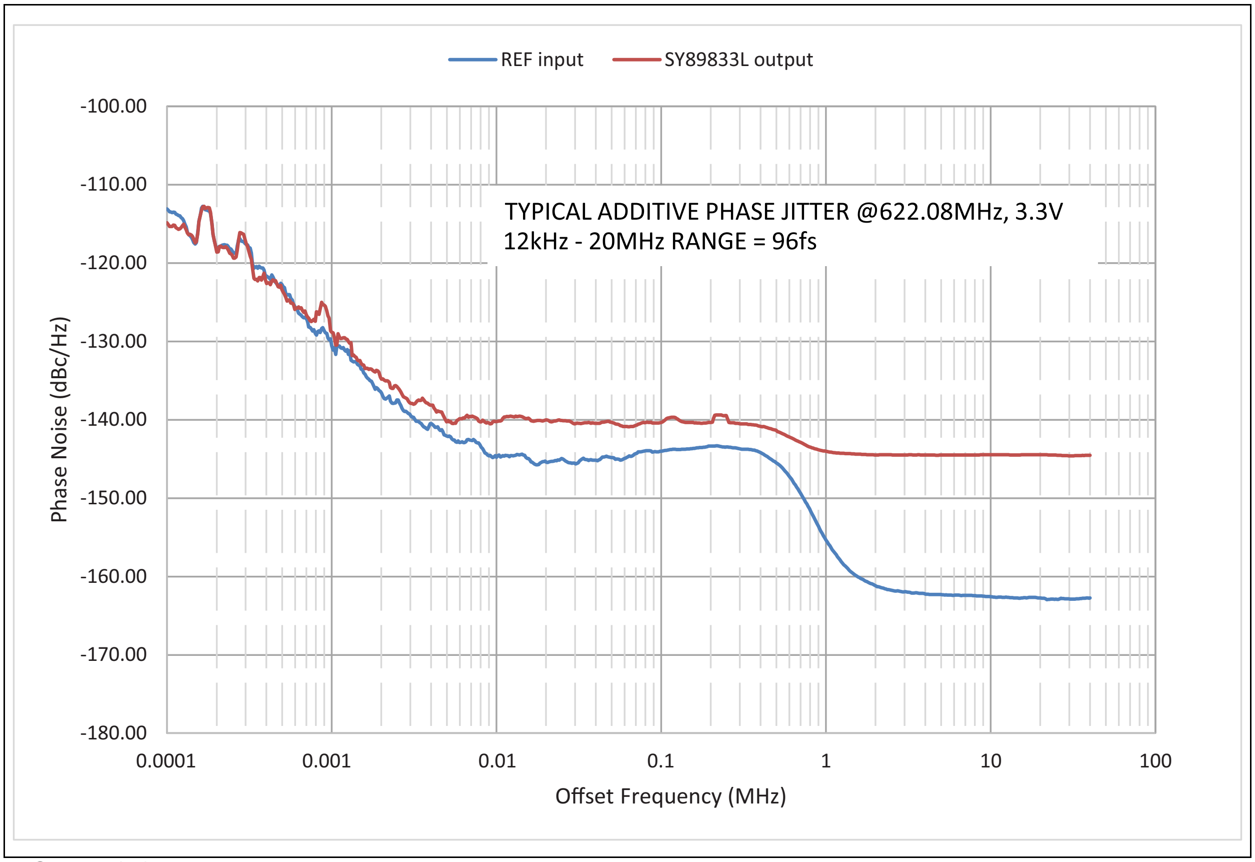


FIGURE 2-6: *Additive Phase Noise Plot.*

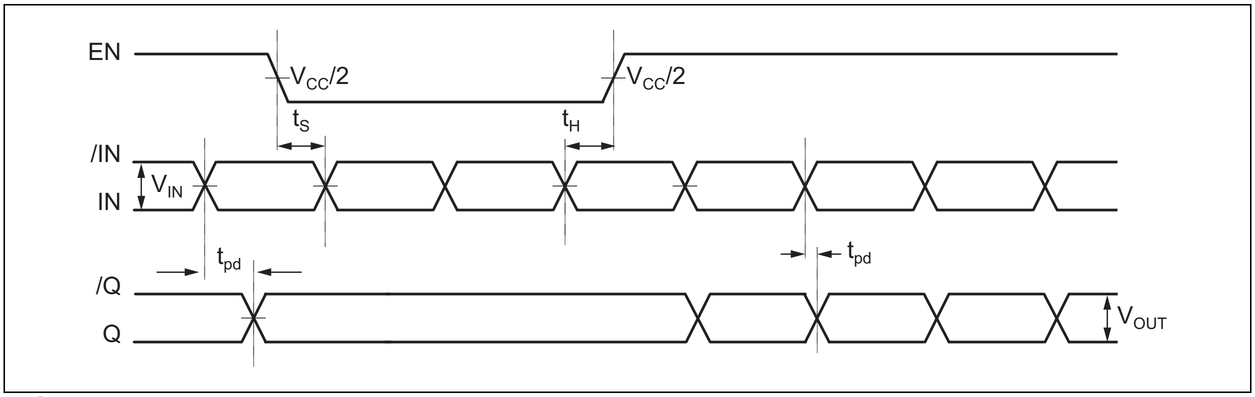


FIGURE 2-7: *Timing Diagram.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
15, 16 1, 2 3, 4 5, 6	Q0, /Q0 Q1, /Q1 Q2, /Q2 Q3, /Q3	LVDS Differential Outputs: Normally terminated with 100Ω across the pair (Q, /Q). See “LVDS Outputs” section. Unused outputs should be terminated with a 100Ω resistor across each pair.
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic low state. Note that this input is internally connected to a 25 kΩ pull-up resistor and will default to logic high state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled differential signals as small as 100 mV. Each pin of a pair internally terminates to a V_T pin through 50Ω. Note that these inputs will default to an intermediate state if left open. Please refer to the Input Interface Applications section for more details.
10	V_{REF-AC}	Reference Voltage: These outputs bias to V_{CC} – 1.425V.They are used when AC coupling the inputs (IN, /IN). For AC-coupled applications, connect V_{REF-AC} to V_T pin and bypass with 0.01 µF low-ESR capacitor to V_{CC}. See the Input Interface Applications section for more details. Maximum sink/source current is ±1.5 mA.
11	V_T	Input Termination Center-Tap: Each side of the differential input pair terminates to a V_T pin. The V_T pin provides a center-tap to a termination network for maximum interface flexibility. See the Input Interface Applications section for more details.
13	GND	Ground. GND pin and exposed pad must be connected to the most negative potential of the device ground.
7, 14	V_{CC}	Positive Power Supply: Bypass with 0.1 µF//0.01 µF low-ESR capacitors and place as close as possible to each V_{CC} pin.

TABLE 3-2: TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0 (Note 1)	1 (Note 1)

Note 1: On next negative transition of the input signal (IN).

4.0 INPUT INFORMATION

4.1 Input Stage

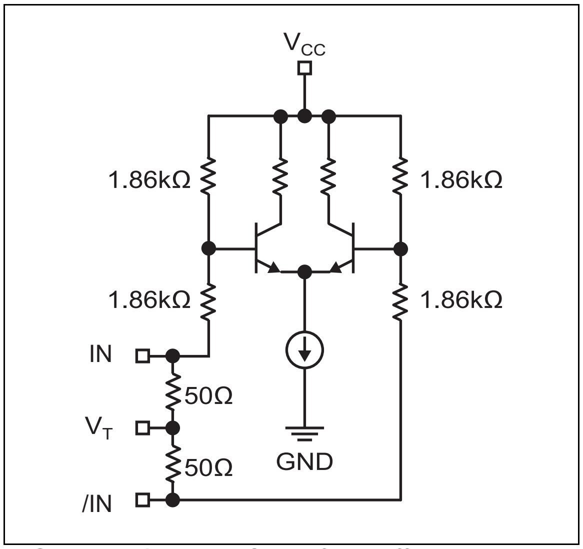


FIGURE 4-1: *Simplified Differential Input Buffer.*

4.2 Input Interface Applications

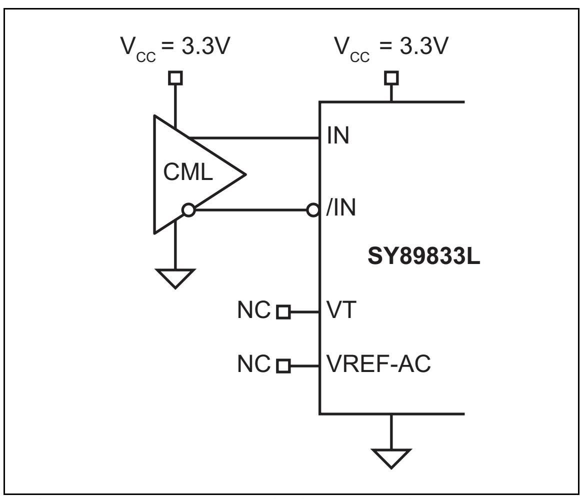


FIGURE 4-2: *DC-Coupled CML Input Interface.*

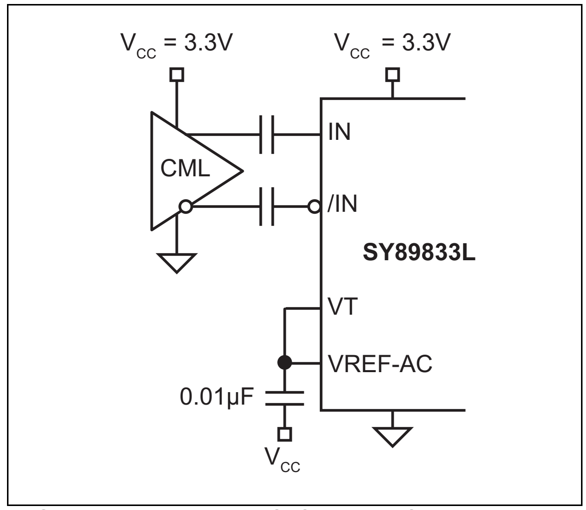


FIGURE 4-3: *AC-Coupled CML Input Interface.*

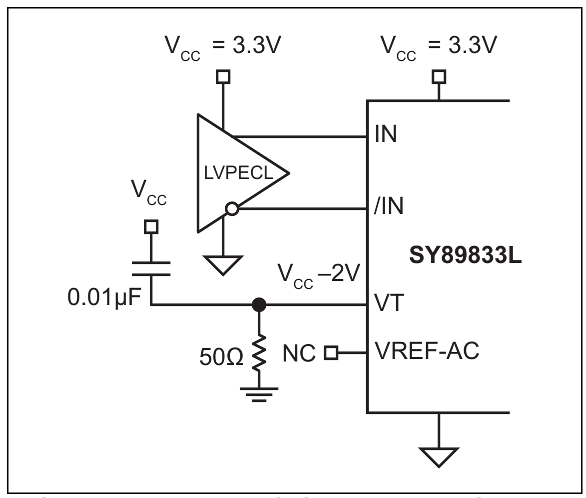


FIGURE 4-4: *DC-Coupled LVPECL Input Interface.*

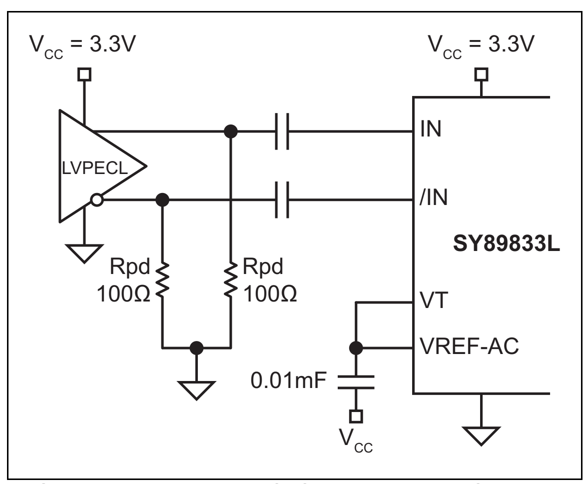


FIGURE 4-5: *AC-Coupled LVPECL Input Interface.*

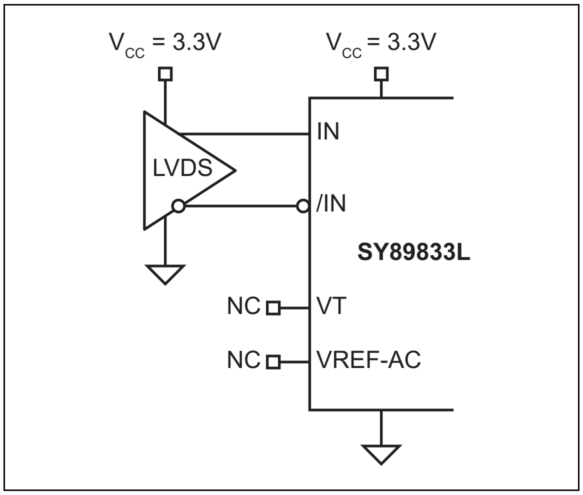


FIGURE 4-6: *LVDS Input Interface.*

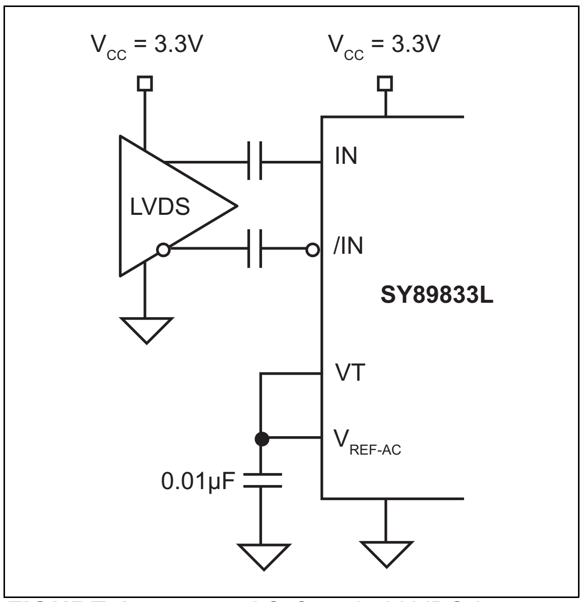


FIGURE 4-7: *AC-Coupled LVDS Input Interface.*

Please note: be certain that the LVDS driver can be AC-coupled before attempting this design.

5.0 LVDS OUTPUTS

LVDS specifies a small swing of 325 mV typical, on a nominal 1.20V common-mode above ground. The common-mode voltage has tight limits to permit large variations in ground noise between a LVDS driver and receiver.

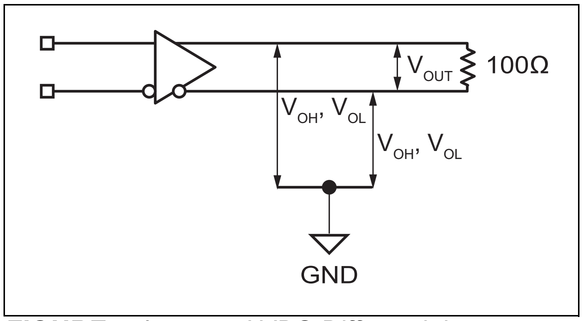


FIGURE 5-1: *LVDS Differential Measurement.*

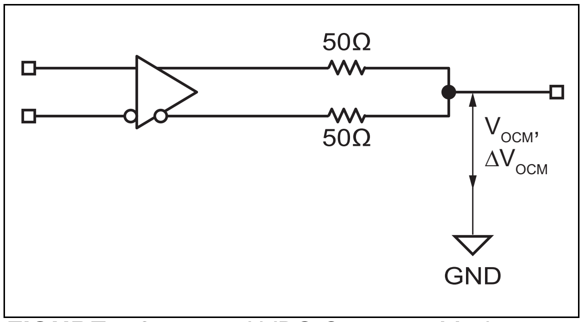


FIGURE 5-2: *LVDS Common-Mode Measurement.*

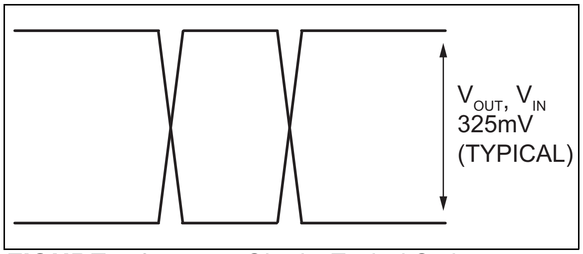


FIGURE 5-3: *Single-Ended Swing.*

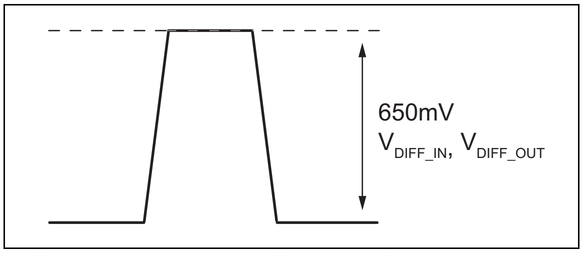
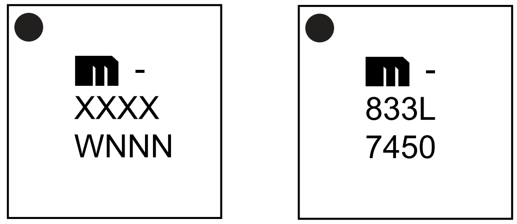


FIGURE 5-4: *Differential Swing.*

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead VQFN* Example



Legend:

XX...X	Product code or customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

●, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

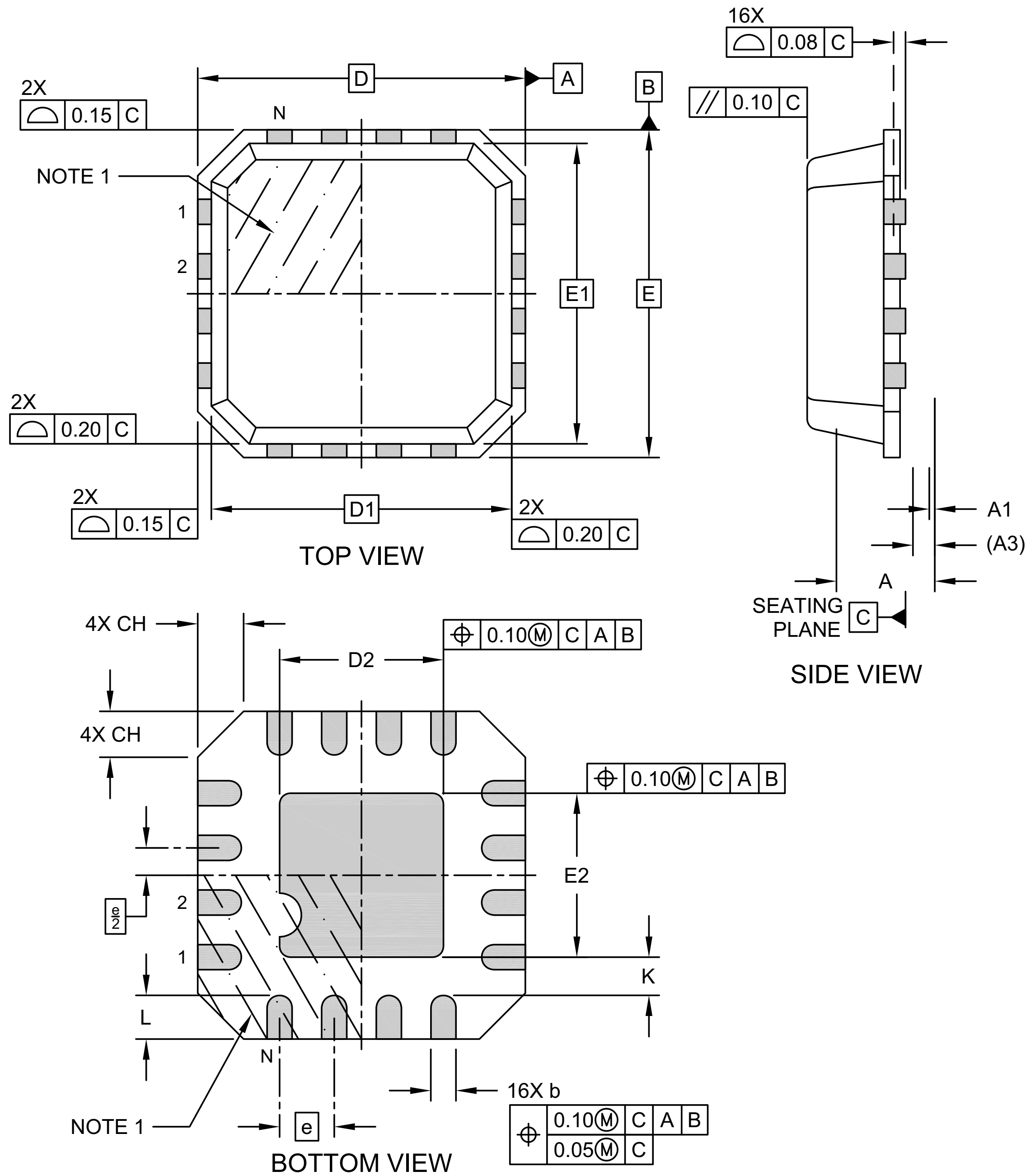
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

16-Lead 3 mm x 3 mm VQFN Package Outline and Recommended Land Pattern

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN]

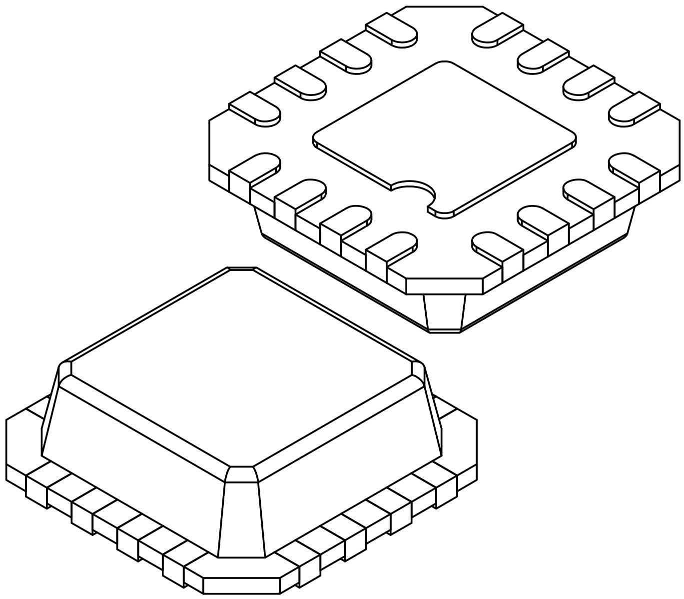
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev A Sheet 1 of 2

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.85	-	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Mold Cap Length	D1		2.75 BSC	
Exposed Pad Length	D2	1.35	1.50	1.65
Overall Width	E		3.00 BSC	
Mold Cap Width	E1		2.75 BSC	
Exposed Pad Width	E2	1.35	1.50	1.65
Body Corner Chamfer	CH	0.24	0.42	0.60
Terminal Width	b	0.16	0.23	0.28
Terminal Length	L	0.10	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

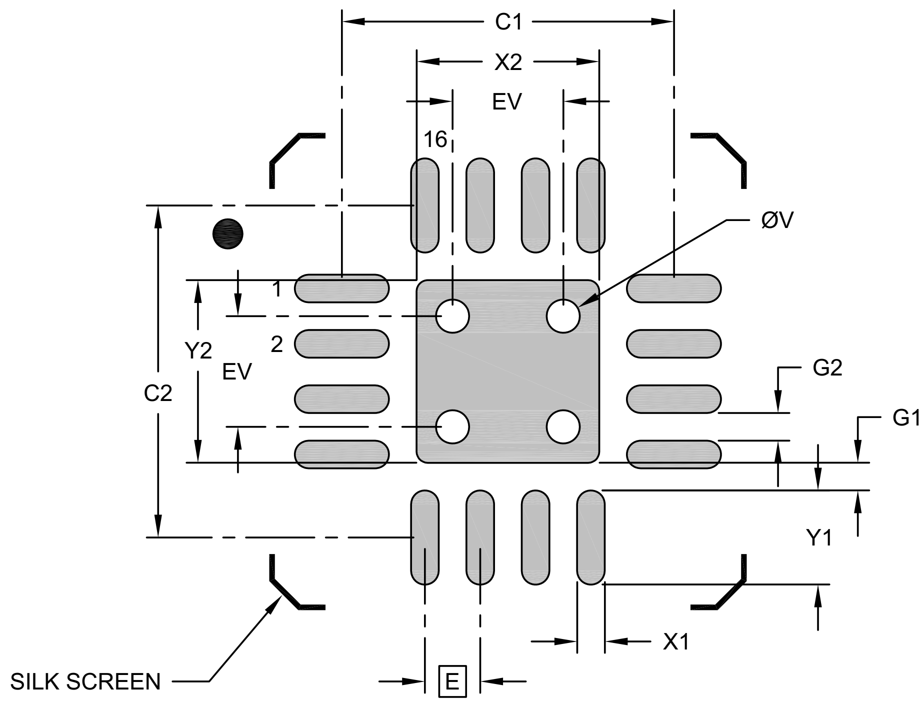
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is punch singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev A Sheet 1 of 2

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.65
Optional Center Pad Length	Y2			1.65
Contact Pad Spacing	C1		3.00	
Contact Pad Spacing	C2		3.00	
Contact Pad Width (x16)	X1			0.25
Contact Pad Length (x16)	Y1			0.85
Contact Pad to Center Pad (x16)	G1	0.25		
Contact Pad to Contact Pad (X12)	G2	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-1103-NCA Rev A

APPENDIX A: REVISION HISTORY

Revision A (June 2021)

- Converted Micrel document SY89833L to Microchip data sheet DS20005726A.
- Minor text changes throughout.
- Updated Figure 2-6.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	XX
Device	Voltage Option	Package	Temperature	Special Processing

Device:	SY89833:		3.3V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination
Voltage Option:	L	=	3.3V Only
Package:	M	=	16-Lead 3 mm x 3 mm VQFN
Temperature:	G	=	–40°C to +85°C
Special Processing:	<blank> TR	= =	100/Tube 1,000/Reel

Note 1: Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.

Examples:

a) SY89833LMG: 3.3V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination, 3.3V Voltage Option, –40°C to +85°C Temp. Range, 16-Lead VQFN 100/Tube

b) SY89833LMG TR: 3.3V Ultra-Precision 1:4 LVDS Fanout Buffer/Translator with Internal Termination, 3.3V Voltage Option, –40°C to +85°C Temp. Range, 16-Lead VQFN, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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China - Suzhou
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Japan - Osaka
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Japan - Tokyo
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Korea - Daegu
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Malaysia - Penang
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Philippines - Manila
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Singapore
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Taiwan - Hsin Chu
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Thailand - Bangkok
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Vietnam - Ho Chi Minh
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