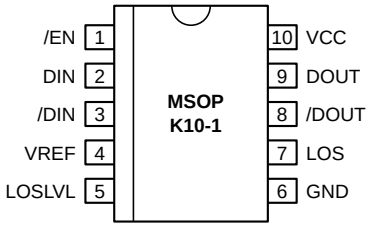
PACKAGE/ORDERING INFORMATION



10-Pin MSOP (K10-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88923VKC	K10-1	Commercial	923V	Sn-Pb
SY88923VKCTR[2]	K10-1	Commercial	923V	Sn-Pb
SY88923VKG[3]	K10-1	Industrial	923V with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY88923VKGTR[2, 3]	K10-1	Industrial	923V with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Type	Function
D_{IN}	Data Input	Data Input
$/D_{IN}$	Data Input	Inverting Data Input
LOS_{LVL}	Input	LOS Limit Set
/EN	TTL Input	Output Enable (Active Low)
LOS	TTL Output (Open Collector)	Loss of Signal Indicator (Active High)
GND	Ground	Ground
$/D_{OUT}$	PECL Output	Inverting Data Output
D_{OUT}	PECL Output	Data Output
V_{CC}	Power Supply	Positive Power Supply
V_{REF}	Output	Reference Voltage Output for LOS Level Set (see Fig. 3)

GENERAL DESCRIPTION

General

The SY88923V is an integrated limiting amplifier intended for high-frequency fiber-optic applications. The circuit connects to typical trans-impedance amplifiers found within a fiber-optics link. The linear signal output from a trans-impedance amplifier can contain significant amounts of noise, and may vary in amplitude over time. The SY88923V limiting amplifier quantizes the signal and outputs a voltage-limited waveform.

The /EN pin allows the user to disable the output signal without removing the input signal.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	0 to +7.0	V
D_{IN}, $/D_{IN}$	Input Voltage	0 to V_{CC}	V
D_{OUT}, $/D_{OUT}$	Output Voltage (with 50Ω load)	V_{CC} –2.5 to V_{CC} +0.3	V
/EN	Input Voltage	0 to V_{CC}	V
LOS_{LVL}	Input Voltage	0 to V_{CC}	V
V_{REF}	Output Voltage	V_{CC} –2.0 to V_{CC}	V
T_A	Operating Temperature Range	–40 to +85	°C
T_{store}	Storage Temperature Range	–55 to +125	°C

Note:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±10% or +3.3V ±10%, R_{LOAD} = 50Ω to V_{CC} –2V

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{CC}	Power Supply Current[1] 5V	—	40	—	40	—	30	40	—	45	mA
	3.3V	—	40	—	40	—	28	40	—	45	
I_{IL}	/EN Input LOW Current	–0.3[6]	—	–0.3[6]	—	–0.3[6]	—	—	–0.3[6]	—	mA
I_{IH}	/EN Input HIGH Current	—	20[4]	—	20[4]	—	—	20[4]	—	20[4]	µA
		—	100[5]	—	100[5]	—	—	100[5]	—	100[5]	
V_{CMR}	Common Mode Range	GND +2.0	V_{CC}	GND +2.0	V_{CC}	GND +2.0	—	V_{CC}	GND +2.0	V_{CC}	V
V_{offset}	Differential Output Offset	—	±100	—	±100	—	±17	±100	—	±100	mV
LOS_{LVL}	LOS_{LVL} Level	V_{REF}	V_{CC}	V_{REF}	V_{CC}	V_{REF}	—	V_{CC}	V_{REF}	V_{CC}	V
V_{OL}	LOS Output Low Level[2]	—	0.5	—	0.5	—	—	0.5	—	0.5	V
I_{OH}	LOS Output Leakage[3]	—	100	—	100	—	—	100	—	100	uA
V_{OH}	D_{OUT} and $/D_{OUT}$ HIGH Output	V_{CC} –1085	V_{CC} –880	V_{CC} –1025	V_{CC} –880	V_{CC} –1025	V_{CC} –955	V_{CC} –880	V_{CC} –1025	V_{CC} –880	mV
V_{OL}	D_{OUT} and $/D_{OUT}$ LOW Output	V_{CC} –1830	V_{CC} –1555	V_{CC} –1810	V_{CC} –1620	V_{CC} –1810	V_{CC} –1705	V_{CC} –1620	V_{CC} –1810	V_{CC} –1620	mV
V_{REF}	Reference Supply	V_{CC} –1.38	V_{CC} –1.26	V_{CC} –1.38	V_{CC} –1.26	V_{CC} –1.38	V_{CC} –1.32	V_{CC} –1.26	V_{CC} –1.38	V_{CC} –1.26	V
I_{REF}	V_{REF} Output Current	–0.8	0.5	–0.8	0.5	–0.8	—	0.5	–0.8	0.5	mA
V_{IH}	/EN Input HIGH Voltage	2.0	—	2.0	—	2.0	—	—	2.0	—	V
V_{IL}	/EN Input LOW Voltage	—	0.8	—	0.8	—	—	0.8	—	0.8	V

Notes:

1. No output load
2. I_{OL} = + 2mA
3. V_{OH} = 5.5V
4. V_{IN} = 2.7V
5. V_{IN} = V_{CC}
6. V_{IN} = 0.5V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±10% or +3.3V ±10%, R_{LOAD} = 50Ω to V_{CC} –2V

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
PSRR	Power Supply[1] Rejection Ratio	—	—	—	—	—	35	—	—	—	dB	Input referred, 55MHz
V_{ID}	Input Voltage Range	5	1800	5	1800	5	—	1800	5	1800	mV_{PP}	
V_{OD}	Differential Output Voltage Swing[2]	—	—	—	—	—	700	—	—	—	mV	V_{ID} = 15mV_{PP}
		—	—	—	—	—	300	—	—	—	mV	V_{ID} = 5mV_{PP}
t_{OFFL}	LOS Release Time[3] Minimum Input	—	0.5	—	0.5	—	0.1	0.5	—	0.5	µs	
t_{ONL}	LOS Assert Time[3]	—	0.5	—	0.5	—	0.2	0.5	—	0.5	µs	
t_{OFFH}	LOS Release Time[4] Maximum Input	—	0.5	—	0.5	—	0.1	0.5	—	0.5	µs	
V_{SR}	LOS Sensitivity Range	5	50	5	50	5	—	50	5	50	mV_{PP}	2^{23}-1 pattern
HYS	LOS Hysteresis	2	8	2	8	2	4.6	8	2	8	dB	2^{23}-1 pattern
t_r, t_f	Output Rise/Fall Time	—	175	—	175	—	150	175	—	175	ps	V_{ID} > 100mV_{PP}
		—	—	—	—	—	t_{rin},t_{fin}	—	—	—		V_{ID} < 100mV_{PP}

Notes:

1. Input referred noise = RMS output noise/low frequency gain.
2. Input is a 622MHz square wave.
3. Input is a 200MHz square wave, t_r < 300ps, 8mV_{PP}.
4. Input is a 200MHz square wave, t_r < 300ps, 1.8V_{PP}.

DESIGN PROCEDURE

Output Termination

The SY88923V outputs must be terminated with a 50Ω load to V_{CC} – 2V (or Thevenin equivalent).

Layout and PCB Design

Since the SY88923V is a high-frequency component, performance can largely be determined by board layout and design. A common problem with high-gain amplifiers is feedback from the large swing outputs to the input via the power supply.

The SY88923V ground pin should be connected to the circuit board ground. Use multiple PCB vias close to the part to connect to ground. Avoid long, inductive runs which can degrade performance.

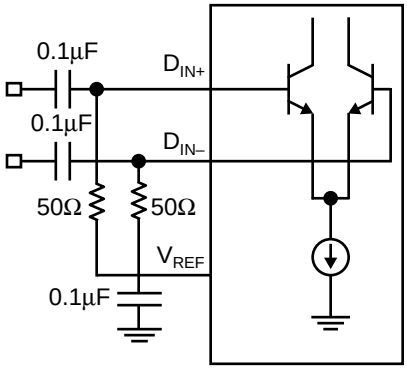


Figure 2. Differential Input Configuration

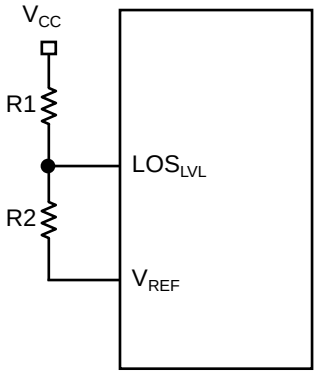


Figure 3. LOS_{LVL} Circuit

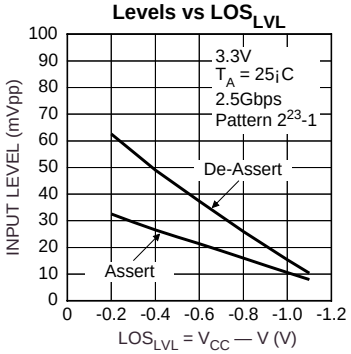
Notes:

$$LOS_{LVL} = V_{CC} - 1.32V + \frac{R2 \times 1.32V}{R1 + R2}$$

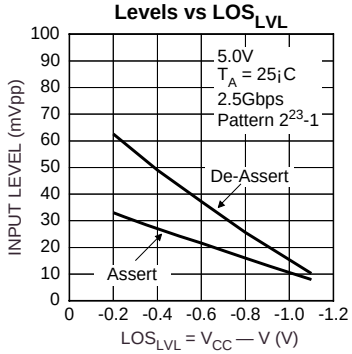
$R1 + R2 \geq 2.6k\Omega$

PERFORMANCE CURVE

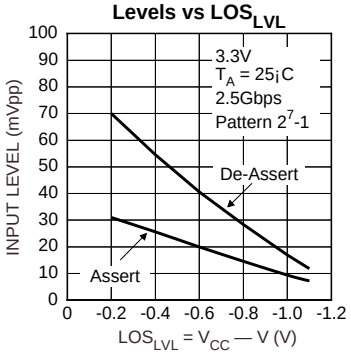
LOS Assert and De-Assert Levels vs LOS_{LVL}



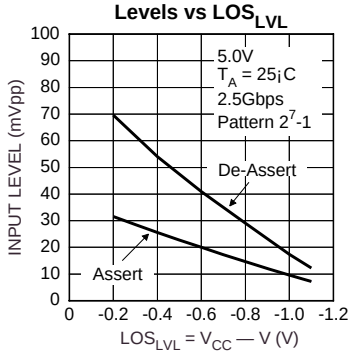
LOS Assert and De-Assert Levels vs LOS_{LVL}



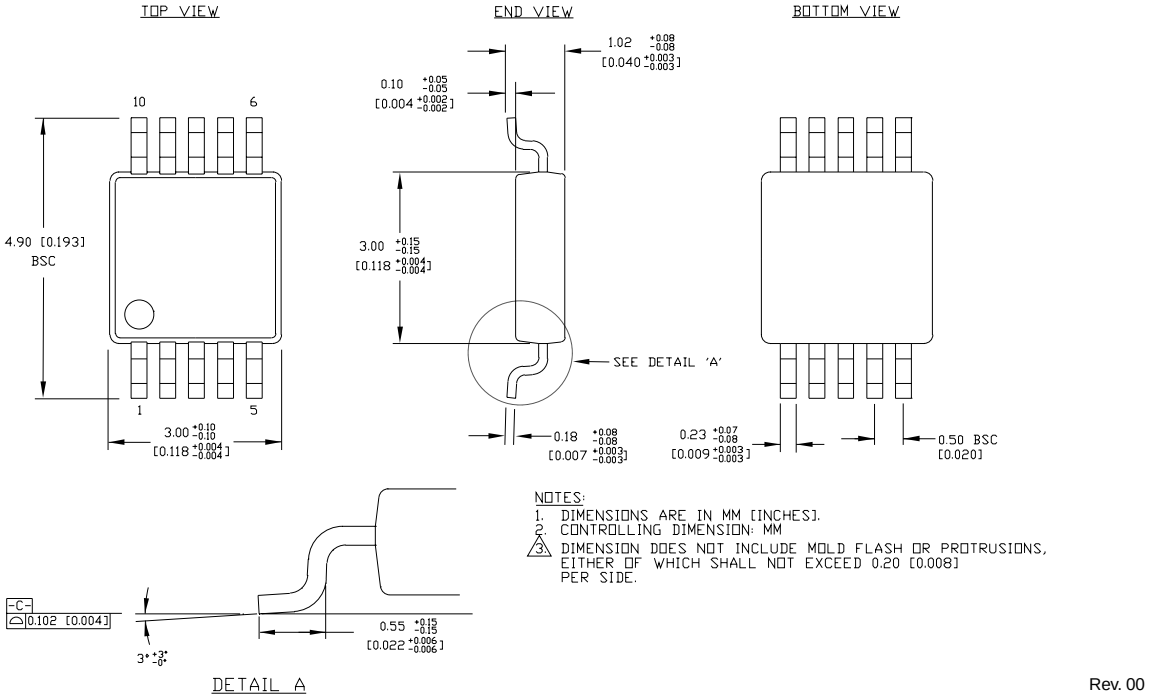
LOS Assert and De-Assert Levels vs LOS_{LVL}



LOS Assert and De-Assert Levels vs LOS_{LVL}



10-PIN MSOP (K10-1)



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