Contents

1 Electrical characteristics

Table 1. Absolute maximum ratings (limiting value)

Symbol	Parameter	Rating	Unit
AV_{DD}	Analog supply voltage	-0.3 to +5.5	V
V_{dig}	Digital supply voltage	-0.3 to +3.3	V
$V_{I/O}$	Input voltage logic lines (DATA, CLK, CS)	-0.5 to V_{dig} + 0.5	V
$V_{ESD\ (HBM)}$	Human body model, JESD22-A114-B, All I/O	2	kV
$V_{ESD\ (CDM)}$	Charge device model, JESD22-C101-C, All I/O	500	V
T_{stg}	Storage temperature range	-55 to +150	°C
T_j	Maximum junction temperature	150	°C

Table 2. Recommended operating conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
T_{AMB_oP}	Operating ambient temperature	-25	-	+85	°C
AV_{DD}	Analog supply voltage	2.3	-	5	V
V_{dig}	Digital supply voltage	1.7	-	3	V
V_{IH}	Input voltage logic level HIGH (DATA, CLK, CS)	0.7*V_{dig}	-	V_{dig} + 0.3	V
V_{IL}	Input voltage logic level LOW (DATA, CLK, CS)	-0.3	-	0.35*V_{dig}	V

Table 3. DC characteristics

Conditions: AV_{dd} from 2.3 to 5 V, V_{dig} from 1.7 to 3 V, T_{amb} from -25 °C to +85 °C unless otherwise specified						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.(1)**	**Max.**	**Unit**
I_{DD}	AV_{DD} supply current	Shutdown mode			5	µA
		Active mode (3 outputs active)		0.67	1	mA
I_{dig}	V_{dig} supply current	Shutdown mode, CS level LOW			10	µA
		Active Mode: (3 outputs active) CS LOW CS HIGH, F_{CLK} = 13 MHz CS HIGH, F_{CLK} = 26 MHz			 0.2 0.6 1	mA
I_{IH}	Input current logic level HIGH	Any mode, DATA, CLK, CS pins	-2		2	µA
I_{IL}	Input current logic level LOW	Any mode, DATA, CLK, CS pins	-2		2	µA

1. Typical value with typical application condition, V_{HV} = 20 V, AV_{DD} = 3.3 V, 25 °C, I_{load} = 3*1µA

Table 4. Boost converter characteristics

Conditions: AV_{DD} from 2.3 to 5 V, V_{dig} from 1.7 to 3 V, T_{amb} from -25 °C to +85 °C unless otherwise specified)						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{hv_low}	Minimum programmable output voltage	Active mode, DAC_boost = 0h		15		V
V_{hv_high}	Maximum programmable output voltage	Active mode, DAC_boost = Fh		30		V
Resolution	Boost voltage resolution	4 bits DAC		1		V
Error	DAC boost error	DAC A, DAC B, DAC C and DAC_boost settings according to *Table 6.*	-6		+6	$\%V_{out}$

Table 5. High voltage DAC output characteristics

Conditions: AV_{DD} from 2.3 to 5 V, V_{dig} from 1.7 to 3 V, T_{amb} from -25 °C to +85 °C, OUTA, OUTB, OUTC, unless otherwise specified)						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
SHUTDOWN MODE						
Z_{out}	OUTA, OUTB, OUTC output impedance		7			MΩ
ACTIVE MODE						
V_{OH}	OUTA, OUTB, OUTC maximum output voltage	DAC A = DAC B = DAC C = FFh DAC_boost = Fh, I_{OH} < 10 µA	26.5			V
V_{OL}	OUTA, OUTB, OUTC minimum output voltage	DAC A = DAC B = DAC C = 01h DAC_boost from 0h to Fh I_{OL} < 10 µA			2	V
R_{PD}	OUTA, OUTB, OUTC set in pull down mode	DAC A = DAC B = DAC C = 00h DAC_boost from 0h to Fh			500	Ω
Resolution	Voltage resolution / OUTA, OUTB, OUTC	8 bits DAC, full range 30 V		117.64		mV
V_{offset}	Zero scale offset	DAC A, DAC B, DAC C and DAC_boost settings according to *Table 6.*	-2		+2	LSB
INL	Integral non linearity	DAC A, DAC B, DAC C and DAC_boost settings according to *Table 6.*	-3		+3	LSB
DNL	Differential non linearity	DAC A, DAC B, DAC C and DAC_boost settings according to *Table 6.*	-0.5		+0.5	LSB
Δgain	Gain error	DAC A, DAC B, DAC C and DAC_boost settings according to *Table 6.*	-6		+6	%V_{out}
I_{sc}	Over current protection	Any DAC output			50	mA

Table 6. Recommended settings for DAC outputs and DAC_boost

Conditions: AV_{DD} from 2.3 to 5 V, V_{dig} from 1.7 to 3 V, T_{amb} from -25 °C to +85 °C, OUTA, OUTB, OUTC, unless otherwise specified						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
DAC_{MIN}	Minimum DAC setting	DAC_boost from 0H to FH	13h			-
DAC_{MAX}	Maximum DAC setting	DAC_boost = 0h DAC_boost = 1h DAC_boost = 2h DAC_boost = 3h DAC_boost = 4h DAC_boost = 5h DAC_boost = 6h DAC_boost = 7h DAC_boost = 8h DAC_boost = 9h DAC_boost = Ah DAC_boost = Bh DAC_boost = Ch DAC_boost = Dh DAC_boost = Eh DAC_boost = Fh			5Dh 65h 6Dh 75h 7Dh 85h 8Dh 95h 9Dh A5h ADh B5h BDh C5h CDh D5h	-
$VDAC_{typ}$	Typical DAC output voltage	DAC_boost = 0h, DACx = DAC_{MAX} DAC_boost = 1h, DACx = DAC_{MAX} DAC_boost = 2h, DACx = DAC_{MAX} DAC_boost = 3h, DACx = DAC_{MAX} DAC_boost = 4h, DACx = DAC_{MAX} DAC_boost = 5h, DACx = DAC_{MAX} DAC_boost = 6h, DACx = DAC_{MAX} DAC_boost = 7h, DACx = DAC_{MAX} DAC_boost = 8h, DACx = DAC_{MAX} DAC_boost = 9h, DACx = DAC_{MAX} DAC_boost = Ah, DACx = DAC_{MAX} DAC_boost = Bh, DACx = DAC_{MAX} DAC_boost = Ch, DACx = DAC_{MAX} DAC_boost = Dh, DACx = DAC_{MAX} DAC_boost = Eh, DACx = DAC_{MAX} DAC_boost = Fh, DACx = DAC_{MAX}		10.90 11.84 12.77 13.71 14.65 15.59 16.52 17.46 18.40 19.34 20.27 21.21 22.15 23.09 24.02 24.96		V

2 Functional block diagram

Figure 2. HVDAC functional block diagram

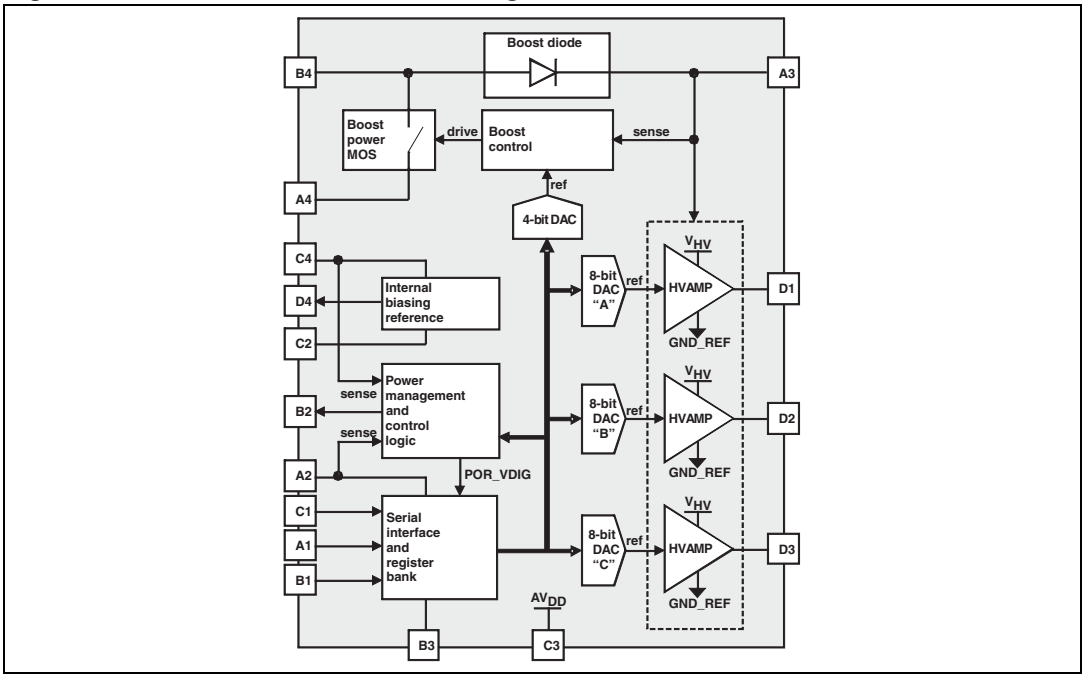


Table 7. Signal descriptions

Pin number	Pin name	Description
A1	DATA	Serial interface / Serial DATA
A2	V_{dig}	Digital supply
A3	VHV	Boost high voltage output
A4	GND_BOOST	Ground
B1	CS	Serial interface / Chip select
B2	TEST	Test pin / connected to GND in final application
B3	GND_DIG	Ground
B4	IND_BOOST	Boost inductance
C1	CLK	Serial interface / Serial clock
C2	GND_REF	Analog ground
C3	AVDD	Analog supply
C4	AVDD	Analog supply
D1	OUTA	High voltage output A
D2	OUTB	High voltage output B
D3	OUTC	High voltage output C
D4	R_{bias}	Biasing reference resistance

3 Theory of operation

3.1 HVDAC output voltages

The HVDAC outputs are directly controlled by programming the 8-bit DAC (DAC A, DAC B and DAC C) through the 3-wire serial interface.

The DAC stages are driven from a reference voltage, generating an analog output voltage driving a high voltage amplifier supplied from the boost converter (see HVDAC block diagram - *Figure 2*).

The HVDAC output voltages are scaled from 0 to 30 V, with 255 steps of 117 mV (30/255 = 0.11764 V). The nominal HVDAC output can be approximated to 117 mV x (DAC value).

For performance optimization, it is also possible to control the boost output voltage (VHV) from 15 V to 30 V, by programming the DAC_boost value (4 bits / 1 V step).

For proper operation, ST recommends the operation of the HVDAC outputs 2 V below the actual boost output voltage (VHV), to avoid clamping the HVDAC outputs to the boost output voltage.

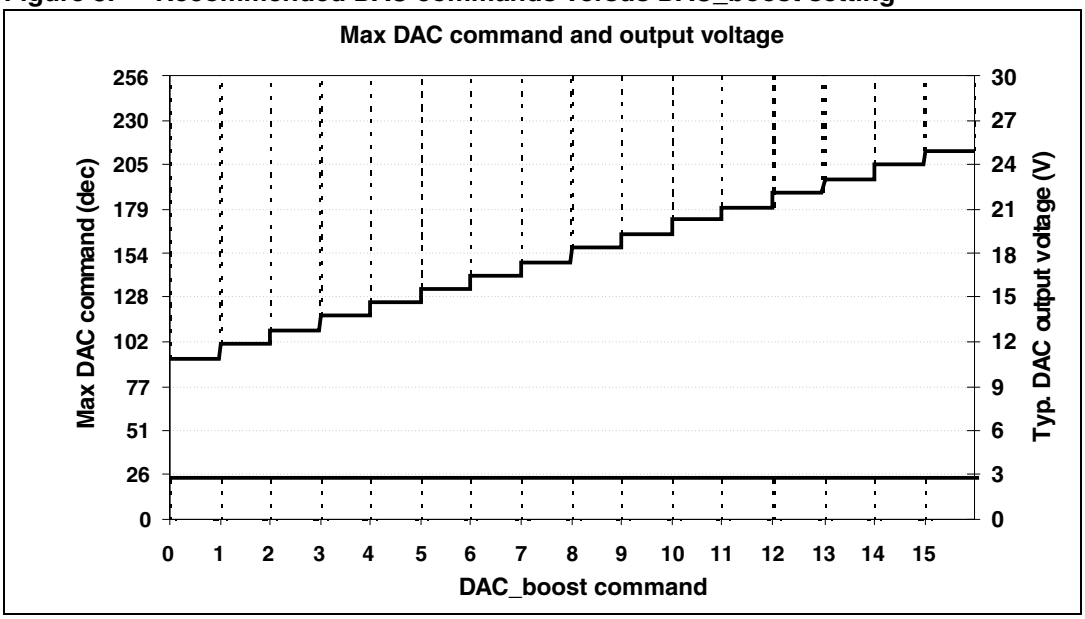
Recommended settings for DAC A, DAC B and DAC C according to DAC_boost settings are described in *Table 6.*, considering the overall HVDAC accuracy. These recommended settings are further described on *Figure 5*

Minimum HVDAC output voltage is also limited to 2 V, meaning minimum DAC command is equal to 19 (or 13h), independent of the DAC_boost setting.

DAC settings can be programmed outside this recommended operating range, but in this case the HVDAC performance (accuracy and noise) be outside the specified range.

If DAC value is set to 00 h, then the corresponding output is directly connected to GND through a pull-down resistor (500 Ω).

Figure 3. Recommended DAC commands versus DAC_boost setting



3.2 Operating modes

The following operating modes are accessible through the serial interface:

- **Shutdown mode:** The HVDAC is switched off, and all the blocks in the control ASIC are switched off. Power consumption is almost zero in this mode, the DAC outputs are in high Z state. The shutdown mode is set by sending a dedicated command through the serial interface.
- **Active mode:** The HVDAC is switched on and the DAC outputs are fully controlled through the serial interface. The DAC settings can be dynamically modified and the HV outputs will be adjusted according to the specified timing diagrams. Each DAC can be individually controlled and/or switched off according to application requirements. This mode is set and controlled through serial interface commands.

3.3 Power-on reset

Power-on reset is implemented on the V_{dig} supply input, ensuring the HVDAC will be reset to default mode once V_{dig} supply line rises above a given threshold (typically 1 V). This trigger will force all registers to their default value.

3.4 3-wire serial interface

The HVDAC is fully controlled through a 3-wire serial interface (DATA, CS, CLOCK).This interface is further described in the next sections of this document.

3.5 Power-up / down sequence

Table 8 and *Figure 5* describe the HVDAC settling time requirements and recommended timing diagrams.

Switching from shutdown to active mode is triggered by sending a dedicated serial interface command.

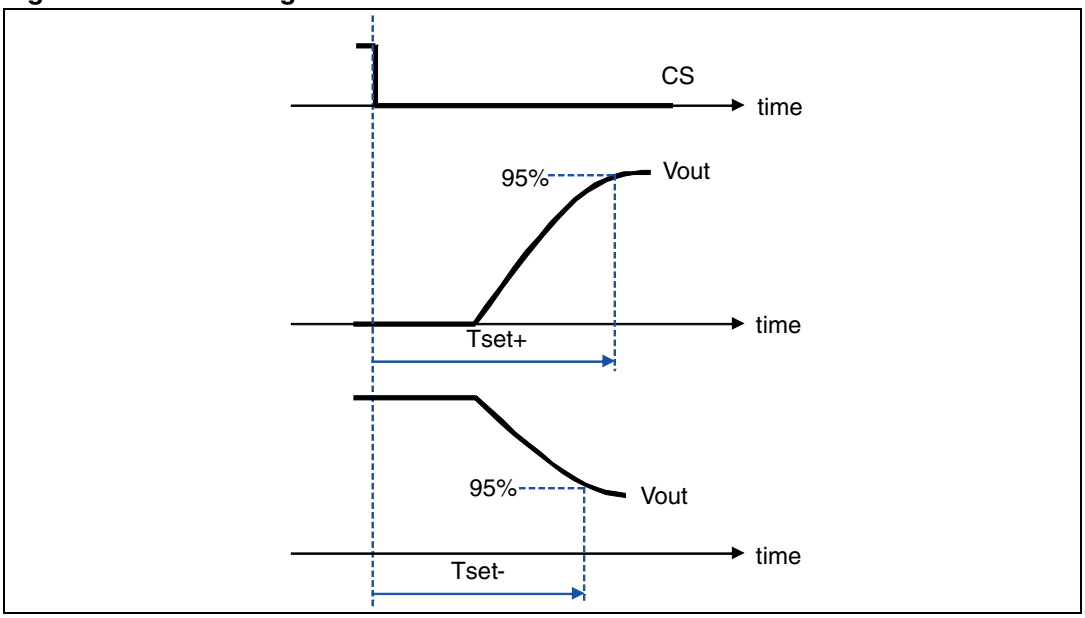
Switching from active to shutdown mode will occur after sending the related command through the 3-wire serial interface.

Active mode can be directly activated from shutdown. In any case the HVDAC will be operational only after T_{active} (max 300 µs). A settling time (T_{set}) is required following each DAC command in active mode. During this settling time the HVDAC output voltages will vary from the initial to the updated DAC command.

3.6 Settling time

The ST HVDAC will set the bias voltage of the tuner within 35 µs after the chip select is released. The setting time is defined as the time it takes for the output to reach 95% of its final value. A positive setting time (T_{set} +) is defined when the output voltage rises and a negative setting time (T_{set} -) when it decreases to its final value. See *Figure 4* for details.

Figure 4. Bias voltage of the tuner



3.7 Power supply sequencing

The ST HVDAC does not require any specific power supply sequencing. It is assumed that the AV_{DD} input will be directly supplied from the battery and will then be the first on.

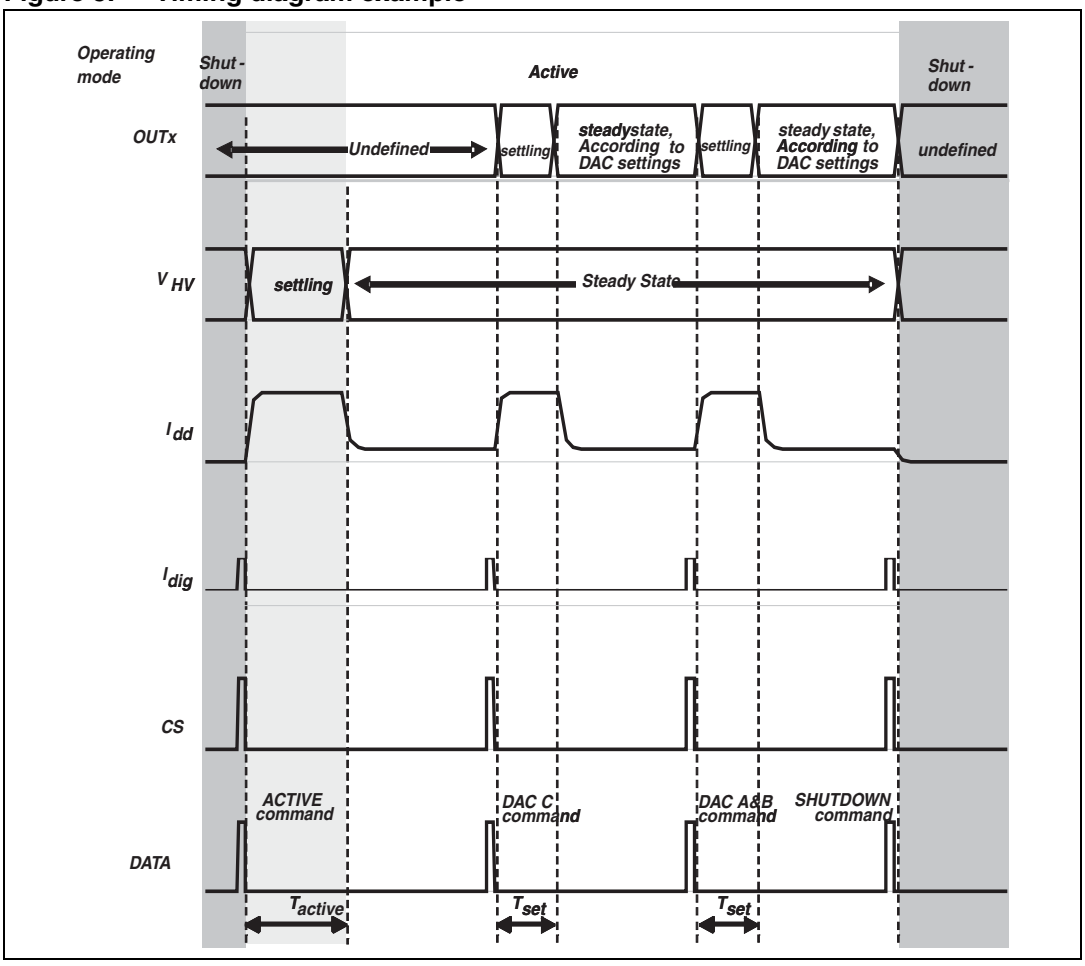
If V_{dig} supply is pulsed, 5 µs are required (max) to settle internal voltages before sending the first command through the 3-wire serial interface.

3.8 Timing parameters

Table 8. Timing parameters

Conditions: AV_{DD} from 2.3 to 5 V, V_{dig} from 1.7 to 3 V, T_{amb} from -25 °C to +85 °C, OUTA, OUTB, OUTC, unless otherwise specified				
Symbol	**Parameter**	**Conditions**	**max.**	**Unit**
T_{active}	Activation time	Internal voltages activation time from shutdown to active mode C_{hv} = 22 nF, DAC_boost = 07h	300	µs
T_{set+}	Output positive setting time @ 95%	C_{hv} = 22 nF, DAC boost 07h, V_{out} 00h to 88h (worst-case), equivalent load of 15 kΩ and 1 nF	35	µs
T_{set-}	Output negative setting time @ 95%	C_{hv} = 22 nF, DAC boost 07h, V_{out} 88 h to 13 h, equivalent load of 15 kΩ and 1 nF	35	µs

Figure 5. Timing diagram example



4 Register table

The HVDAC embeds 5 x 16-bit registers. Registers content is described in *Table 9.*

Registers 1 to 3 are used to control the mode of operations and the HVDAC settings. HVDAC control and settings are thus fully ensured by programming these three registers.

Registers 4 and 5 are reserved for test purpose, and should not be addressed.

Table 9. Register table

Reg #	Name	Purpose	Access type	Size (bits)
1	DAC control DATA register #1	Used to set up OUT C	W	16
2	DAC control DATA register #2	Used to set up OUT A and B	W	16
3	DAC control Mode register	Used to set up the operating modes	W	16
4	Reserved			
5	Reserved			

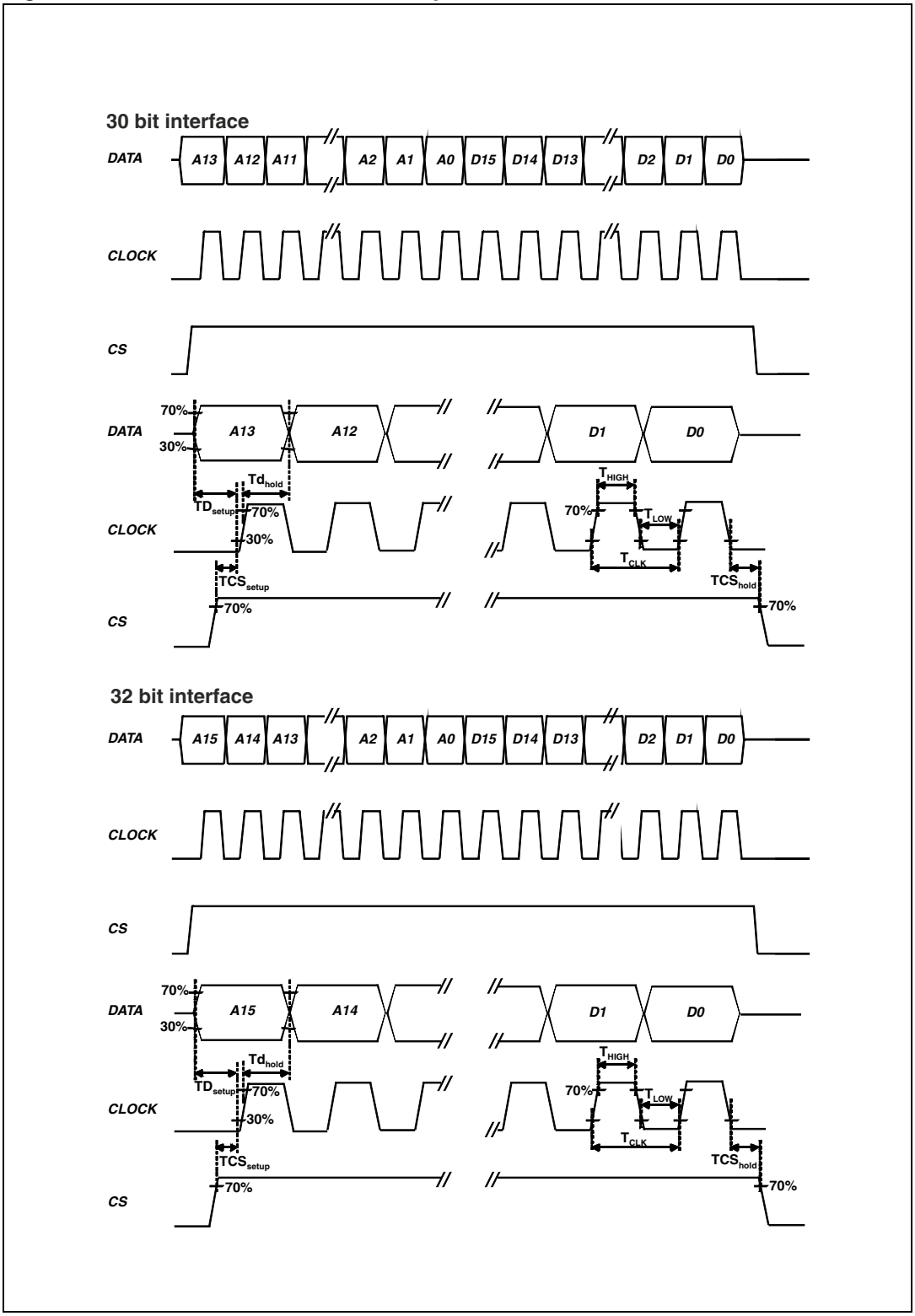
5 Serial interface specification

Table 10. Interface specification

Conditions: AV_{DD} from 2.3 to 5 V, V_{dig} from 1.7 to 3 V, T_{amb} from -25 °C to +85 °C, unless otherwise specified						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
F_{CLK}	Clock frequency				26	MHz
T_{CLK}	Clock period		38.4			ns
T_{HIGH}	Clock high time		13			ns
T_{LOW}	Clock low time		13			ns
N_{BIT}	SPI telegram length	STHVDAC-303Ix6	30			bits
N_{BIT}	SPI telegram length	STHVDAC-303x6	32			bits
TCS_{setup}	CS setup time	70% of rising edge of CS to 30% of rising edge of first clock cycle	5			ns
TCS_{hold}	CS hold time	30% of falling edge of last CLK cycle to 70% of falling edge of CS	5			ns
TD_{setup}	DATA setup time	Relative to 30% of CLK rising edge	4			ns
TD_{hold}	DATA hold time	Relative to 70% of CLK rising edge	4			ns
C_{CLK}	CLK pin input capacitance	V_{OSC} = 30 mV, F = 1 MHz			5	pF
C_{DATA}	DATA pin input capacitance				5	pF
C_{CS}	CS pin input capacitance				5	pF

In *Figure 6: 3-wire serial interface description* the data is presented on the falling edge of CLK, and latched on the rising edge of CLK. Command is latched on the falling edge of CS.

Figure 6. 3-wire serial interface description



6 Serial interface frame structure

Table 11. 30-bit frame address decoding

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	1	0	0	X	X	X	X	X
Fixed	Tuner			Device ID					Register address for operation				

Table 12. 32-bit frame address decoding

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	1	0	1	0	0	1	0	0	X	X	X	X	X
Fixed			Tuner			Device ID					Register address for operation				

Table 13. Register decoding

Command	A4	A3	A2	A1	A0	DATA
#1	0	0	0	0	0	<15:8> reserved <7:0> DAC C
#2	0	0	0	0	1	<15:8> DAC B <7:0> DAC A
#3	1	0	0	0	0	Mode selection
#4	1	1	0	0	0	Reserved
#5	1	0	0	1	0	Reserved

Table 14. Data decoding for data register [00000]

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved								DAC C							

Table 15. Data decoding for data register [00001]

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DAC B								DAC A							

Table 16. Data decoding for mode selection register [10000]

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	DAC_BOOST				Mode		0	0	DAC A	DAC B	DAC C	0

Table 17. HV-DAC mode selection - Register [10000]

D11	D10	D9	D8	D7	D6	D3	D2	D1	Comments	
DAC boost				Mode		DAC A	DAC B	DAC C		
0	0	0	0	Active mode		x	x	x	VHV = 15V	
0	0	0	1			x	x	x	VHV = 16V	
0	0	1	0			x	x	x	VHV = 17V	
0	0	1	1			x	x	x	VHV = 18V	
0	1	0	0			x	x	x	VHV = 19V	
0	1	0	1			x	x	x	VHV = 20V	
0	1	1	0			x	x	x	VHV = 21V	
0	1	1	1			x	x	x	VHV = 22V	
1	0	0	0			x	x	x	VHV = 23V	
1	0	0	1			x	x	x	VHV = 24V	
1	0	1	0			x	x	x	VHV = 25V	
1	0	1	1			x	x	x	VHV = 26V	
1	1	0	0			x	x	x	VHV = 27V	
1	1	0	1			x	x	x	VHV = 28V	
1	1	1	0			x	x	x	VHV = 29V	
1	1	1	1			x	x	x	VHV = 30V	
x	x	x	x	0	0	x	x	x	Shutdown mode	
x	x	x	x	0	1	x	x	x	reserved	
x	x	x	x	1	0	x	x	x	Active mode	
x	x	x	x	1	1	x	x	x	reserved	
x	x	x	x	1	0	0	0	0	Active mode / DAC outputs in high Z-state	Any DAC outputs combination possible, as described in *Table 6.*
x	x	x	x	1	0	1	1	1	Active mode / DAC outputs enabled	

Table 18. HVDAC mode selection default settings - Register [10000]

D11	D10	D9	D8	D7	D6	D3	D2	D1
DAC boost				Mode		DAC A	DAC B	DAC C
0	0	0	0	0	0	0	0	0

Table 19. Data registers [00000] default settings

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reserved								DAC C							

Table 20. Data registers [00001] default settings

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAC B								DAC A							

7 Application schematic

Figure 7. Recommended application schematic

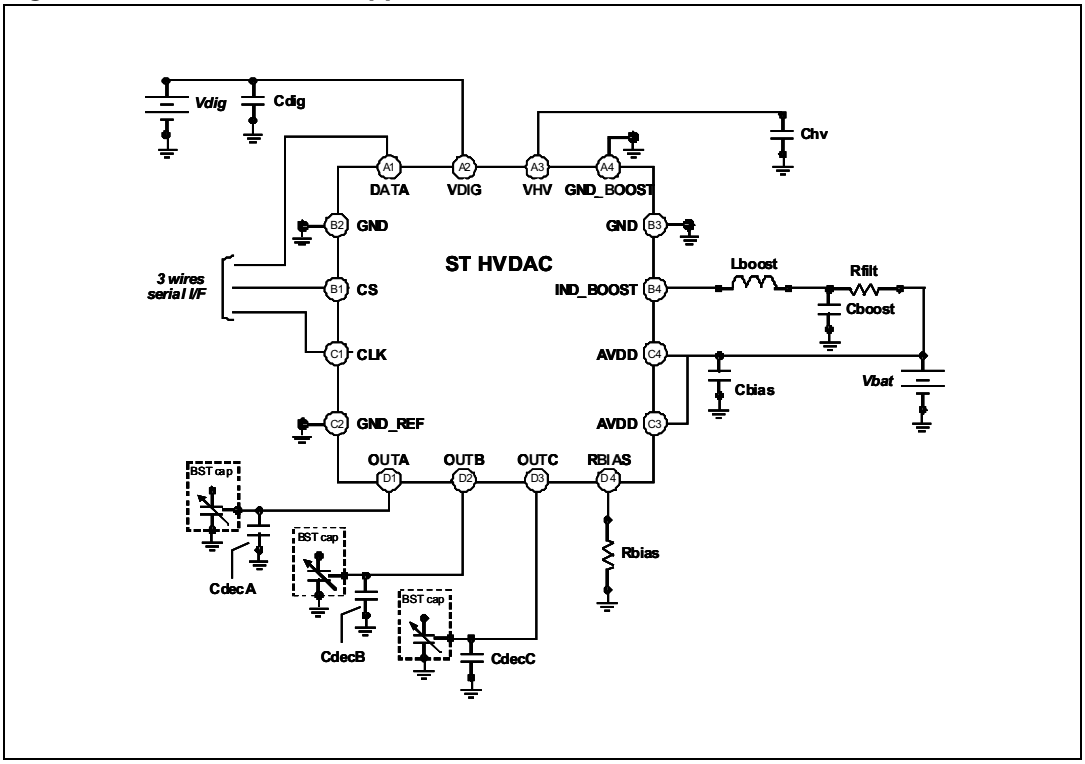


Figure 8. Recommended PCB layout

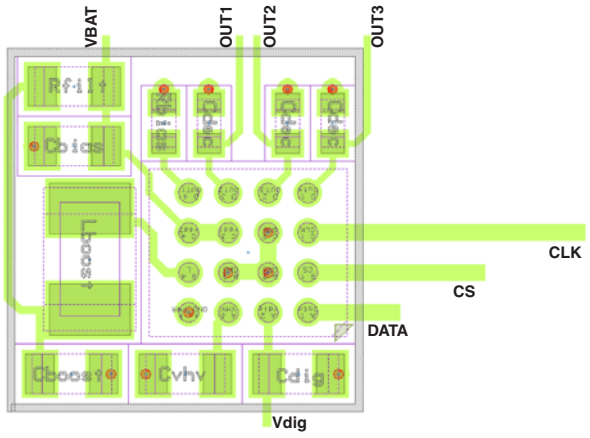


Table 21. Recommended external BOM

Component	Description	Nominal value	Package (inch)	Package (mm)	Recommended P/N
C_{boost}	Boost supply capacitor	1 µF	0402	1005	Murata: GRM155R60J105KE19D
L_{boost}	Boost inductance	15 µH	0603	1608	COILCRAFT: 0603LS-153XGL
				2014	ABCO: LPS181210T-150M
R_{filt}	Decoupling resistor, 5%	3.3 Ω	0402	1005	Vishay: CRCW04023R30JNED
C_{dig}	Digital supply decoupling	100 nF	0402	1005	Murata: GRM155R71C104KA88D
C_{bias}	Analog supply decoupling	1 µF	0402	1005	Murata: GRM155R60J105KE19D
R_{bias}	Reference bias resistor, 1%	110 kΩ	0201	0603	Multicomp: MCRE000189
C_{hv}	Boost output capacitance, 50 V	22 nF	0402	1005	Murata: GRM155R71H223KA12 Semco: CL21B223KBCNNNC
C_{dec}	Decoupling capacitance, 50 V	100 pF	0201	0603	TDK: C0603COG1H101J

8 Ordering information schemes

Figure 9. Ordering information scheme for 30-bit serial peripheral interface

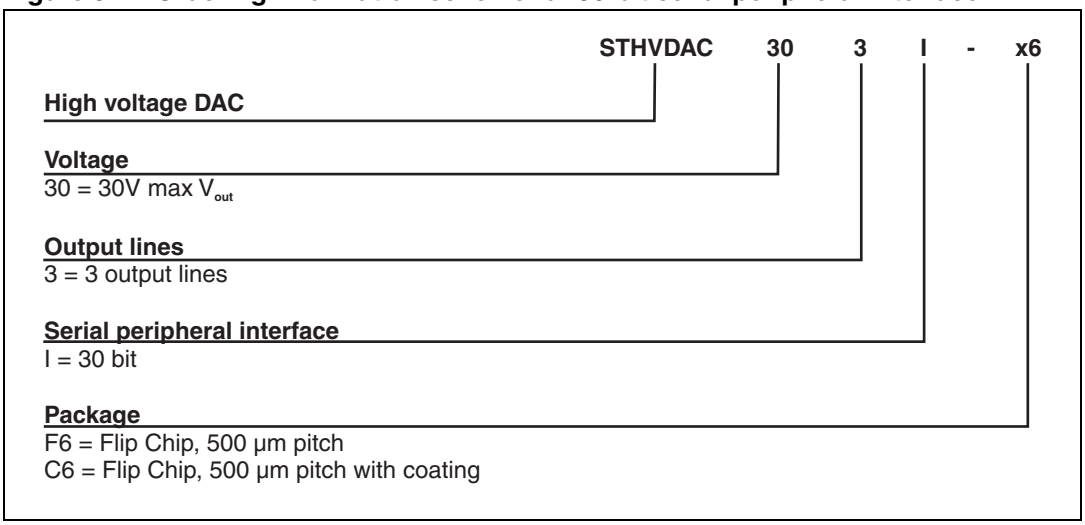
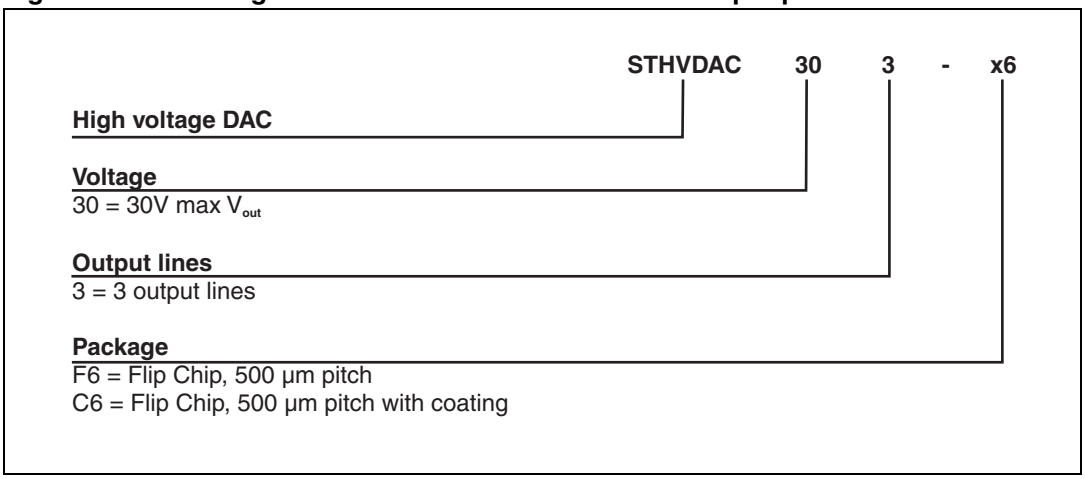


Figure 10. Ordering information scheme for 32-bit serial peripheral interface



9 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 11. Package dimensions

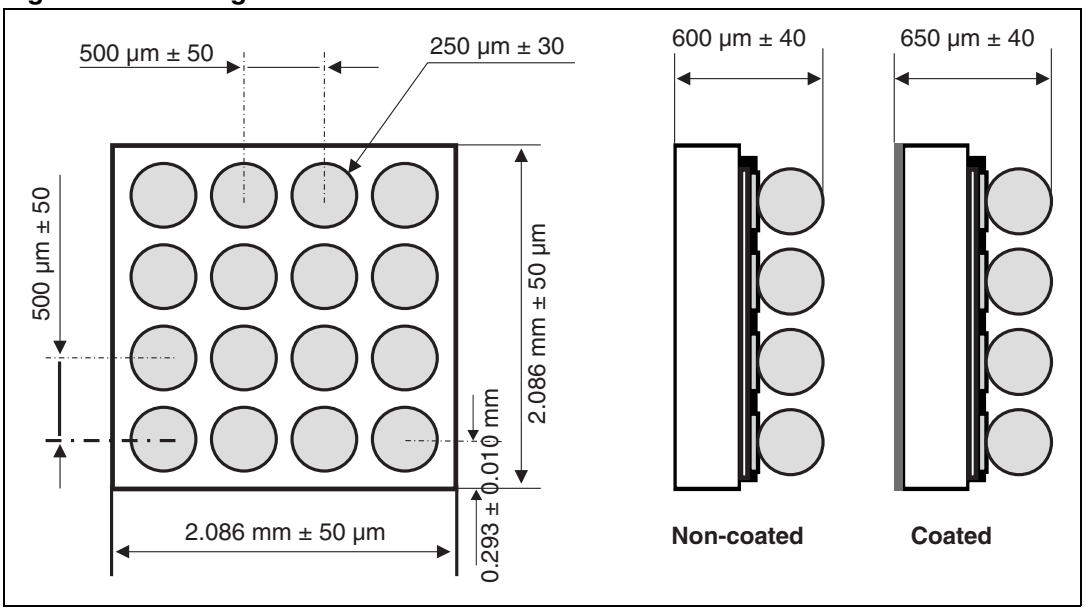


Figure 12. Footprint

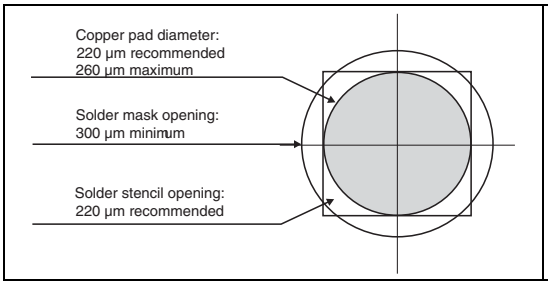


Figure 13. Marking

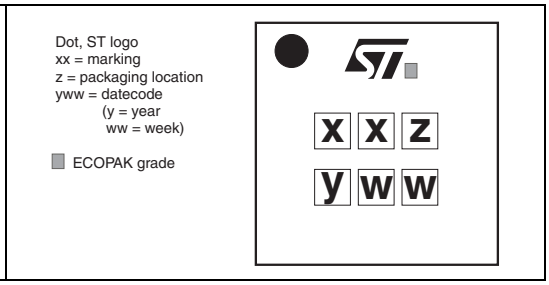
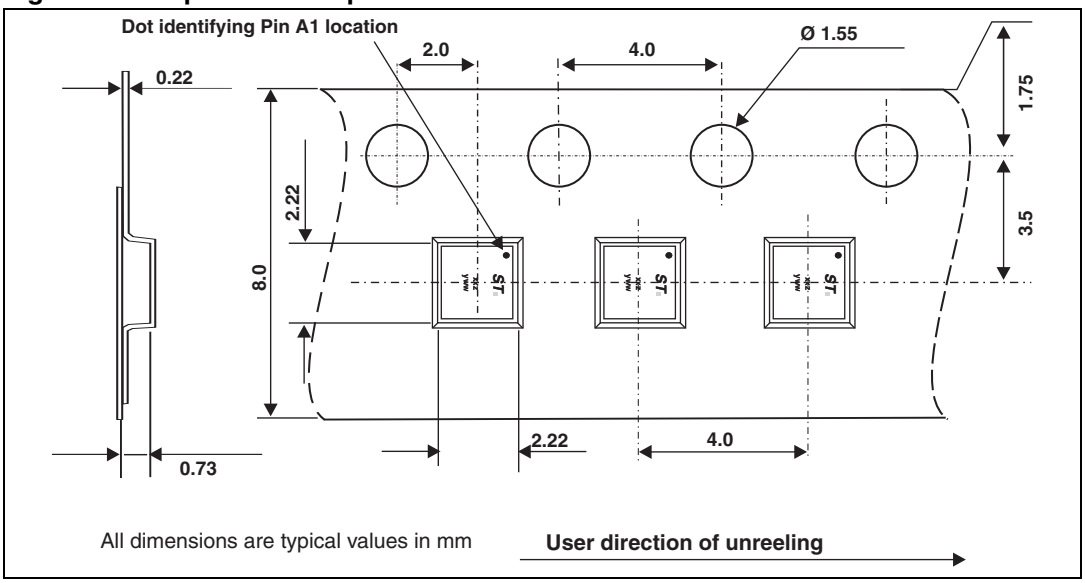


Figure 14. Tape and reel specification



10 Ordering information

Table 22. Ordering information

Order code	SPI	Marking	Package	Weight	Base qty	Delivery mode
STHVDAC-303IF6	30 bits	PC	Flip Chip	5 mg	5000	Tape and reel
STHVDAC-303IC6	30 bits	PE	Coated Flip Chip	5.3 mg		
STHVDAC-303F6	32 bits	PA	Flip Chip	5 mg		
STHVDAC-303C6	32 bits	PD	Coated Flip Chip	5.3 mg		

Note: More information is available in the STMicroelectronics Application note: AN1235: "Flip Chip: Package description and recommendations for use"

11 Revision history

Table 23. Document revision history

Date	Revision	Changes
14-Mar-2011	1	Initial release.
04-Apr-2012	2	Corrected typographical error in *Application*.
05-Nov-2012	3	Updated document status.

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