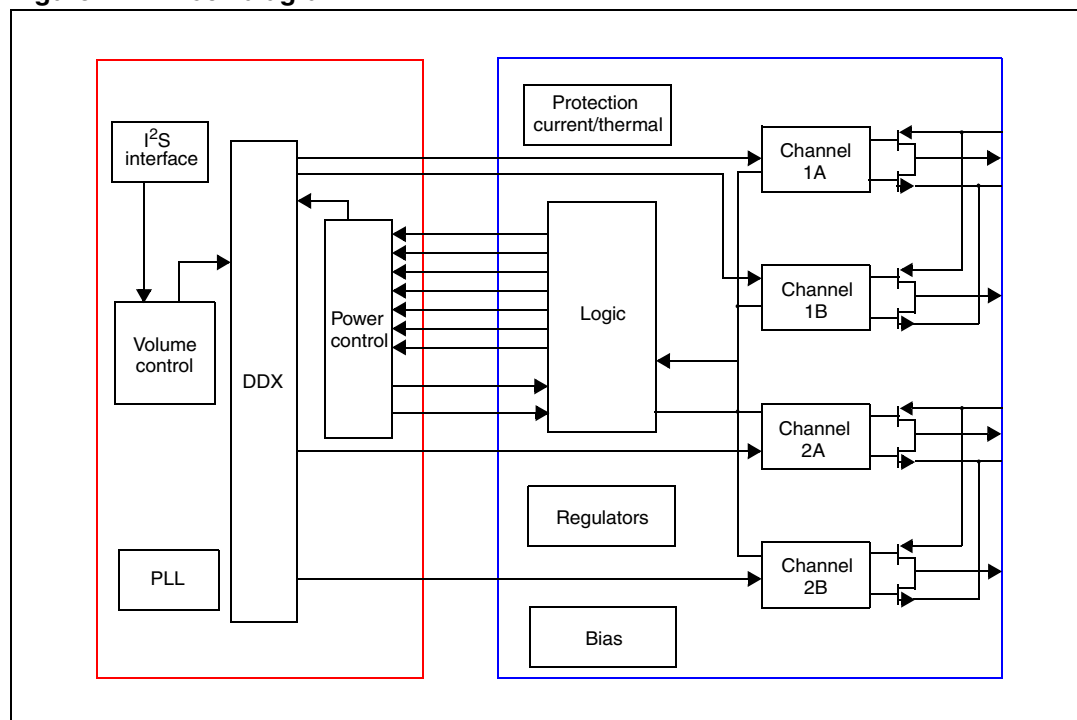


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# 1 Block diagram

Figure 1. Block diagram



## 2 Pin description

Figure 2. Pin connections (top view)

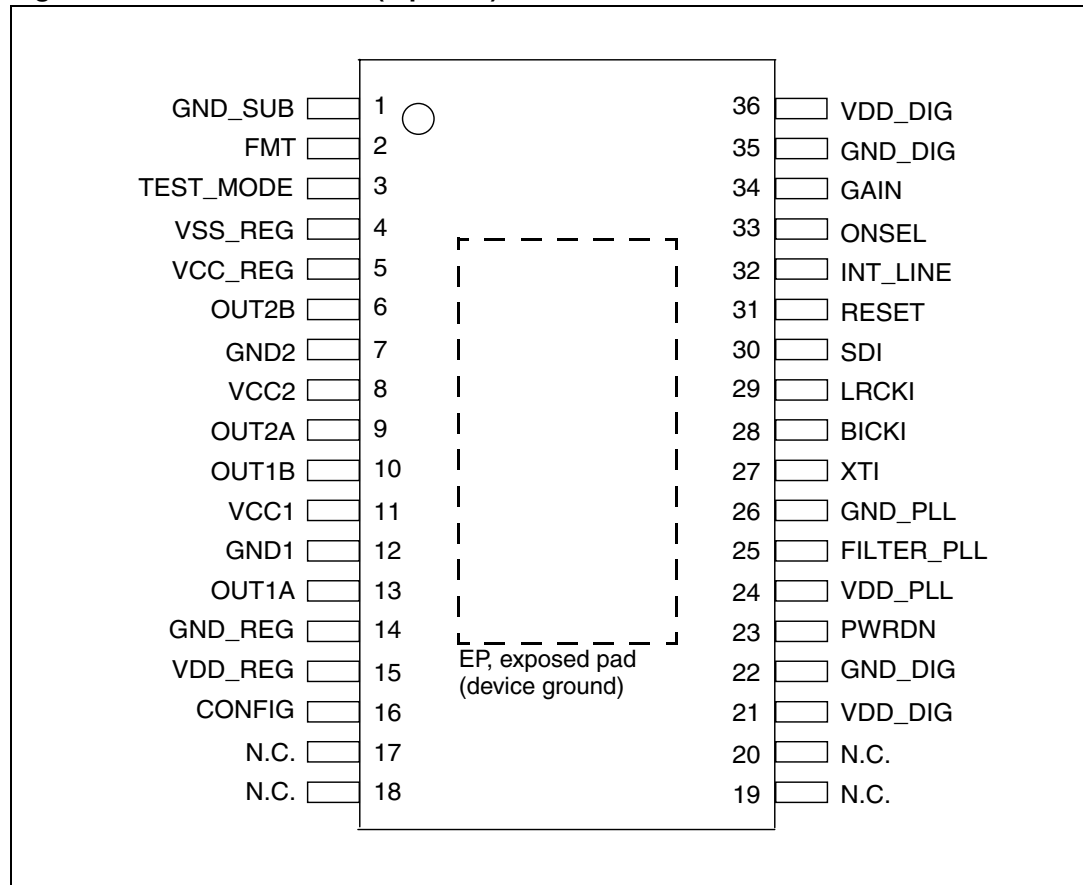


Table 2. Pin description

Pin	Name	Type	Description
1	GND_SUB	Gnd	Substrate ground
2	FMT	In	Serial format: 0: I <sup>2</sup> S format 1: left justified
3	TEST_MODE	In	This pin must be connected to GROUND
4	VSS_REG	Analog	Internal reference at V <sub>CC</sub> - 3.3 V
5	VCC_REG	Analog	Internal V <sub>CC</sub> reference
6	OUT2B	Out	Output half bridge 2B
7	GND2	Gnd	Power negative supply
8	VCC2	Power	Power positive supply
9	OUT2A	Out	Output half bridge 2A
10	OUT1B	Out	Output half bridge 1B

Table 2. Pin description (continued)

Pin	Name	Type	Description
11	VCC1	Power	Power positive supply
12	GND1	Gnd	Power negative supply
13	OUT1A	Out	Output half-bridge 1A
14	GND_REG	Analog	Internal ground reference
15	VDD_REG	Analog	Internal 3.3 V reference voltage
16	CONFIG	In	Configuration mode, must be connected to ground
17	N.C.	-	Not connected
18	N.C.	-	Not connected
19	N.C.	-	Not connected
20	N.C.	-	Not connected
21	VDD_DIG	Power	Positive supply digital
22	GND_DIG	Gnd	Digital ground
23	PWRDN	In	Power-down: 0: low-power mode 1: normal operation
24	VDD_PLL	Power	Positive supply for PLL
25	FILTER_PLL	In	Connection to PLL filter
26	GND_PLL	Gnd	Negative supply for PLL
27	XTI	In	PLL input clock, 256 * fs or 384 * fs
28	BICKI	In	I <sup>2</sup> S serial clock
29	LRCKI	In	I <sup>2</sup> S left/right clock
30	SDI	In	I <sup>2</sup> S serial data channel
31	RESET	In	Reset
32	INT_LINE	Out	Fault interrupt
33	ONSEL	In	Oversampling selector: 0: 256 * fs 1: 384 * fs
34	GAIN	In	Gain selector: 0: 0 dBFs 1: 24 dBFs
35	GND_DIG	Gnd	Digital ground
36	VDD_DIG	Power	Digital supply
-	EP	-	Exposed pad for PCB heatsink, to be connected to ground plane

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Power supply voltage (pins VCC1, VCC2)	-	-	23	V
V <sub>L</sub>	Logic input interface	-0.3	-	4	V
V <sub>DD</sub>	Digital supply (pin VDD_DIG)	-	-	4	V
T <sub>op</sub>	Operating junction temperature	0	-	150	°C
T <sub>stg</sub>	Storage temperature	-40	-	150	°C

### 3.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Min	Typ	Max	Unit
R <sub>Th(j-case)</sub>	Thermal resistance junction to case (thermal pad)	-	1.5	2	°C/W
T <sub>sd</sub>	Thermal shutdown junction temperature	140	-	150	°C
T <sub>hsd</sub>	Thermal shutdown hysteresis	18	20	22	°C

### 3.3 Recommended operating condition

**Table 5. Recommended operating condition**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Power supply voltage (pins VCC1, VCC2)	4.5	-	20.0	V
V <sub>L</sub>	Logic input interface	2.7	3.3	3.6	V
V <sub>DD</sub>	Digital supply (pin VDD_DIG)	2.7	3.3	3.6	V
T <sub>amb</sub>	Ambient temperature	0	-	70	°C

### 3.4 Electrical specifications - digital section

**Table 6. Electrical specifications for digital section**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{il}$	Input current without bias device	$V_i = 0\text{ V}$	-10	-	10	$\mu\text{A}$
$I_{ih}$		$V_i = V_{DD} = 3.6\text{ V}$	-10	-	10	$\mu\text{A}$
$V_{il}$	Low-level input voltage	-	-	-	$0.2 * V_{DD}$	V
$V_{ih}$	High-level input voltage	-	$0.8 * V_{DD}$	-	-	V
$V_{ol}$	Low-level output voltage	$I_{ol} = 2\text{ mA}$	-	-	$0.4 * V_{DD}$	V
$V_{oh}$	High-level output voltage	$I_{oh} = 2\text{ mA}$	$0.8 * V_{DD}$	-	-	V
$I_{pu}$	Pull-up/down current	-	-25	66	125	$\mu\text{A}$
$R_{pu}$	Equivalent pull-up/down resistance	-	-	50	-	$\text{k}\Omega$

### 3.5 Electrical specifications - power section

The specifications given here are with the operating conditions:  $V_{CC} = 18\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$ ,  $f_{sw} = 384\text{ kHz}$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$ ,  $R_L = 8\text{ }\Omega$  unless otherwise specified

**Table 7. Electrical specifications for power section**

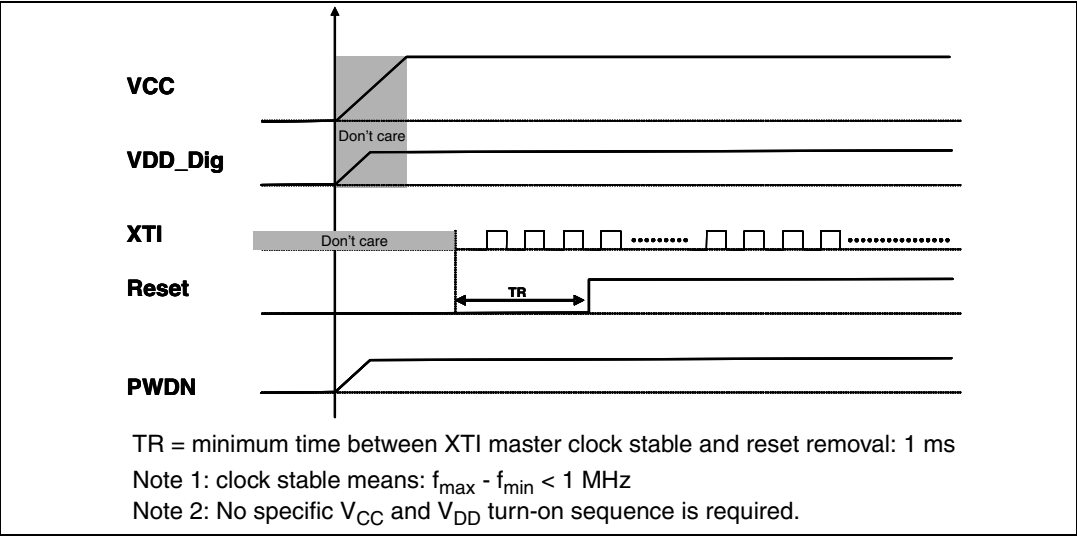
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_o$	Output power BTL	THD = 1%	-	16	-	W
		THD = 10%	-	20	-	
$R_{dsON}$	On resistance of power P-channel/N-channel MOSFET (total bridge)	$I_d = 1\text{ A}$	-	180	250	$\text{m}\Omega$
$I_{dss}$	Power P-channel/N-channel leakage current	-	-	-	10	$\mu\text{A}$
$g_P$	Power P-channel $R_{dsON}$ matching	$I_d = 1\text{ A}$	95	-	-	%
$g_N$	Power N-channel $R_{dsON}$ matching	$I_d = 1\text{ A}$	95	-	-	%
$I_{LDT}$	Low current dead time (static)	Resistive load <a href="#">Figure 4</a>	-	5	10	ns
$I_{HDT}$	High current dead time (dynamic)	Load = 1.5 A ( <a href="#">Figure 5</a> )	-	10	20	ns
$t_r$	Rise time	Resistive load <a href="#">Figure 4</a>	-	8	10	ns
$t_f$	Fall time	Resistive load <a href="#">Figure 4</a>	-	8	10	ns

**Table 7. Electrical specifications for power section** (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VCC}$	Supply current from $V_{CC}$ in power down	PWRDN = 0	0.03	0.06	0.2	mA
	Supply current from $V_{CC}$ in operation	PCM Input signal = -60 dBFs. Switching frequency = 384 kHz No LC filters	-	30	50	mA
$I_{VDD\_DIG}$	Supply current DDX processing (reference only)	Internal clock = 49.152 MHz	10	30	50	mA
	Supply current in standby	-	8	11	25	mA
$I_{SCP}$	short-circuit protection	Hi-Z output	2.7	3.8	5.0	A
UVL	Undervoltage protection threshold	-	-	3.5	4.3	V
$t_{min}$	Output minimum pulse width	No load	20	30	60	ns
DR	Dynamic range	-	-	100	-	dB
SNR	Signal-to-noise ratio	A-weighted	-	100	-	dB
THD+N	Total harmonic distortion + noise	$P_o = 1\text{ W}$ , $f = 1\text{ kHz}$	-	0.05	0.2	%
PSRR	Power supply rejection ratio	DDX stereo, <5 kHz Vripple = 1 V RMS Audio input = dither only	-	80	-	dB
$X_{TALK}$	Crosstalk	DDX stereo, <5 kHz One chan. driven at 1 W other channel measured	-	80	-	dB
$\eta$	Peak efficiency, DDX mode	$P_o = 2 \times 20\text{ W}$ into $8\ \Omega$	-	90	-	%
$f_{sw}$	PWM carrier frequency switching	-	-	384	-	kHz

3.6 Power-on sequence

Figure 3. Power-on sequence



3.7 Test circuits

Figure 4. Resistive load

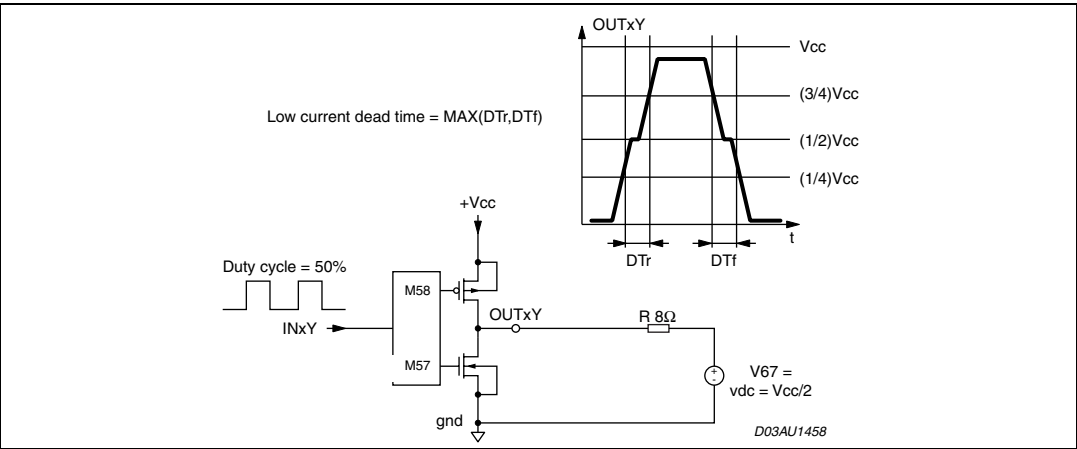
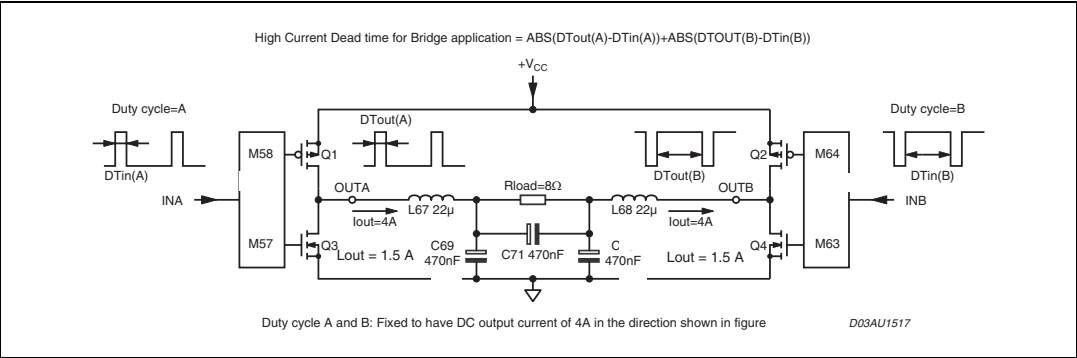


Figure 5. Test circuit





## 4 Functional description

### 4.1 Serial audio interface protocols

The STA333ML serial audio input interfaces with standard digital audio components and accepts serial data formats. The STA333ML always acts as a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using 3 input pins: left/right clock LRCKI (pin 29), serial clock BICKI (pin 28), and serial data SDI (pin 30).

The available formats are given in [Figure 6](#) and [Figure 7](#). Pin FMT (pin 2) selects the format such that FMT = logical 0 gives the I<sup>2</sup>S format and FMT = logical 1 gives the left-justified.

Figure 6. I<sup>2</sup>S

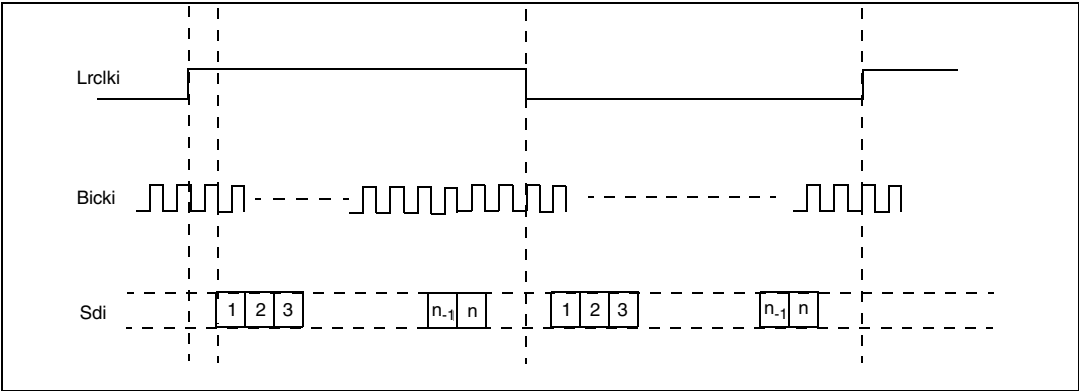
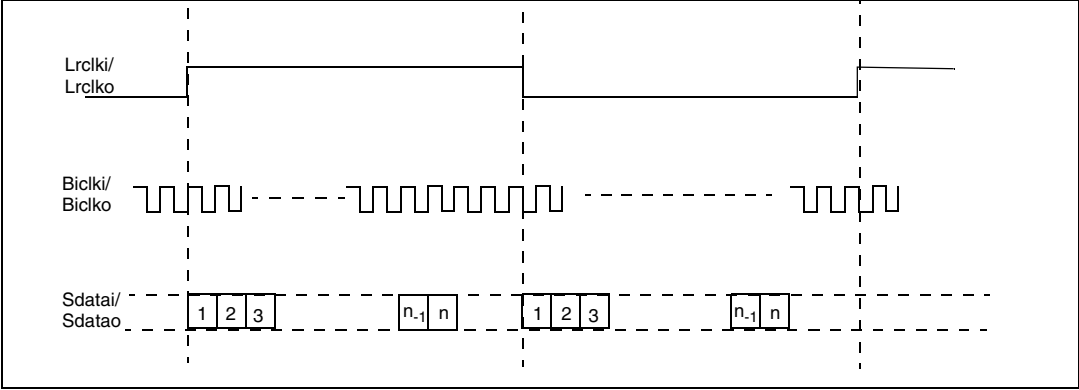


Figure 7. Left-justified



## 4.2 Fault-detect recovery bypass

The on-chip power output block provides feedback to the digital controller using inputs to the power control block. The fault input is used to indicate a fault condition (either overcurrent or thermal). When fault is asserted (set to 0), the power control block attempts a recovery from the fault by asserting the 3-state output (setting it to 0 which directs the power output block to begin recovery), holds it at 0 for 1 ms and then toggles it back to 1. This sequence is repeated for as long as the fault exists.

## 4.3 Zero-detect mute enable

If this function is enabled, the zero-detect circuit examines each processing channel to see if 2048 consecutive zero value samples (regardless of fs) are received. If so, the channel is muted.

## 4.4 Fade-in/out feature

The STA333ML has internal fade-in / fade-out feature when powered on or off, or after a fault condition.

## 4.5 Oversampling selector

Pin ONSEL (33) is used to configure the PLL to accept  $256 \cdot f_s$  or  $384 \cdot f_s$  master clock. Where  $f_s$  is the I<sup>2</sup>S LRCKI frequency:

ONSEL = logical 0 gives  $256 \cdot f_s$

ONSEL = logical 1 gives  $384 \cdot f_s$ .

## 4.6 Gain selector

Pin GAIN (34) is used to configure the STA333ML gain:

GAIN = logical 0 gives 0 dBfs

GAIN = logical 1 gives 24 dBfs.

## 4.7 Power-down function

Pin PWDN (23) is used to power down the STA333ML:

PWDN = logical 0 sets the power-down mode

PWDN = logical 1 gives normal operation.

If the power stage is switched off, then the PLL is also switched off.

It is possible to use the PWDN function as a mute function.

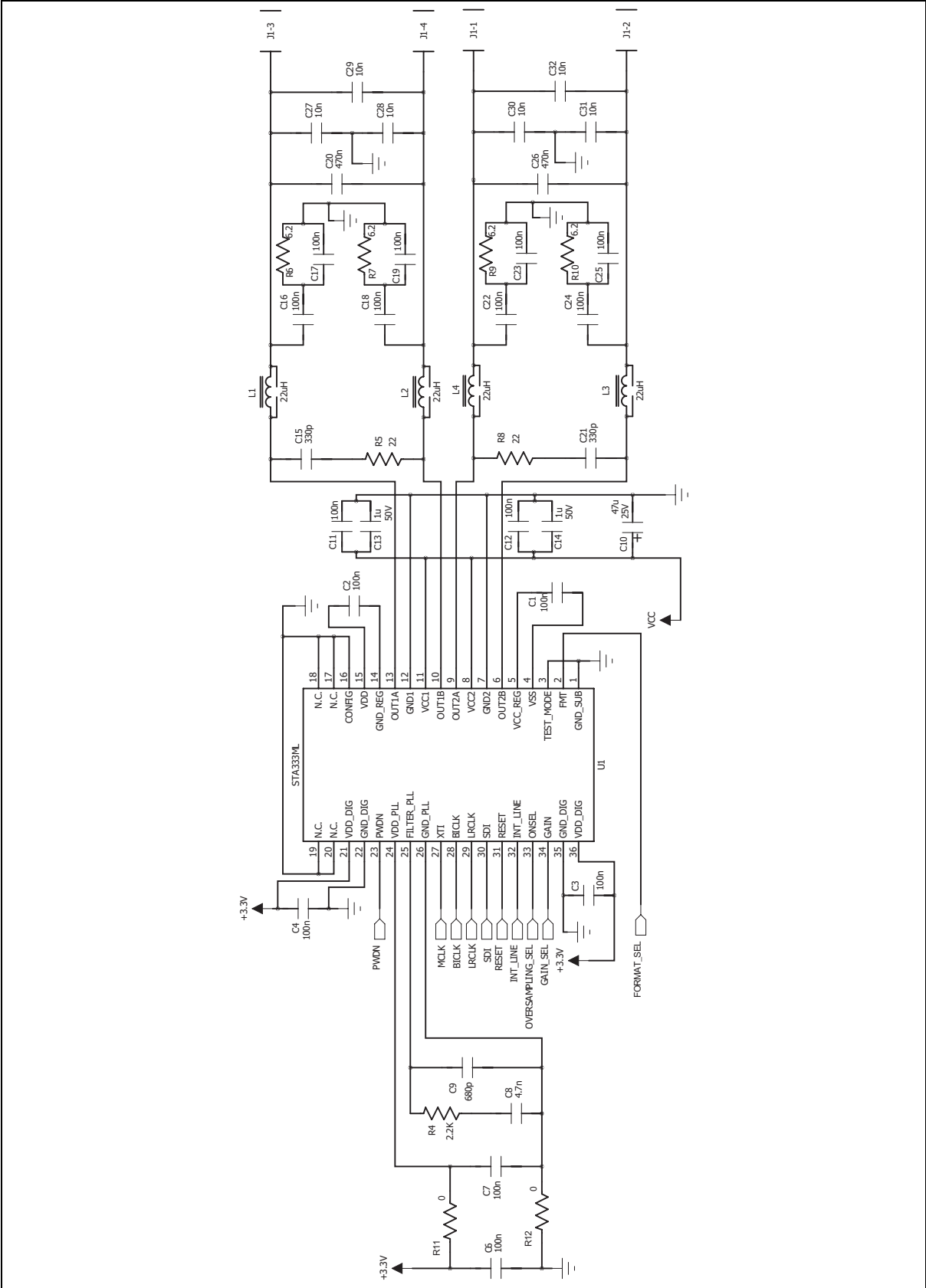
## 5 Applications

### 5.1 Applications schematic

*Figure 8 on page 13* shows the schematic of a typical application for the STA333ML.

Concerning the power supplies, take care when designing the PCB layout. In particular, the 3.3-Ω resistors on the digital supplies (VDD\_DIG) must be placed as close as possible to the device. This helps to prevent parasitic oscillation in the digital part of the device due to the inductive tracks of the PCB. The same rule applies for all the decoupling capacitors in order to limit any spikes on the supply pins.

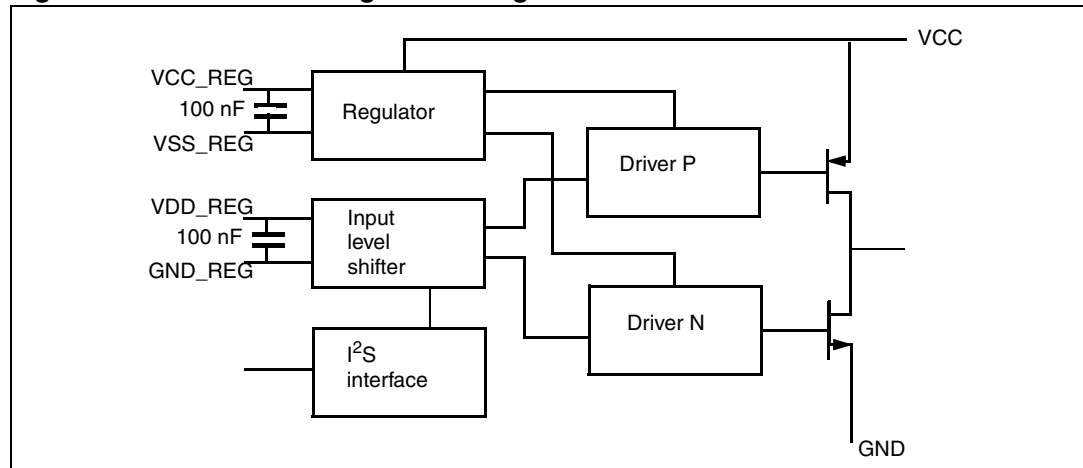
Figure 8. Application schematic



## 5.2 Internal voltage reference

An embedded voltage regulator produces the reference voltages for the DMOS bridge driver. It requires two 100 nF capacitors to keep the regulator stable. The capacitors should be placed close to the pins.

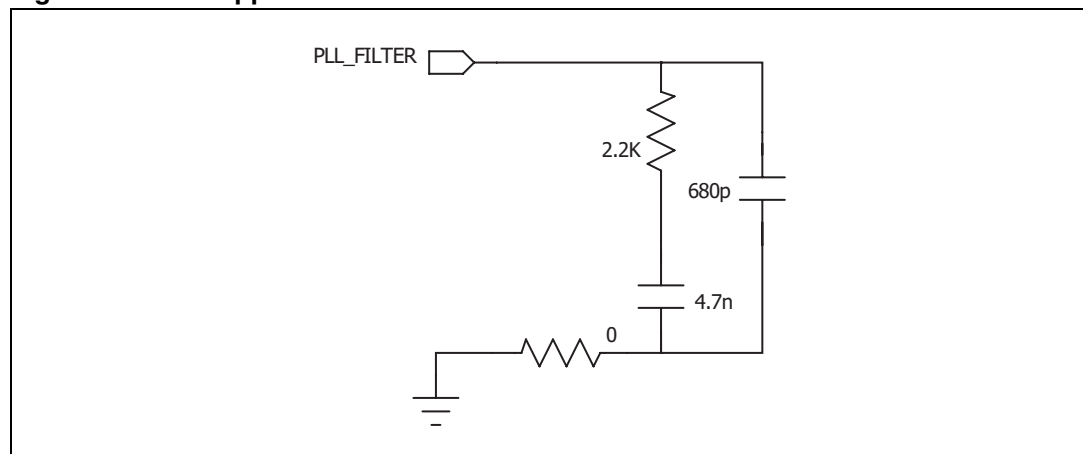
**Figure 9. Reference voltage block diagram**



## 5.3 PLL filter schematic

It is recommended to use the below scheme and values for the PLL loop filter to achieve the best performances from the device in general application. Please note that the ground of this filter scheme has to be connected to the ground of the PLL without any resistive path. Concerning the component values, please take into account that the greater the filter bandwidth, the less the lock time, but the higher the PLL output jitter.

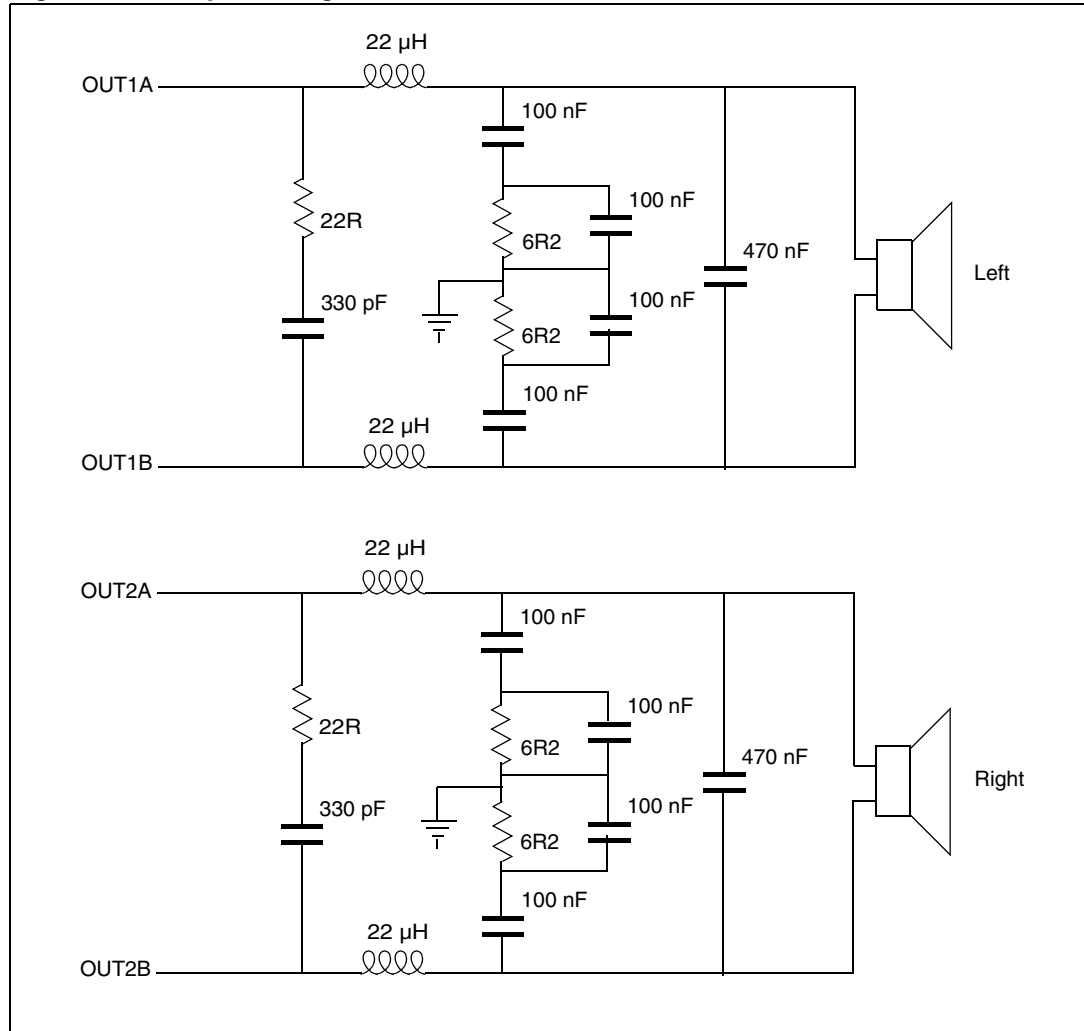
**Figure 10. PLL application schematic**

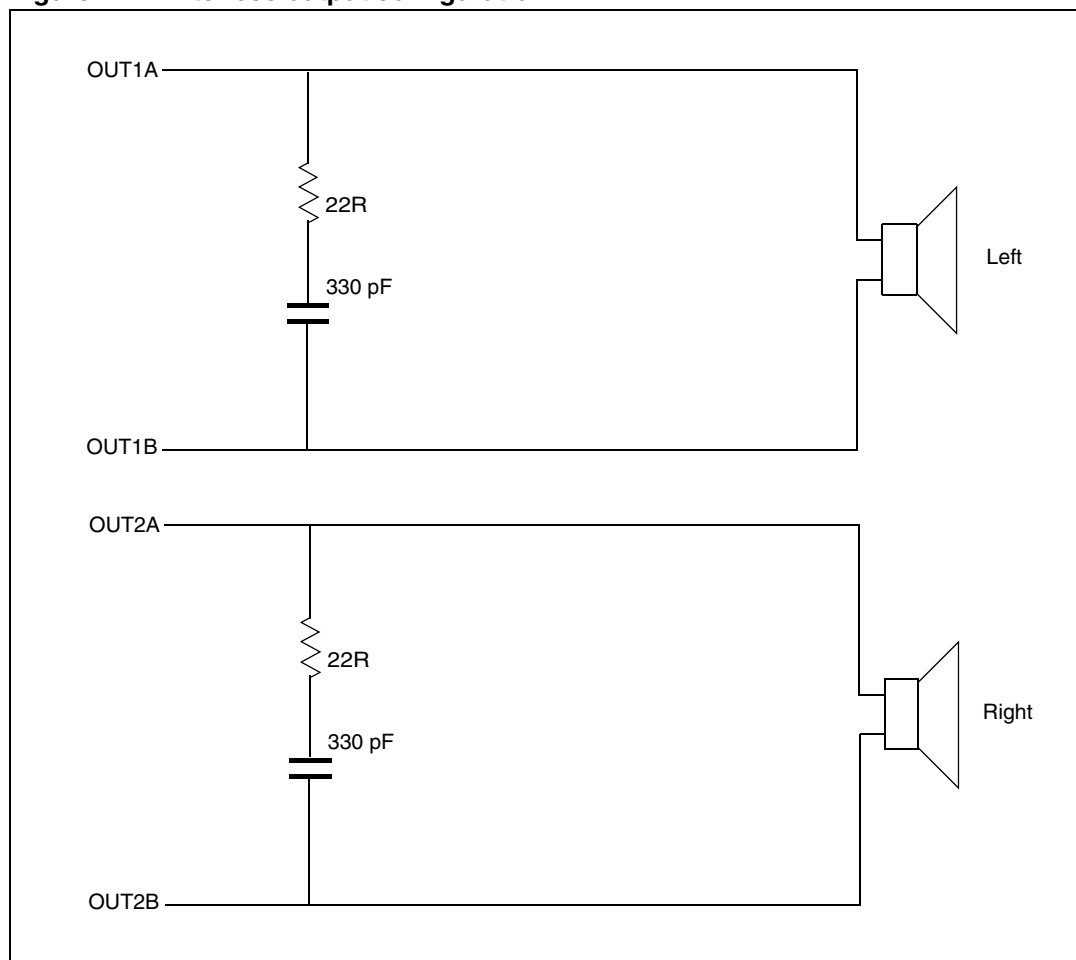


## 5.4 Typical output configuration

Figure 11 and Figure 12 show the typical output circuits used for the BTL stereo mode.

**Figure 11. Output configuration for stereo BTL mode**



**Figure 12. Filterless output configuration**

The filterless application is more critical in terms of EMI. It is quite important to follow the below suggestions:

- Tracks from amplifier to speaker should be as short as possible.
- Ferrite beads can be used (instead of coils) to improve EMI performance.
  - Ferrite beads must have a low impedance in the audio band and high impedance at high frequencies.
  - Place ferrite beads as close as possible to the IC.
  - Ferrite filters must reduce EMI above 1 MHz.
  - FCC and CE authorities test radiated emission above 30 MHz.

The presence of snubber networks reduce the EMI. The snubber networks should be placed as close as possible to the IC.

## 6 Package thermal characteristics

Using a double layer PCB the thermal resistance junction to ambient with 2 copper ground areas of  $3 \times 3 \text{ cm}^2$  and with 16 via holes (see [Figure 13](#)) is  $24 \text{ }^\circ\text{C/W}$  in natural air convection.

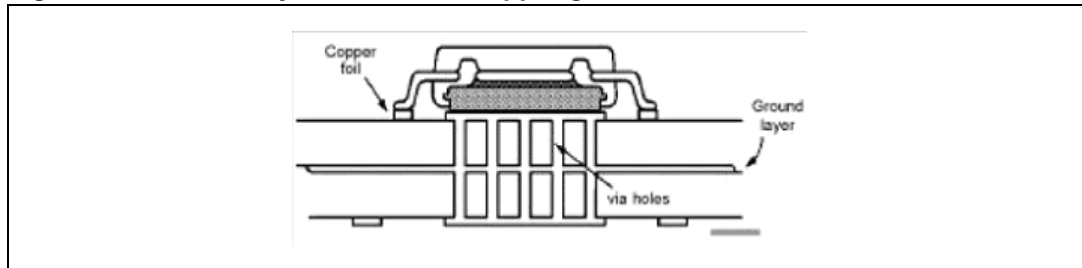
The dissipated power within the device depends primarily on the supply voltage, load impedance and output modulation level.

The max estimated dissipated power for the is:

$2 \times 20 \text{ W}$  into  $8 \text{ }\Omega$ , at  $18 \text{ V}$

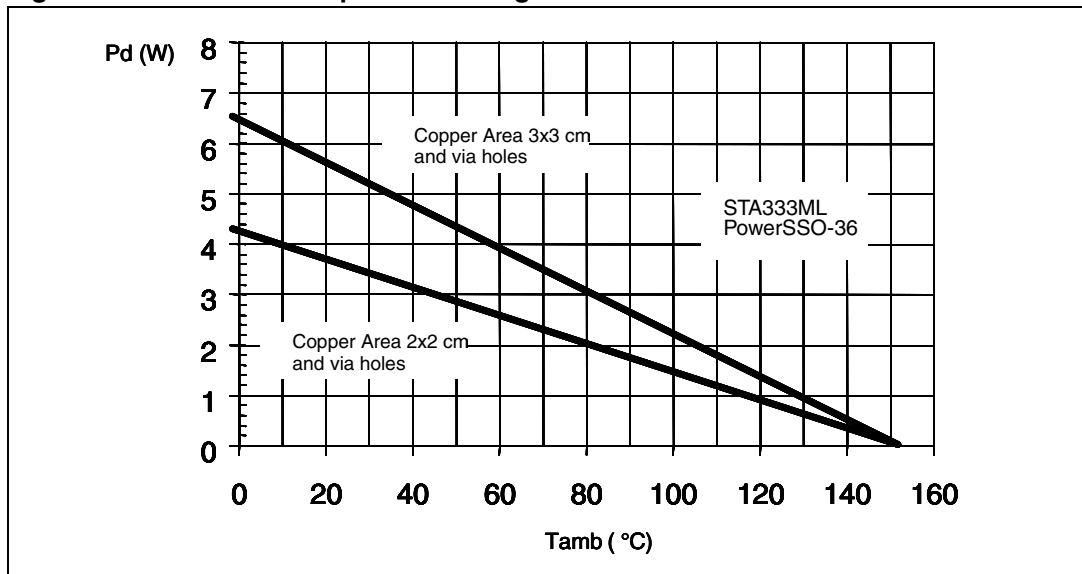
$P_d$  max is approximately  $4 \text{ W}$

**Figure 13. Double layer PCB with 2 copper ground areas and 16 via holes**



[Figure 14](#) shows the power derating curve for the PowerSSO-36 package on a board with two copper areas of  $2 \times 2 \text{ cm}^2$  and  $3 \times 3 \text{ cm}^2$ .

**Figure 14. PowerSSO-36 power derating curve**





# 7 Package mechanical data

Figure 15 shows the package outline and Table 8 gives the dimensions.

Figure 15. PowerSSO-36 EPD outline drawing

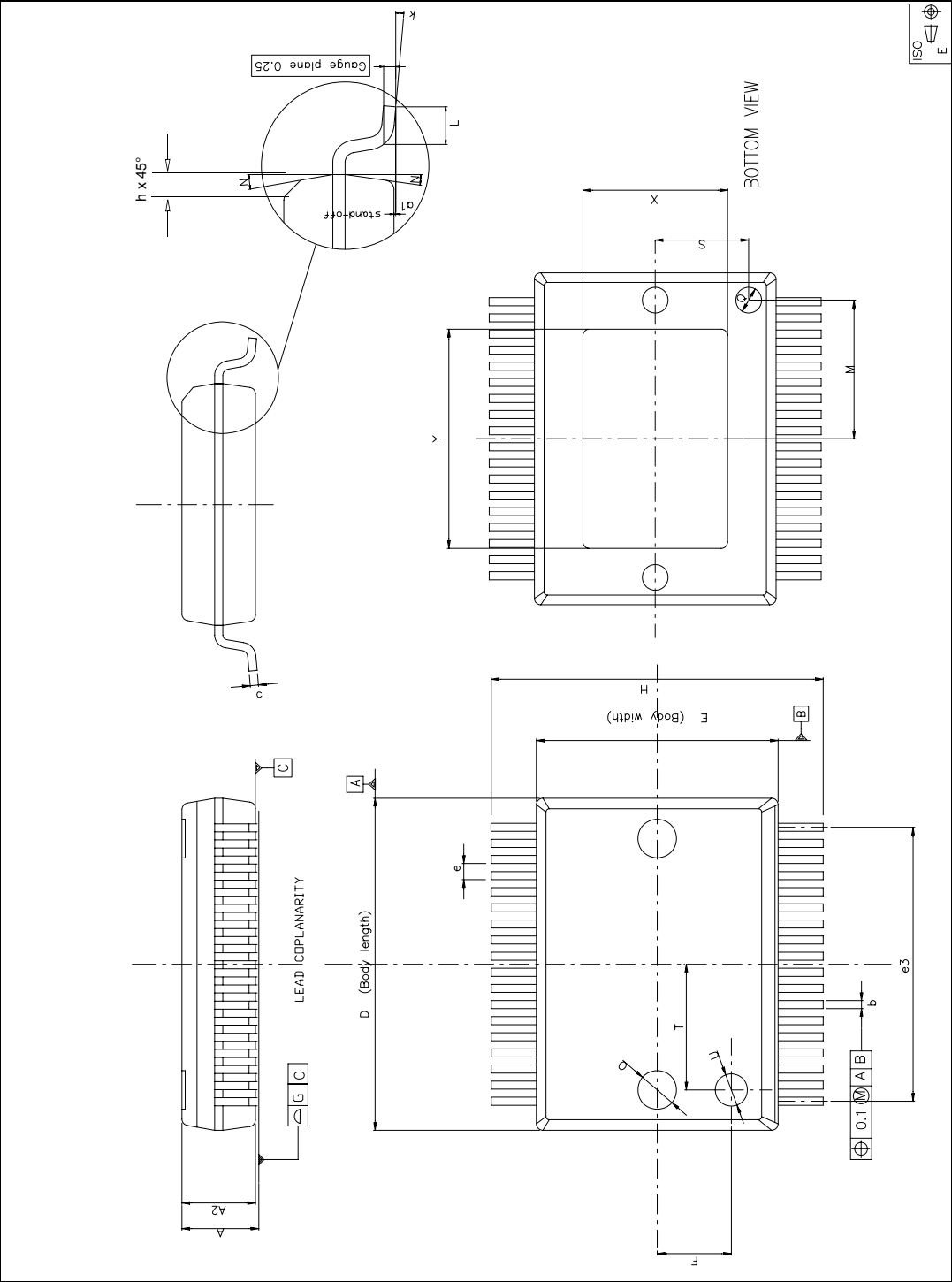


Table 8. PowerSSO-36 EPD dimensions

Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.47	0.085	-	0.097
A2	2.15	-	2.40	0.085	-	0.094
a1	0.00	-	0.10	0.00	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	0	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	4.90	-	7.10	0.193	-	0.280

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

## 8 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
1-Feb-2007	1	Initial release
2-May-2008	2	Package information update
4-Nov-2008	3	Added <a href="#">Table 6: Electrical specifications for digital section on page 7</a> Updated <a href="#">Table 7: Electrical specifications for power section on page 7</a> Added <a href="#">Section 3.6: Power-on sequence on page 9</a> Updated <a href="#">Chapter 4: Functional description on page 10</a> Added <a href="#">Chapter 5: Applications on page 12</a> Updated <a href="#">Chapter 6: Package thermal characteristics on page 17</a> .
28-Jan-2010	4	Updated supply voltage range in Features <a href="#">on page 1</a> Added package exposed pad to <a href="#">Figure 2</a> and <a href="#">Table 2: Pin description on page 4</a> Updated supply voltage range in <a href="#">Table 5: Recommended operating condition on page 6</a> Updated exposed pad Y dimension in <a href="#">Table 8: PowerSSO-36 EPD dimensions on page 19</a> .
3-Feb-2010	5	Updated junction temperature range in <a href="#">Table 3: Absolute maximum ratings on page 6</a> Removed max estimated dissipated power example <a href="#">on page 17</a>
05-Mar-2012	6	Updated <a href="#">Figure 8: Application schematic on page 13</a> Updated <a href="#">Figure 10: PLL application schematic on page 14</a> Removed reference to application note in <a href="#">Section 5.4: Typical output configuration</a> Minor textual updates

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