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# 1 Introduction

## 1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

## 1.2 Description

The MPC5604B/C is a family of next generation microcontrollers built on the Power Architecture® embedded category.

The MPC5604B/C family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

**Table 1. MPC5604B/C device comparison[1]**

| Feature | Device | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MPC5602BxLH | MPC5602BxLL | MPC5602BxLQ | MPC5602CxLH | MPC5602CxLL | MPC5603BxLH | MPC5603BxLL | MPC5603BxLQ | MPC5603CxLH | MPC5603CxLL | MPC5604BxLH | MPC5604BxLL | MPC5604BxLQ | MPC5604CxLH | MPC5604CxLL | MPC5604BxMG |
| CPU | e200z0h | | | | | | | | | | | | | | | |
| Execution speed[2] | Static – up to 64 MHz | | | | | | | | | | | | | | | |
| Code Flash | 256 KB | | | | | 384 KB | | | | | 512 KB | | | | | |
| Data Flash | 64 KB (4 × 16 KB) | | | | | | | | | | | | | | | |
| RAM | 24 KB | | | 32 KB | | 28 KB | | | 40 KB | | 32 KB | | | 48 KB | | |
| MPU | 8-entry | | | | | | | | | | | | | | | |
| ADC (10-bit) | 12 ch | 28 ch | 36 ch | 8 ch | 28 ch | 12 ch | 28 ch | 36 ch | 8 ch | 28 ch | 12 ch | 28 ch | 36 ch | 8 ch | 28 ch | 36 ch |
| CTU | Yes | | | | | | | | | | | | | | | |
| Total timer I/O[3] eMIOS | 12 ch, 16-bit | 28 ch, 16-bit | 56 ch, 16-bit | 12 ch, 16-bit | 28 ch, 16-bit | 12 ch, 16-bit | 28 ch, 16-bit | 56 ch, 16-bit | 12 ch, 16-bit | 28 ch, 16-bit | 12 ch, 16-bit | 28 ch, 16-bit | 56 ch, 16-bit | 12 ch, 16-bit | 28 ch, 16-bit | 56 ch, 16-bit |

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**Table 1. MPC5604B/C device comparison[1] (continued)**

| Feature | Device | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MPC5602BxLH | MPC5602BxLL | MPC5602BxLQ | MPC5602CxLH | MPC5602CxLL | MPC5603BxLH | MPC5603BxLL | MPC5603BxLQ | MPC5603CxLH | MPC5603CxLL | MPC5604BxLH | MPC5604BxLL | MPC5604BxLQ | MPC5604CxLH | MPC5604CxLL | MPC5604BxMG |
| • PWM + MC + IC/OC[4] | 2 ch | 5 ch | 10 ch | 2 ch | 5 ch | 2 ch | 5 ch | 10 ch | 2 ch | 5 ch | 2 ch | 5 ch | 10 ch | 2 ch | 5 ch | 10 ch |
| • PWM + IC/OC[4] | 10 ch | 20 ch | 40 ch | 10 ch | 20 ch | 10 ch | 20 ch | 40 ch | 10 ch | 20 ch | 10 ch | 20 ch | 40 ch | 10 ch | 20 ch | 40 ch |
| • IC/OC[4] | — | 3 ch | 6 ch | — | 3 ch | — | 3 ch | 6 ch | — | 3 ch | — | 3 ch | 6 ch | — | 3 ch | 6 ch |
| SCI (LINFlex) | 3[5] | | | 4 | | | | | | | | | | | | |
| SPI (DSPI) | 2 | 3 | | 2 | 3 | 2 | 3 | | 2 | 3 | 2 | 3 | | 2 | 3 | |
| CAN (FlexCAN) | 2[6] | | | 5 | 6 | 3[7] | | | 5 | 6 | 2[6] | 3[7] | | 5 | 6 | |
| $I^2C$ | 1 | | | | | | | | | | | | | | | |
| 32 kHz oscillator | Yes | | | | | | | | | | | | | | | |
| GPIO[8] | 45 | 79 | 123 | 45 | 79 | 45 | 79 | 123 | 45 | 79 | 45 | 79 | 123 | 45 | 79 | 123 |
| Debug | JTAG | | | | | | | | | | | | | | | Nexus2+ |
| Package | 64 LQFP | 100 LQFP | 144 LQFP | 64 LQFP | 100 LQFP | 64 LQFP | 100 LQFP | 144 LQFP | 64 LQFP | 100 LQFP | 64 LQFP | 100 LQFP | 144 LQFP | 64 LQFP | 100 LQFP | 208 MAPBGA[9] |

1 Feature set dependent on selected peripheral multiplexing—table shows example implementation.

2 Based on 125 °C ambient operating temperature.

3 See the eMIOS section of the device reference manual for information on the channel configuration and functions.

4 IC – Input Capture; OC – Output Compare; PWM – Pulse Width Modulation; MC – Modulus counter.

5 SCI0, SCI1 and SCI2 are available. SCI3 is not available.

6 CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.

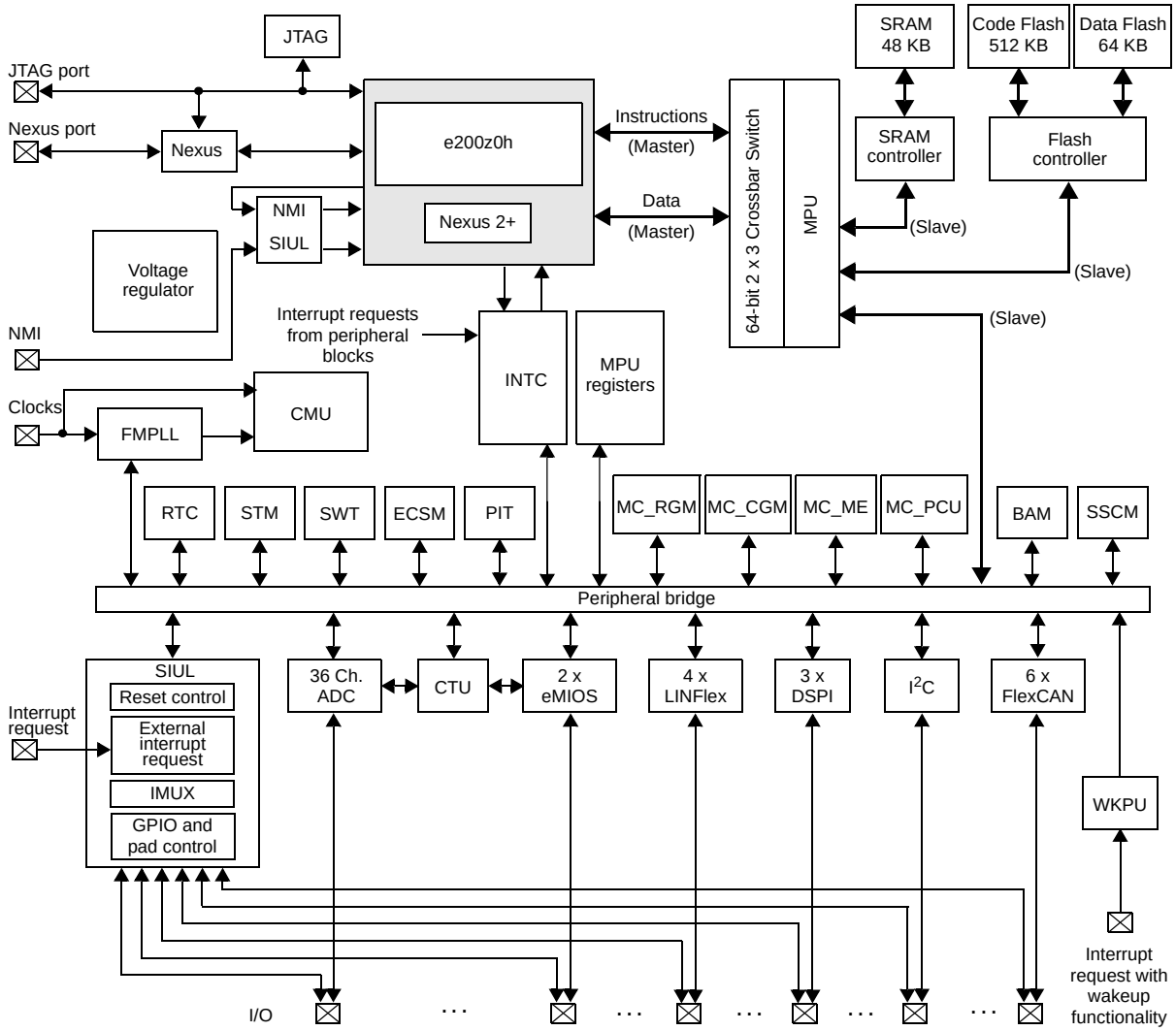
7 CAN0, CAN3 and either CAN1 or CAN4 are available. CAN2, CAN5 and CAN6 are not available

8 I/O count based on multiplexing with peripherals.

9 208 MAPBGA available only as development package for Nexus2+.

## Block diagram

Figure 1 shows a top-level block diagram of the MPC5604B/C device series.




Legend:

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| BAM | Boot Assist Module |
| FlexCAN | Controller Area Network |
| CMU | Clock Monitor Unit |
| CTU | Cross Triggering Unit |
| DSPI | Deserial Serial Peripheral Interface |
| eMIOS | Enhanced Modular Input Output System |
| FMPLL | Frequency-Modulated Phase-Locked Loop |
| $I^2C$ | Inter-integrated Circuit Bus |
| IMUX | Internal Multiplexer |
| INTC | Interrupt Controller |
| JTAG | JTAG controller |
| LINFlex | Serial Communication Interface (LIN support) |
| ECSM | Error Correction Status Module |
| MC_CGM | Clock Generation Module |
| MC_ME | Mode Entry Module |
| MC_PCU | Power Control Unit |
| MC_RGM | Reset Generation Module |
| MPU | Memory Protection Unit |
| Nexus | Nexus Development Interface (NDI) Level |
| NMI | Non-Maskable Interrupt |
| PIT | Periodic Interrupt Timer |
| RTC | Real-Time Clock |
| SIUL | System Integration Unit Lite |
| SRAM | Static Random-Access Memory |
| SSCM | System Status Configuration Module |
| STM | System Timer Module |
| SWT | Software Watchdog Timer |
| WKPU | Wakeup Unit |

**Figure 1. MPC5604B/C block diagram**

Table 2 summarizes the functions of all blocks present in the MPC5604B/C series of microcontrollers. Please note that the presence and number of blocks vary by device and package.



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**Table 2. MPC5604B/C series block summary**

| Block | Function |
|---|---|
| Analog-to-digital converter (ADC) | Multi-channel, 10-bit analog-to-digital converter |
| Boot assist module (BAM) | A block of read-only memory containing VLE code which is executed according to the boot mode of the device |
| Clock monitor unit (CMU) | Monitors clock source (internal and external) integrity |
| Cross triggering unit (CTU) | Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT |
| Deserial serial peripheral interface (DSPI) | Provides a synchronous serial interface for communication with external devices |
| Error Correction Status Module (ECSM) | Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes |
| Enhanced Direct Memory Access (eDMA) | Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels. |
| Enhanced modular input output system (eMIOS) | Provides the functionality to generate or measure events |
| Flash memory | Provides non-volatile storage for program code, constants and variables |
| FlexCAN (controller area network) | Supports the standard CAN communications protocol |
| Frequency-modulated phase-locked loop (FMPLL) | Generates high-speed system clocks and supports programmable frequency modulation |
| Internal multiplexer (IMUX) SIU subblock | Allows flexible mapping of peripheral interface on the different pins of the device |
| Inter-integrated circuit ($I^2C$™) bus | A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices |
| Interrupt controller (INTC) | Provides priority-based preemptive scheduling of interrupt requests |
| JTAG controller | Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode |
| LINFlex controller | Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load |
| Clock generation module (MC_CGM) | Provides logic and control required for the generation of system and peripheral clocks |
| Mode entry module (MC_ME) | Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications |
| Power control unit (MC_PCU) | Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU |
| Reset generation module (MC_RGM) | Centralizes reset sources and manages the device reset sequence of the device |
| Memory protection unit (MPU) | Provides hardware access control for all memory references generated in a device |



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**Table 2. MPC5604B/C series block summary (continued)**

| Block | Function |
|---|---|
| Nexus development interface (NDI) | Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard |
| Periodic interrupt timer (PIT) | Produces periodic interrupts and triggers |
| Real-time counter (RTC) | A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode) |
| System integration unit (SIU) | Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration |
| Static random-access memory (SRAM) | Provides storage for program code, constants, and variables |
| System status configuration module (SSCM) | Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable |
| System timer module (STM) | Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks |
| Software watchdog timer (SWT) | Provides protection from runaway code |
| Wakeup unit (WKPU) | The wakeup unit supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events. |
| Crossbar (XBAR) switch | Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width. |

# 2 Package pinouts and signal descriptions

## 2.1 Package pinouts

The available LQFP pinouts and the 208 MAPBGA ballmap are provided in the following figures. For pin signal descriptions, please refer to the device reference manual.



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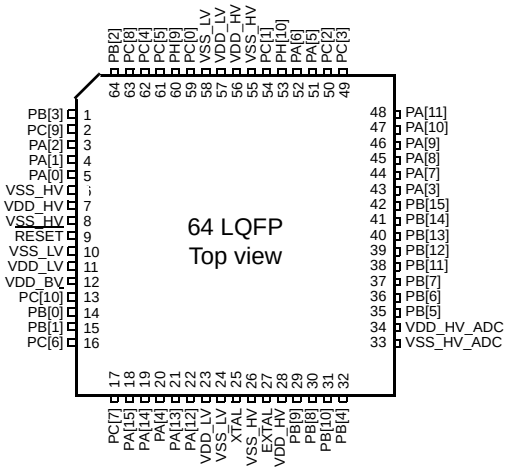


**Figure 2. MPC560xB LQFP 64-pin configuration**

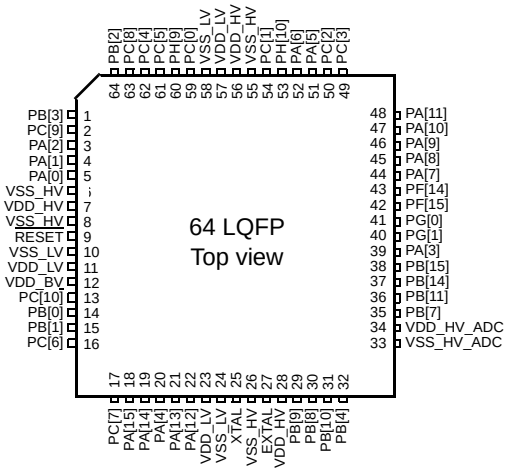


**Figure 3. MPC560xC LQFP 64-pin configuration**



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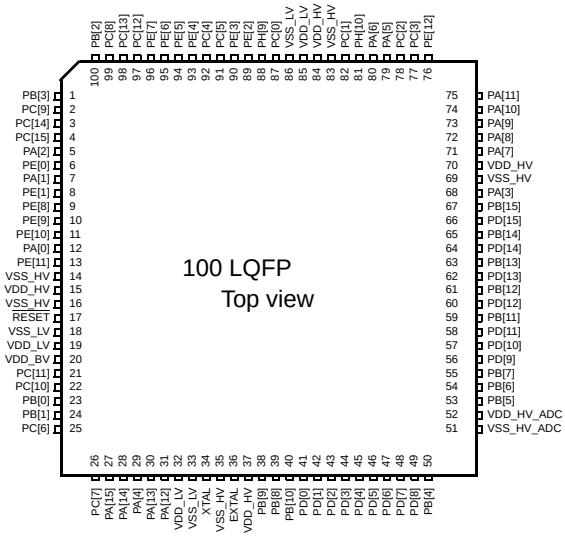


Note:
Availability of port pin alternate functions depends on product selection.

**Figure 4. LQFP 100-pin configuration**



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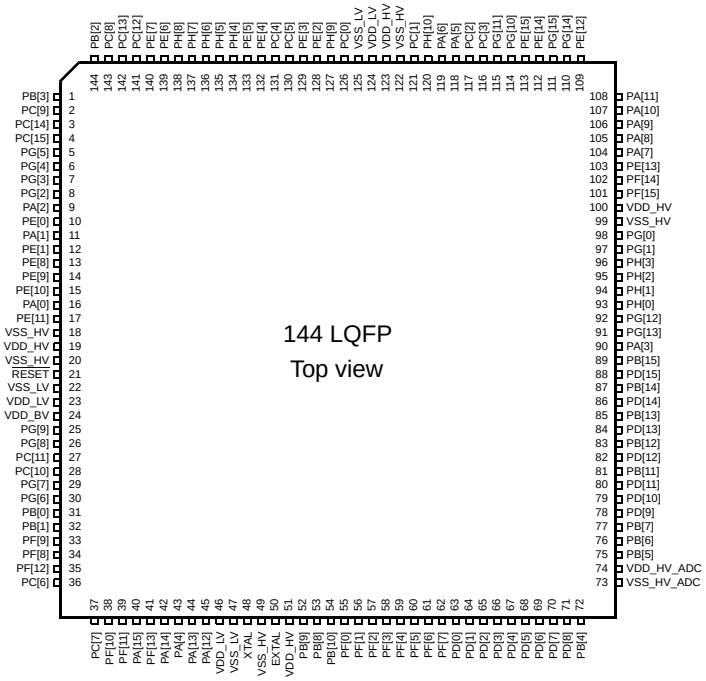


Note:
Availability of port pin alternate functions depends on product selection.

**Figure 5. LQFP 144-pin configuration**



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| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | PC[8] | PC[13] | NC | NC | PH[8] | PH[4] | PC[5] | PC[0] | NC | NC | PC[2] | NC | PE[15] | NC | NC | NC | A |
| B | PC[9] | PB[2] | NC | PC[12] | PE[6] | PH[5] | PC[4] | PH[9] | PH[10] | NC | PC[3] | PG[11] | PG[15] | PG[14] | PA[11] | PA[10] | B |
| C | PC[14] | VDD_HV | PB[3] | PE[7] | PH[7] | PE[5] | PE[3] | VSS_LV | PC[1] | NC | PA[5] | NC | PE[14] | PE[12] | PA[9] | PA[8] | C |
| D | NC | NC | PC[15] | NC | PH[6] | PE[4] | PE[2] | VDD_LV | VDD_HV | NC | PA[6] | NC | PG[10] | PF[14] | PE[13] | PA[7] | D |
| E | PG[4] | PG[5] | PG[3] | PG[2] | | | | | | | | | PG[1] | PG[0] | PF[15] | VDD_HV | E |
| F | PE[0] | PA[2] | PA[1] | PE[1] | | | | | | | | | PH[0] | PH[1] | PH[3] | PH[2] | F |
| G | PE[9] | PE[8] | PE[10] | PA[0] | | | VSS_HV | VSS_HV | VSS_HV | VSS_HV | | | VDD_HV | NC | NC | MSEO | G |
| H | VSS_HV | PE[11] | VDD_HV | NC | | | VSS_HV | VSS_HV | VSS_HV | VSS_HV | | | MDO3 | MDO2 | MDO0 | MDO1 | H |
| J | RESET | VSS_LV | NC | NC | | | VSS_HV | VSS_HV | VSS_HV | VSS_HV | | | NC | NC | NC | NC | J |
| K | EVTI | NC | VDD_BV | VDD_LV | | | VSS_HV | VSS_HV | VSS_HV | VSS_HV | | | NC | PG[12] | PA[3] | PG[13] | K |
| L | PG[9] | PG[8] | NC | EVTO | | | | | | | | | PB[15] | PD[15] | PD[14] | PB[14] | L |
| M | PG[7] | PG[6] | PC[10] | PC[11] | | | | | | | | | PB[13] | PD[13] | PD[12] | PB[12] | M |
| N | PB[1] | PF[9] | PB[0] | NC | NC | PA[4] | VSS_LV | EXTAL | VDD_HV | PF[0] | PF[4] | NC | PB[11] | PD[10] | PD[9] | PD[11] | N |
| P | PF[8] | NC | PC[7] | NC | NC | PA[14] | VDD_LV | XTAL | PB[10] | PF[1] | PF[5] | PD[0] | PD[3] | VDD_HV_ADC | PB[6] | PB[7] | P |
| R | PF[12] | PC[6] | PF[10] | PF[11] | VDD_HV | PA[15] | PA[13] | NC | OSC32K_XTAL | PF[3] | PF[7] | PD[2] | PD[4] | PD[7] | VSS_HV_ADC | PB[5] | R |
| T | NC | NC | NC | MCKO | NC | PF[13] | PA[12] | NC | OSC32K_EXTAL | PF[2] | PF[6] | PD[1] | PD[5] | PD[6] | PD[8] | PB[4] | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

Note: 208 MAPBGA available only as development package for Nexus 2+.

NC = Not connected

**Figure 6. 208 MAPBGA configuration**

## 2.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up whilst TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.



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- Nexus output pads (MDO[*n*], MCKO, EVTO, MSEO) are forced to output.

## 2.3 Voltage supply pins

Voltage supply pins are used to provide power to the device. Three dedicated VDD_LV/VSS_LV supply pairs are used for 1.2 V regulator stabilization.

**Table 3. Voltage supply pin descriptions**

| Port pin | Function | Pin number | | | |
|---|---|---|---|---|---|
| | | 64 LQFP[1] | 100 LQFP | 144 LQFP | 208 MAPBGA[2] |
| VDD_HV | Digital supply voltage | 7, 28, 56 | 15, 37, 70, 84 | 19, 51, 100, 123 | C2, D9, E16, G13, H3, N9, R5 |
| VSS_HV | Digital ground | 6, 8, 26, 55 | 14, 16, 35, 69, 83 | 18, 20, 49, 99, 122 | G7, G8, G9, G10, H1, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10 |
| VDD_LV | 1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV}$ pin.[3] | 11, 23, 57 | 19, 32, 85 | 23, 46, 124 | D8, K4, P7 |
| VSS_LV | 1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV}$ pin.[3] | 10, 24, 58 | 18, 33, 86 | 22, 47, 125 | C8, J2, N7 |
| VDD_BV | Internal regulator supply voltage | 12 | 20 | 24 | K3 |
| VSS_HV_ADC | Reference ground and analog ground for the ADC | 33 | 51 | 73 | R15 |
| VDD_HV_ADC | Reference voltage and analog supply for the ADC | 34 | 52 | 74 | P14 |

1 Pin numbers apply to both the MPC560xB and MPC560xC packages.

2 208 MAPBGA available only as development package for Nexus2+

3 A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet for details).

## 2.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[1]
M = Medium[1 2]
F = Fast[1 2]
I = Input only with analog feature[1]
J = Input/Output ('S' pad) with analog feature
X = Oscillator

1. See the I/O pad electrical characteristics in the device datasheet for details.
2. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see PCR.SRC in section Pad Configuration Registers (PCR0–PCR122) in the device reference manual).



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## 2.5 System pins

The system pins are listed in Table 4.

**Table 4. System pin descriptions**

| System pin | Function | I/O direction | Pad type | RESET configuration | Pin number | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | 64 LQFP[1] | 100 LQFP | 144 LQFP | 208 MAPBGA[2] |
| $\overline{\text{RESET}}$ | Bidirectional reset with Schmitt-Trigger characteristics and noise filter. | I/O | M | Input, weak pull-up only after PHASE2 | 9 | 17 | 21 | J1 |
| EXTAL | Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode.<br>Analog input for the clock generator when the oscillator is in bypass mode.[3] | I/O | X | Tristate | 27 | 36 | 50 | N8 |
| XTAL | Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.[3] | I | X | Tristate | 25 | 34 | 48 | P8 |

1 Pin numbers apply to both the MPC560xB and MPC560xC packages.

2 208 MAPBGA available only as development package for Nexus2+

3 See the relevant section of the datasheet

## 2.6 Functional ports

The functional port pins are listed in Table 5.

**Table 5. Functional port pin descriptions**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PA[0] | PCR[0] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[0]<br>E0UC[0]<br>CLKOUT<br>—<br>WKPU[19][4] | SIUL<br>eMIOS_0<br>CGL<br>—<br>WKPU | I/O<br>I/O<br>O<br>—<br>I | M | Tristate | 5 | 5 | 12 | 16 | G4 |
| PA[1] | PCR[1] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[1]<br>E0UC[1]<br>—<br>—<br>NMI[5]<br>WKPU[2][4] | SIUL<br>eMIOS_0<br>—<br>—<br>WKPU<br>WKPU | I/O<br>I/O<br>—<br>—<br>I<br>I | S | Tristate | 4 | 4 | 7 | 11 | F3 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PA[2] | PCR[2] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[2]<br>E0UC[2]<br>—<br>—<br>WKPU[3][4] | SIUL<br>eMIOS_0<br>—<br>—<br>WKPU | I/O<br>I/O<br>—<br>—<br>I | S | Tristate | 3 | 3 | 5 | 9 | F2 |
| PA[3] | PCR[3] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[3]<br>E0UC[3]<br>—<br>—<br>EIRQ[0] | SIUL<br>eMIOS_0<br>—<br>—<br>SIUL | I/O<br>I/O<br>—<br>—<br>I | S | Tristate | 43 | 39 | 68 | 90 | K15 |
| PA[4] | PCR[4] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[4]<br>E0UC[4]<br>—<br>—<br>WKPU[9][4] | SIUL<br>eMIOS_0<br>—<br>—<br>WKPU | I/O<br>I/O<br>—<br>—<br>I | S | Tristate | 20 | 20 | 29 | 43 | N6 |
| PA[5] | PCR[5] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[5]<br>E0UC[5]<br>—<br>— | SIUL<br>eMIOS_0<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | 51 | 51 | 79 | 118 | C11 |
| PA[6] | PCR[6] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[6]<br>E0UC[6]<br>—<br>—<br>EIRQ[1] | SIUL<br>eMIOS_0<br>—<br>—<br>SIUL | I/O<br>I/O<br>—<br>—<br>I | S | Tristate | 52 | 52 | 80 | 119 | D11 |
| PA[7] | PCR[7] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[7]<br>E0UC[7]<br>LIN3TX<br>—<br>EIRQ[2] | SIUL<br>eMIOS_0<br>LINFlex_3<br>—<br>SIUL | I/O<br>I/O<br>O<br>—<br>I | S | Tristate | 44 | 44 | 71 | 104 | D16 |
| PA[8] | PCR[8] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>N/A[6]<br>— | GPIO[8]<br>E0UC[8]<br>—<br>—<br>EIRQ[3]<br>ABS[0]<br>LIN3RX | SIUL<br>eMIOS_0<br>—<br>—<br>SIUL<br>BAM<br>LINFlex_3 | I/O<br>I/O<br>—<br>—<br>I<br>I<br>I | S | Input, weak pull-up | 45 | 45 | 72 | 105 | C16 |
| PA[9] | PCR[9] | AF0<br>AF1<br>AF2<br>AF3<br>N/A[6] | GPIO[9]<br>E0UC[9]<br>—<br>—<br>FAB | SIUL<br>eMIOS_0<br>—<br>—<br>BAM | I/O<br>I/O<br>—<br>—<br>I | S | Pull-down | 46 | 46 | 73 | 106 | C15 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PA[10] | PCR[10] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[10]<br>E0UC[10]<br>SDA<br>— | SIUL<br>eMIOS_0<br>I2C_0<br>— | I/O<br>I/O<br>I/O<br>— | S | Tristate | 47 | 47 | 74 | 107 | B16 |
| PA[11] | PCR[11] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[11]<br>E0UC[11]<br>SCL<br>— | SIUL<br>eMIOS_0<br>I2C_0<br>— | I/O<br>I/O<br>I/O<br>— | S | Tristate | 48 | 48 | 75 | 108 | B15 |
| PA[12] | PCR[12] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[12]<br>—<br>—<br>—<br>SIN_0 | SIUL<br>—<br>—<br>—<br>DSPI0 | I/O<br>—<br>—<br>—<br>I | S | Tristate | 22 | 22 | 31 | 45 | T7 |
| PA[13] | PCR[13] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[13]<br>SOUT_0<br>—<br>— | SIUL<br>DSPI_0<br>—<br>— | I/O<br>O<br>—<br>— | M | Tristate | 21 | 21 | 30 | 44 | R7 |
| PA[14] | PCR[14] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[14]<br>SCK_0<br>CS0_0<br>—<br>EIRQ[4] | SIUL<br>DSPI_0<br>DSPI_0<br>—<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>I | M | Tristate | 19 | 19 | 28 | 42 | P6 |
| PA[15] | PCR[15] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[15]<br>CS0_0<br>SCK_0<br>—<br>WKPU[10][4] | SIUL<br>DSPI_0<br>DSPI_0<br>—<br>WKPU | I/O<br>I/O<br>I/O<br>—<br>I | M | Tristate | 18 | 18 | 27 | 40 | R6 |
| PB[0] | PCR[16] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[16]<br>CAN0TX<br>—<br>— | SIUL<br>FlexCAN_0<br>—<br>— | I/O<br>O<br>—<br>— | M | Tristate | 14 | 14 | 23 | 31 | N3 |
| PB[1] | PCR[17] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[17]<br>—<br>—<br>—<br>WKPU[4][4]<br>CAN0RX | SIUL<br>—<br>—<br>—<br>WKPU<br>FlexCAN_0 | I/O<br>—<br>—<br>—<br>I<br>I | S | Tristate | 15 | 15 | 24 | 32 | N1 |
| PB[2] | PCR[18] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[18]<br>LIN0TX<br>SDA<br>— | SIUL<br>LINFlex_0<br>I2C_0<br>— | I/O<br>O<br>I/O<br>— | M | Tristate | 64 | 64 | 100 | 144 | B2 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PB[3] | PCR[19] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[19]<br>—<br>SCL<br>—<br>WKPU[11][4]<br>LIN0RX | SIUL<br>—<br>I2C_0<br>—<br>WKPU<br>LINFlex_0 | I/O<br>—<br>I/O<br>—<br>I<br>I | S | Tristate | 1 | 1 | 1 | 1 | C3 |
| PB[4] | PCR[20] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[20]<br>—<br>—<br>—<br>GPI[0] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | 32 | 32 | 50 | 72 | T16 |
| PB[5] | PCR[21] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[21]<br>—<br>—<br>—<br>GPI[1] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | 35 | — | 53 | 75 | R16 |
| PB[6] | PCR[22] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[22]<br>—<br>—<br>—<br>GPI[2] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | 36 | — | 54 | 76 | P15 |
| PB[7] | PCR[23] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[23]<br>—<br>—<br>—<br>GPI[3] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | 37 | 35 | 55 | 77 | P16 |
| PB[8] | PCR[24] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[24]<br>—<br>—<br>—<br>ANS[0]<br>OSC32K_XTAL[7] | SIUL<br>—<br>—<br>—<br>ADC<br>SXOSC | I<br>—<br>—<br>—<br>I<br>I/O | I | Tristate | 30 | 30 | 39 | 53 | R9 |
| PB[9] | PCR[25] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[25]<br>—<br>—<br>—<br>ANS[1]<br>OSC32K_EXTAL[7] | SIUL<br>—<br>—<br>—<br>ADC<br>SXOSC | I<br>—<br>—<br>—<br>I<br>I/O | I | Tristate | 29 | 29 | 38 | 52 | T9 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PB[10] | PCR[26] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[26]<br>—<br>—<br>—<br>ANS[2]<br>WKPU[8][4] | SIUL<br>—<br>—<br>—<br>ADC<br>WKPU | I/O<br>—<br>—<br>—<br>I<br>I | J | Tristate | 31 | 31 | 40 | 54 | P9 |
| PB[11][8] | PCR[27] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[27]<br>E0UC[3]<br>—<br>CS0_0<br>ANS[3] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC | I/O<br>I/O<br>—<br>I/O<br>I | J | Tristate | 38 | 36 | 59 | 81 | N13 |
| PB[12] | PCR[28] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[28]<br>E0UC[4]<br>—<br>CS1_0<br>ANX[0] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC | I/O<br>I/O<br>—<br>O<br>I | J | Tristate | 39 | — | 61 | 83 | M16 |
| PB[13] | PCR[29] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[29]<br>E0UC[5]<br>—<br>CS2_0<br>ANX[1] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC | I/O<br>I/O<br>—<br>O<br>I | J | Tristate | 40 | — | 63 | 85 | M13 |
| PB[14] | PCR[30] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[30]<br>E0UC[6]<br>—<br>CS3_0<br>ANX[2] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC | I/O<br>I/O<br>—<br>O<br>I | J | Tristate | 41 | 37 | 65 | 87 | L16 |
| PB[15] | PCR[31] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[31]<br>E0UC[7]<br>—<br>CS4_0<br>ANX[3] | SIUL<br>eMIOS_0<br>—<br>DSPI_0<br>ADC | I/O<br>I/O<br>—<br>O<br>I | J | Tristate | 42 | 38 | 67 | 89 | L13 |
| PC[0][9] | PCR[32] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[32]<br>—<br>TDI<br>— | SIUL<br>—<br>JTAGC<br>— | I/O<br>—<br>I<br>— | M | Input, weak pull-up | 59 | 59 | 87 | 126 | A8 |
| PC[1][9] | PCR[33] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[33]<br>—<br>TDO[10]<br>— | SIUL<br>—<br>JTAGC<br>— | I/O<br>—<br>O<br>— | M | Tristate | 54 | 54 | 82 | 121 | C9 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PC[2] | PCR[34] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[34]<br>SCK_1<br>CAN4TX[11]<br>—<br>EIRQ[5] | SIUL<br>DSPI_1<br>FlexCAN_4<br>—<br>SIUL | I/O<br>I/O<br>O<br>—<br>I | M | Tristate | 50 | 50 | 78 | 117 | A11 |
| PC[3] | PCR[35] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[35]<br>CS0_1<br>MA[0]<br>—<br>CAN1RX<br>CAN4RX[11]<br>EIRQ[6] | SIUL<br>DSPI_1<br>ADC<br>—<br>FlexCAN_1<br>FlexCAN_4<br>SIUL | I/O<br>I/O<br>O<br>—<br>I<br>I<br>I | S | Tristate | 49 | 49 | 77 | 116 | B11 |
| PC[4] | PCR[36] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[36]<br>—<br>—<br>—<br>SIN_1<br>CAN3RX[11] | SIUL<br>—<br>—<br>—<br>DSPI_1<br>FlexCAN_3 | I/O<br>—<br>—<br>—<br>I<br>I | M | Tristate | 62 | 62 | 92 | 131 | B7 |
| PC[5] | PCR[37] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[37]<br>SOUT_1<br>CAN3TX[11]<br>—<br>EIRQ[7] | SIUL<br>DSPI1<br>FlexCAN_3<br>—<br>SIUL | I/O<br>O<br>O<br>—<br>I | M | Tristate | 61 | 61 | 91 | 130 | A7 |
| PC[6] | PCR[38] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[38]<br>LIN1TX<br>—<br>— | SIUL<br>LINFlex_1<br>—<br>— | I/O<br>O<br>—<br>— | S | Tristate | 16 | 16 | 25 | 36 | R2 |
| PC[7] | PCR[39] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[39]<br>—<br>—<br>—<br>LIN1RX<br>WKPU[12][4] | SIUL<br>—<br>—<br>—<br>LINFlex_1<br>WKPU | I/O<br>—<br>—<br>—<br>I<br>I | S | Tristate | 17 | 17 | 26 | 37 | P3 |
| PC[8] | PCR[40] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[40]<br>LIN2TX<br>—<br>— | SIUL<br>LINFlex_2<br>—<br>— | I/O<br>O<br>—<br>— | S | Tristate | 63 | 63 | 99 | 143 | A1 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PC[9] | PCR[41] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[41]<br>—<br>—<br>—<br>LIN2RX<br>WKPU[13][4] | SIUL<br>—<br>—<br>—<br>LINFlex_2<br>WKPU | I/O<br>—<br>—<br>—<br>I<br>I | S | Tristate | 2 | 2 | 2 | 2 | B1 |
| PC[10] | PCR[42] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[42]<br>CAN1TX<br>CAN4TX[11]<br>MA[1] | SIUL<br>FlexCAN_1<br>FlexCAN_4<br>ADC | I/O<br>O<br>O<br>O | M | Tristate | 13 | 13 | 22 | 28 | M3 |
| PC[11] | PCR[43] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[43]<br>—<br>—<br>—<br>CAN1RX<br>CAN4RX[11]<br>WKPU[5][4] | SIUL<br>—<br>—<br>—<br>FlexCAN_1<br>FlexCAN_4<br>WKPU | I/O<br>—<br>—<br>—<br>I<br>I<br>I | S | Tristate | — | — | 21 | 27 | M4 |
| PC[12] | PCR[44] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[44]<br>E0UC[12]<br>—<br>—<br>SIN_2 | SIUL<br>eMIOS_0<br>—<br>—<br>DSPI_2 | I/O<br>I/O<br>—<br>—<br>I | M | Tristate | — | — | 97 | 141 | B4 |
| PC[13] | PCR[45] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[45]<br>E0UC[13]<br>SOUT_2<br>— | SIUL<br>eMIOS_0<br>DSPI_2<br>— | I/O<br>I/O<br>O<br>— | S | Tristate | — | — | 98 | 142 | A2 |
| PC[14] | PCR[46] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[46]<br>E0UC[14]<br>SCK_2<br>—<br>EIRQ[8] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>I | S | Tristate | — | — | 3 | 3 | C1 |
| PC[15] | PCR[47] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[47]<br>E0UC[15]<br>CS0_2<br>— | SIUL<br>eMIOS_0<br>DSPI_2<br>— | I/O<br>I/O<br>I/O<br>— | M | Tristate | — | — | 4 | 4 | D3 |
| PD[0] | PCR[48] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[48]<br>—<br>—<br>—<br>GPI[4] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 41 | 63 | P12 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PD[1] | PCR[49] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[49]<br>—<br>—<br>—<br>GPI[5] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 42 | 64 | T12 |
| PD[2] | PCR[50] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[50]<br>—<br>—<br>—<br>GPI[6] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 43 | 65 | R12 |
| PD[3] | PCR[51] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[51]<br>—<br>—<br>—<br>GPI[7] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 44 | 66 | P13 |
| PD[4] | PCR[52] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[52]<br>—<br>—<br>—<br>GPI[8] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 45 | 67 | R13 |
| PD[5] | PCR[53] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[53]<br>—<br>—<br>—<br>GPI[9] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 46 | 68 | T13 |
| PD[6] | PCR[54] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[54]<br>—<br>—<br>—<br>GPI[10] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 47 | 69 | T14 |
| PD[7] | PCR[55] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[55]<br>—<br>—<br>—<br>GPI[11] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 48 | 70 | R14 |
| PD[8] | PCR[56] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[56]<br>—<br>—<br>—<br>GPI[12] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 49 | 71 | T15 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PD[9] | PCR[57] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[57]<br>—<br>—<br>—<br>GPI[13] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 56 | 78 | N15 |
| PD[10] | PCR[58] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[58]<br>—<br>—<br>—<br>GPI[14] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 57 | 79 | N14 |
| PD[11] | PCR[59] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[59]<br>—<br>—<br>—<br>GPI[15] | SIUL<br>—<br>—<br>—<br>ADC | I<br>—<br>—<br>—<br>I | I | Tristate | — | — | 58 | 80 | N16 |
| PD[12][8] | PCR[60] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[60]<br>CS5_0<br>E0UC[24]<br>—<br>ANS[4] | SIUL<br>DSPI_0<br>eMIOS_0<br>—<br>ADC | I/O<br>O<br>I/O<br>—<br>I | J | Tristate | — | — | 60 | 82 | M15 |
| PD[13] | PCR[61] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[61]<br>CS0_1<br>E0UC[25]<br>—<br>ANS[5] | SIUL<br>DSPI_1<br>eMIOS_0<br>—<br>ADC | I/O<br>I/O<br>I/O<br>—<br>I | J | Tristate | — | — | 62 | 84 | M14 |
| PD[14] | PCR[62] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[62]<br>CS1_1<br>E0UC[26]<br>—<br>ANS[6] | SIUL<br>DSPI_1<br>eMIOS_0<br>—<br>ADC | I/O<br>O<br>I/O<br>—<br>I | J | Tristate | — | — | 64 | 86 | L15 |
| PD[15] | PCR[63] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[63]<br>CS2_1<br>E0UC[27]<br>—<br>ANS[7] | SIUL<br>DSPI_1<br>eMIOS_0<br>—<br>ADC | I/O<br>O<br>I/O<br>—<br>I | J | Tristate | — | — | 66 | 88 | L14 |
| PE[0] | PCR[64] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[64]<br>E0UC[16]<br>—<br>—<br>CAN5RX[11]<br>WKPU[6][4] | SIUL<br>eMIOS_0<br>—<br>—<br>FlexCAN_5<br>WKPU | I/O<br>I/O<br>—<br>—<br>I<br>I | S | Tristate | — | — | 6 | 10 | F1 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PE[1] | PCR[65] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[65]<br>E0UC[17]<br>CAN5TX[11]<br>— | SIUL<br>eMIOS_0<br>FlexCAN_5<br>— | I/O<br>I/O<br>O<br>— | M | Tristate | — | — | 8 | 12 | F4 |
| PE[2] | PCR[66] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[66]<br>E0UC[18]<br>—<br>—<br>SIN_1 | SIUL<br>eMIOS_0<br>—<br>—<br>DSPI_1 | I/O<br>I/O<br>—<br>—<br>I | M | Tristate | — | — | 89 | 128 | D7 |
| PE[3] | PCR[67] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[67]<br>E0UC[19]<br>SOUT_1<br>— | SIUL<br>eMIOS_0<br>DSPI_1<br>— | I/O<br>I/O<br>O<br>— | M | Tristate | — | — | 90 | 129 | C7 |
| PE[4] | PCR[68] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[68]<br>E0UC[20]<br>SCK_1<br>—<br>EIRQ[9] | SIUL<br>eMIOS_0<br>DSPI_1<br>—<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>I | M | Tristate | — | — | 93 | 132 | D6 |
| PE[5] | PCR[69] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[69]<br>E0UC[21]<br>CS0_1<br>MA[2] | SIUL<br>eMIOS_0<br>DSPI_1<br>ADC | I/O<br>I/O<br>I/O<br>O | M | Tristate | — | — | 94 | 133 | C6 |
| PE[6] | PCR[70] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[70]<br>E0UC[22]<br>CS3_0<br>MA[1] | SIUL<br>eMIOS_0<br>DSPI_0<br>ADC | I/O<br>I/O<br>O<br>O | M | Tristate | — | — | 95 | 139 | B5 |
| PE[7] | PCR[71] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[71]<br>E0UC[23]<br>CS2_0<br>MA[0] | SIUL<br>eMIOS_0<br>DSPI_0<br>ADC | I/O<br>I/O<br>O<br>O | M | Tristate | — | — | 96 | 140 | C4 |
| PE[8] | PCR[72] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[72]<br>CAN2TX[12]<br>E0UC[22]<br>CAN3TX[11] | SIUL<br>FlexCAN_2<br>eMIOS_0<br>FlexCAN_3 | I/O<br>O<br>I/O<br>O | M | Tristate | — | — | 9 | 13 | G2 |
| PE[9] | PCR[73] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[73]<br>—<br>E0UC[23]<br>—<br>WKPU[7][4]<br>CAN2RX[12]<br>CAN3RX[11] | SIUL<br>—<br>eMIOS_0<br>—<br>WKPU<br>FlexCAN_2<br>FlexCAN_3 | I/O<br>—<br>I/O<br>—<br>I<br>I<br>I | S | Tristate | — | — | 10 | 14 | G1 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PE[10] | PCR[74] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[74]<br>LIN3TX<br>CS3_1<br>—<br>EIRQ[10] | SIUL<br>LINFlex_3<br>DSPI_1<br>—<br>SIUL | I/O<br>O<br>O<br>—<br>I | S | Tristate | — | — | 11 | 15 | G3 |
| PE[11] | PCR[75] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[75]<br>—<br>CS4_1<br>—<br>LIN3RX<br>WKPU[14][4] | SIUL<br>—<br>DSPI_1<br>—<br>LINFlex_3<br>WKPU | I/O<br>—<br>O<br>—<br>I<br>I | S | Tristate | — | — | 13 | 17 | H2 |
| PE[12] | PCR[76] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[76]<br>—<br>E1UC[19][13]<br>—<br>SIN_2<br>EIRQ[11] | SIUL<br>—<br>eMIOS_1<br>—<br>DSPI_2<br>SIUL | I/O<br>—<br>I/O<br>—<br>I<br>I | S | Tristate | — | — | 76 | 109 | C14 |
| PE[13] | PCR[77] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[77]<br>SOUT2<br>E1UC[20]<br>— | SIUL<br>DSPI_2<br>eMIOS_1<br>— | I/O<br>O<br>I/O<br>— | S | Tristate | — | — | — | 103 | D15 |
| PE[14] | PCR[78] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[78]<br>SCK_2<br>E1UC[21]<br>—<br>EIRQ[12] | SIUL<br>DSPI_2<br>eMIOS_1<br>—<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>I | S | Tristate | — | — | — | 112 | C13 |
| PE[15] | PCR[79] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[79]<br>CS0_2<br>E1UC[22]<br>— | SIUL<br>DSPI_2<br>eMIOS_1<br>— | I/O<br>I/O<br>I/O<br>— | M | Tristate | — | — | — | 113 | A13 |
| PF[0] | PCR[80] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[80]<br>E0UC[10]<br>CS3_1<br>—<br>ANS[8] | SIUL<br>eMIOS_0<br>DSPI_1<br>—<br>ADC | I/O<br>I/O<br>O<br>—<br>I | J | Tristate | — | — | — | 55 | N10 |
| PF[1] | PCR[81] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[81]<br>E0UC[11]<br>CS4_1<br>—<br>ANS[9] | SIUL<br>eMIOS_0<br>DSPI_1<br>—<br>I | I/O<br>I/O<br>O<br>—<br>I | J | Tristate | — | — | — | 56 | P10 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PF[2] | PCR[82] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[82]<br>E0UC[12]<br>CS0_2<br>—<br>ANS[10] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>ADC | I/O<br>I/O<br>I/O<br>—<br>I | J | Tristate | — | — | — | 57 | T10 |
| PF[3] | PCR[83] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[83]<br>E0UC[13]<br>CS1_2<br>—<br>ANS[11] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>ADC | I/O<br>I/O<br>O<br>—<br>I | J | Tristate | — | — | — | 58 | R10 |
| PF[4] | PCR[84] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[84]<br>E0UC[14]<br>CS2_2<br>—<br>ANS[12] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>ADC | I/O<br>I/O<br>O<br>—<br>I | J | Tristate | — | — | — | 59 | N11 |
| PF[5] | PCR[85] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[85]<br>E0UC[22]<br>CS3_2<br>—<br>ANS[13] | SIUL<br>eMIOS_0<br>DSPI_2<br>—<br>ADC | I/O<br>I/O<br>O<br>—<br>I | J | Tristate | — | — | — | 60 | P11 |
| PF[6] | PCR[86] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[86]<br>E0UC[23]<br>—<br>—<br>ANS[14] | SIUL<br>eMIOS_0<br>—<br>—<br>ADC | I/O<br>I/O<br>—<br>—<br>I | J | Tristate | — | — | — | 61 | T11 |
| PF[7] | PCR[87] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[87]<br>—<br>—<br>—<br>ANS[15] | SIUL<br>—<br>—<br>—<br>ADC | I/O<br>—<br>—<br>—<br>I | J | Tristate | — | — | — | 62 | R11 |
| PF[8] | PCR[88] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[88]<br>CAN3TX[14]<br>CS4_0<br>CAN2TX[15] | SIUL<br>FlexCAN_3<br>DSPI_0<br>FlexCAN_2 | I/O<br>O<br>O<br>O | M | Tristate | — | — | — | 34 | P1 |
| PF[9] | PCR[89] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[89]<br>—<br>CS5_0<br>—<br>CAN2RX[15]<br>CAN3RX[14] | SIUL<br>—<br>DSPI_0<br>—<br>FlexCAN_2<br>FlexCAN_3 | I/O<br>—<br>O<br>—<br>I<br>I | S | Tristate | — | — | — | 33 | N2 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PF[10] | PCR[90] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[90]<br>—<br>—<br>— | SIUL<br>—<br>—<br>— | I/O<br>—<br>—<br>— | M | Tristate | — | — | — | 38 | R3 |
| PF[11] | PCR[91] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[91]<br>—<br>—<br>—<br>WKPU[15][4] | SIUL<br>—<br>—<br>—<br>WKPU | I/O<br>—<br>—<br>—<br>I | S | Tristate | — | — | — | 39 | R4 |
| PF[12] | PCR[92] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[92]<br>E1UC[25]<br>—<br>— | SIUL<br>eMIOS_1<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 35 | R1 |
| PF[13] | PCR[93] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[93]<br>E1UC[26]<br>—<br>—<br>WKPU[16][4] | SIUL<br>eMIOS_1<br>—<br>—<br>WKPU | I/O<br>I/O<br>—<br>—<br>I | S | Tristate | — | — | — | 41 | T6 |
| PF[14] | PCR[94] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[94]<br>CAN4TX[11]<br>E1UC[27]<br>CAN1TX | SIUL<br>FlexCAN_4<br>eMIOS_1<br>FlexCAN_4 | I/O<br>O<br>I/O<br>O | M | Tristate | — | 43 | — | 102 | D14 |
| PF[15] | PCR[95] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>—<br>— | GPIO[95]<br>—<br>—<br>—<br>CAN1RX<br>CAN4RX[11]<br>EIRQ[13] | SIUL<br>—<br>—<br>—<br>FlexCAN_1<br>FlexCAN_4<br>SIUL | I/O<br>—<br>—<br>—<br>I<br>I<br>I | S | Tristate | — | 42 | — | 101 | E15 |
| PG[0] | PCR[96] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[96]<br>CAN5TX[11]<br>E1UC[23]<br>— | SIUL<br>FlexCAN_5<br>eMIOS_1<br>— | I/O<br>O<br>I/O<br>— | M | Tristate | — | 41 | — | 98 | E14 |
| PG[1] | PCR[97] | AF0<br>AF1<br>AF2<br>AF3<br>—<br>— | GPIO[97]<br>—<br>E1UC[24]<br>—<br>CAN5RX[11]<br>EIRQ[14] | SIUL<br>—<br>eMIOS_1<br>—<br>FlexCAN_5<br>SIUL | I/O<br>—<br>I/O<br>—<br>I<br>I | S | Tristate | — | 40 | — | 97 | E13 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PG[2] | PCR[98] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[98]<br>E1UC[11]<br>—<br>— | SIUL<br>eMIOS_1<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 8 | E4 |
| PG[3] | PCR[99] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[99]<br>E1UC[12]<br>—<br>—<br>WKPU[17][4] | SIUL<br>eMIOS_1<br>—<br>—<br>WKPU | I/O<br>I/O<br>—<br>—<br>I | S | Tristate | — | — | — | 7 | E3 |
| PG[4] | PCR[100] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[100]<br>E1UC[13]<br>—<br>— | SIUL<br>eMIOS_1<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 6 | E1 |
| PG[5] | PCR[101] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[101]<br>E1UC[14]<br>—<br>—<br>WKPU[18][4] | SIUL<br>eMIOS_1<br>—<br>—<br>WKPU | I/O<br>I/O<br>—<br>—<br>I | S | Tristate | — | — | — | 5 | E2 |
| PG[6] | PCR[102] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[102]<br>E1UC[15]<br>—<br>— | SIUL<br>eMIOS_1<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 30 | M2 |
| PG[7] | PCR[103] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[103]<br>E1UC[16]<br>—<br>— | SIUL<br>eMIOS_1<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 29 | M1 |
| PG[8] | PCR[104] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[104]<br>E1UC[17]<br>—<br>CS0_2<br>EIRQ[15] | SIUL<br>eMIOS_1<br>—<br>DSPI_2<br>SIUL | I/O<br>I/O<br>—<br>I/O<br>I | S | Tristate | — | — | — | 26 | L2 |
| PG[9] | PCR[105] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[105]<br>E1UC[18]<br>—<br>SCK_2 | SIUL<br>eMIOS_1<br>—<br>DSPI_2 | I/O<br>I/O<br>—<br>I/O | S | Tristate | — | — | — | 25 | L1 |
| PG[10] | PCR[106] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[106]<br>E0UC[24]<br>—<br>— | SIUL<br>eMIOS_0<br>—<br>— | I/O<br>I/O<br>—<br>— | S | Tristate | — | — | — | 114 | D13 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PG[11] | PCR[107] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[107]<br>E0UC[25]<br>—<br>— | SIUL<br>eMIOS_0<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 115 | B12 |
| PG[12] | PCR[108] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[108]<br>E0UC[26]<br>—<br>— | SIUL<br>eMIOS_0<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 92 | K14 |
| PG[13] | PCR[109] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[109]<br>E0UC[27]<br>—<br>— | SIUL<br>eMIOS_0<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 91 | K16 |
| PG[14] | PCR[110] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[110]<br>E1UC[0]<br>—<br>— | SIUL<br>eMIOS_1<br>—<br>— | I/O<br>I/O<br>—<br>— | S | Tristate | — | — | — | 110 | B14 |
| PG[15] | PCR[111] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[111]<br>E1UC[1]<br>—<br>— | SIUL<br>eMIOS_1<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 111 | B13 |
| PH[0] | PCR[112] | AF0<br>AF1<br>AF2<br>AF3<br>— | GPIO[112]<br>E1UC[2]<br>—<br>—<br>SIN1 | SIUL<br>eMIOS_1<br>—<br>—<br>DSPI_1 | I/O<br>I/O<br>—<br>—<br>I | M | Tristate | — | — | — | 93 | F13 |
| PH[1] | PCR[113] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[113]<br>E1UC[3]<br>SOUT1<br>— | SIUL<br>eMIOS_1<br>DSPI_1<br>— | I/O<br>I/O<br>O<br>— | M | Tristate | — | — | — | 94 | F14 |
| PH[2] | PCR[114] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[114]<br>E1UC[4]<br>SCK_1<br>— | SIUL<br>eMIOS_1<br>DSPI_1<br>— | I/O<br>I/O<br>I/O<br>— | M | Tristate | — | — | — | 95 | F16 |
| PH[3] | PCR[115] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[115]<br>E1UC[5]<br>CS0_1<br>— | SIUL<br>eMIOS_1<br>DSPI_1<br>— | I/O<br>I/O<br>I/O<br>— | M | Tristate | — | — | — | 96 | F15 |



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**Table 5. Functional port pin descriptions (continued)**

| Port pin | PCR | Alternate function[1] | Function | Peripheral | I/O direction[2] | Pad type | RESET configuration | Pin number | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | MPC560xB 64 LQFP | MPC560xC 64 LQFP | 100 LQFP | 144 LQFP | 208 MAPBGA[3] |
| PH[4] | PCR[116] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[116]<br>E1UC[6]<br>—<br>— | SIUL<br>eMIOS_1<br>—<br>— | I/O<br>I/O<br>—<br>— | M | Tristate | — | — | — | 134 | A6 |
| PH[5] | PCR[117] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[117]<br>E1UC[7]<br>—<br>— | SIUL<br>eMIOS_1<br>—<br>— | I/O<br>I/O<br>—<br>— | S | Tristate | — | — | — | 135 | B6 |
| PH[6] | PCR[118] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[118]<br>E1UC[8]<br>—<br>MA[2] | SIUL<br>eMIOS_1<br>—<br>ADC | I/O<br>I/O<br>—<br>O | M | Tristate | — | — | — | 136 | D5 |
| PH[7] | PCR[119] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[119]<br>E1UC[9]<br>CS3_2<br>MA[1] | SIUL<br>eMIOS_1<br>DSPI_2<br>ADC | I/O<br>I/O<br>O<br>O | M | Tristate | — | — | — | 137 | C5 |
| PH[8] | PCR[120] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[120]<br>E1UC[10]<br>CS2_2<br>MA[0] | SIUL<br>eMIOS_1<br>DSPI_2<br>ADC | I/O<br>I/O<br>O<br>O | M | Tristate | — | — | — | 138 | A5 |
| PH[9][9] | PCR[121] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[121]<br>—<br>TCK<br>— | SIUL<br>—<br>JTAGC<br>— | I/O<br>—<br>I<br>— | S | Input, weak pull-up | 60 | 60 | 88 | 127 | B8 |
| PH[10][9] | PCR[122] | AF0<br>AF1<br>AF2<br>AF3 | GPIO[122]<br>—<br>TMS<br>— | SIUL<br>—<br>JTAGC<br>— | I/O<br>—<br>I<br>— | S | Input, weak pull-up | 53 | 53 | 81 | 120 | B9 |

1 Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2 Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

3 208 MAPBGA available only as development package for Nexus2+

4 All WKPU pins also support external interrupt capability. See wakeup unit chapter for further details.

5 NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

6 "Not applicable" because these functions are available only while the device is booting. Refer to BAM chapter of the reference manual for details.



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[7] Value of PCR.IBE bit must be 0

[8] Be aware that this pad is used on the MPC5607B 100-pin and 144-pin to provide VDD_HV_ADC and VSS_HV_ADC1. Therefore, you should be careful in ensuring compatibility between MPC5604B/C and MPC5607B.

[9] Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.
PC[0:1] are available as JTAG pins (TDI and TDO respectively).
PH[9:10] are available as JTAG pins (TCK and TMS respectively).
If the user configures these JTAG pins in GPIO mode the device is no longer compliant with IEEE 1149.1-2001.

[10] The TDO pad has been moved into the STANDBY domain in order to allow low-power debug handshaking in STANDBY mode. However, no pull-resistor is active on the TDO pad while in STANDBY mode. At this time the pad is configured as an input. When no debugger is connected the TDO pad is floating causing additional current consumption. To avoid the extra consumption TDO must be connected. An external pull-up resistor in the range of 47–100 kΩ should be added between the TDO pin and VDD_HV. Only in case the TDO pin is used as application pin and a pull-up cannot be used then a pull-down resistor with the same value should be used between TDO pin and GND instead.

[11] Available only on MPC560xC versions, MPC5603B 64 LQFP, MPC5604B 64 LQFP and MPC5604B 208 MAPBGA devices

[12] Not available on MPC5602B devices

[13] Not available in 100 LQFP package

[14] Available only on MPC5604B 208 MAPBGA devices

[15] Not available on MPC5603B 144-pin devices

## 2.7 Nexus 2+ pins

In the 208 MAPBGA package, eight additional debug pins are available (see Table 6).

**Table 6. Nexus 2+ pin descriptions**

| Debug pin | Function | I/O direction | Pad type | Function after reset | Pin number | | |
|---|---|---|---|---|---|---|---|
| | | | | | 100 LQFP | 144 LQFP | 208 MAP BGA[1] |
| MCKO | Message clock out | O | F | — | — | — | T4 |
| MDO0 | Message data out 0 | O | M | — | — | — | H15 |
| MDO1 | Message data out 1 | O | M | — | — | — | H16 |
| MDO2 | Message data out 2 | O | M | — | — | — | H14 |
| MDO3 | Message data out 3 | O | M | — | — | — | H13 |
| EVTI | Event in | I | M | Pull-up | — | — | K1 |
| EVTO | Event out | O | M | — | — | — | L4 |
| MSEO | Message start/end out | O | M | — | — | — | G16 |

[1] 208 MAPBGA available only as development package for Nexus2+.



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## 2.8 Electrical characteristics

## 2.9 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid applying any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level ($V_{DD}$ or $V_{SS}$). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

## 2.10 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in Table 7 are used and the parameters are tagged accordingly in the tables where appropriate.

**Table 7. Parameter classifications**

| Classification tag | Tag description |
|---|---|
| P | Those parameters are guaranteed during production testing on each individual device. |
| C | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations. |
| T | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D | Those parameters are derived mainly from simulations. |

**NOTE**

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

## 2.11 NVUSRO register

Bit values in the Non-Volatile User Options (NVUSRO) Register control portions of the device configuration, namely electrical parameters such as high voltage supply and oscillator margin, as well as digital functionality (watchdog enable/disable after reset).

For a detailed description of the NVUSRO register, please refer to the device reference manual.

### 2.11.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. Table 8 shows how NVUSRO[PAD3V5V] controls the device configuration.



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**Table 8. PAD3V5V field description**

| Value[1] | Description |
|---|---|
| 0 | High voltage supply is 5.0 V |
| 1 | High voltage supply is 3.3 V |

1 Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

## 2.11.2 NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. Table 9 shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

**Table 9. OSCILLATOR_MARGIN field description**

| Value[1] | Description |
|---|---|
| 0 | Low consumption configuration (4 MHz/8 MHz) |
| 1 | High margin configuration (4 MHz/16 MHz) |

1 Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.

## 2.11.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. Table 10 shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

**Table 10. WATCHDOG_EN field description**

| Value[1] | Description |
|---|---|
| 0 | Disable after reset |
| 1 | Enable after reset |

1 Default manufacturing value is ‘1’. Value can be programmed by customer in Shadow Flash.



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## 2.12 Absolute maximum ratings

**Table 11. Absolute maximum ratings**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{SS}$ | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| $V_{DD}$ | SR | Voltage on VDD_HV pins with respect to ground ($V_{SS}$) | — | –0.3 | 6.0 | V |
| $V_{SS_LV}$ | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground ($V_{SS}$) | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V |
| $V_{DD_BV}$ | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground ($V_{SS}$) | — | –0.3 | 6.0 | V |
| | | | Relative to $V_{DD}$ | –0.3 | $V_{DD}$+0.3 | |
| $V_{SS_ADC}$ | SR | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground ($V_{SS}$) | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V |
| $V_{DD_ADC}$ | SR | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground ($V_{SS}$) | — | –0.3 | 6.0 | V |
| | | | Relative to $V_{DD}$ | $V_{DD}$ –0.3 | $V_{DD}$+0.3 | |
| $V_{IN}$ | SR | Voltage on any GPIO pin with respect to ground ($V_{SS}$) | — | –0.3 | 6.0 | V |
| | | | Relative to $V_{DD}$ | — | $V_{DD}$+0.3 | |
| $I_{INJPAD}$ | SR | Injected input current on any pin during overload condition | — | –10 | 10 | mA |
| $I_{INJSUM}$ | SR | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | |
| $I_{AVGSEG}$ | SR | Sum of all the static I/O current within a supply segment | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | 70 | mA |
| | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | 64 | |
| $I_{CORELV}$ | SR | Low voltage static current sink through VDD_BV | — | — | 150 | mA |
| $T_{STORAGE}$ | SR | Storage temperature | — | –55 | 150 | °C |

### NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground ($V_{SS}$) must not exceed the recommended values.



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## 2.13 Recommended operating conditions

**Table 12. Recommended operating conditions (3.3 V)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{SS}$ | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| $V_{DD}$[1] | SR | Voltage on VDD_HV pins with respect to ground ($V_{SS}$) | — | 3.0 | 3.6 | V |
| $V_{SS_LV}$[2] | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground ($V_{SS}$) | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V |
| $V_{DD_BV}$[3] | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground ($V_{SS}$) | — | 3.0 | 3.6 | V |
| | | | Relative to $V_{DD}$ | $V_{DD}$–0.1 | $V_{DD}$+0.1 | |
| $V_{SS_ADC}$ | SR | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground ($V_{SS}$) | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V |
| $V_{DD_ADC}$[4] | SR | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground ($V_{SS}$) | — | 3.0[5] | 3.6 | V |
| | | | Relative to $V_{DD}$ | $V_{DD}$–0.1 | $V_{DD}$+0.1 | |
| $V_{IN}$ | SR | Voltage on any GPIO pin with respect to ground ($V_{SS}$) | — | $V_{SS}$–0.1 | — | V |
| | | | Relative to $V_{DD}$ | — | $V_{DD}$+0.1 | |
| $I_{INJPAD}$ | SR | Injected input current on any pin during overload condition | — | –5 | 5 | mA |
| $I_{INJSUM}$ | SR | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | |
| $TV_{DD}$ | SR | $V_{DD}$ slope to ensure correct power up[6] | — | — | 0.25 | V/µs |
| $T_{A}$ C-Grade Part | SR | Ambient temperature under bias | $f_{CPU} \leq 64$ MHz | –40 | 85 | °C |
| $T_{J}$ C-Grade Part | SR | Junction temperature under bias | | –40 | 110 | |
| $T_{A}$ V-Grade Part | SR | Ambient temperature under bias | | –40 | 105 | |
| $T_{J}$ V-Grade Part | SR | Junction temperature under bias | | –40 | 130 | |
| $T_{A}$ M-Grade Part | SR | Ambient temperature under bias | | –40 | 125 | |
| $T_{J}$ M-Grade Part | SR | Junction temperature under bias | | –40 | 150 | |

1 100 nF capacitance needs to be provided between each $V_{DD}/V_{SS}$ pair

2 330 nF capacitance needs to be provided between each $V_{DD_LV}/V_{SS_LV}$ supply pair.

3 400 nF capacitance needs to be provided between $V_{DD_BV}$ and the nearest $V_{SS_LV}$ (higher value may be needed depending on external regulator characteristics).

4 100 nF capacitance needs to be provided between $V_{DD_ADC}/V_{SS_ADC}$ pair.

5 Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below $V_{LVDHVL}$, device is reset.

6 Guaranteed by device validation.



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**Table 13. Recommended operating conditions (5.0 V)**

| Symbol | | Parameter | Conditions | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{SS}$ | SR | Digital ground on VSS_HV pins | — | 0 | 0 | V |
| $V_{DD}$[1] | SR | Voltage on VDD_HV pins with respect to ground ($V_{SS}$) | — | 4.5 | 5.5 | V |
| | | | Voltage drop[2] | 3.0 | 5.5 | |
| $V_{SS_LV}$[3] | SR | Voltage on VSS_LV (low voltage digital supply) pins with respect to ground ($V_{SS}$) | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V |
| $V_{DD_BV}$[4] | SR | Voltage on VDD_BV pin (regulator supply) with respect to ground ($V_{SS}$) | — | 4.5 | 5.5 | V |
| | | | Voltage drop[2] | 3.0 | 5.5 | |
| | | | Relative to $V_{DD}$ | $V_{DD}$–0.1 | $V_{DD}$+0.1 | |
| $V_{SS_ADC}$ | SR | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground ($V_{SS}$ | — | $V_{SS}$–0.1 | $V_{SS}$+0.1 | V |
| $V_{DD_ADC}$[5] | SR | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground ($V_{SS}$) | — | 4.5 | 5.5 | V |
| | | | Voltage drop[2] | 3.0 | 5.5 | |
| | | | Relative to $V_{DD}$ | $V_{DD}$–0.1 | $V_{DD}$+0.1 | |
| $V_{IN}$ | SR | Voltage on any GPIO pin with respect to ground ($V_{SS}$) | — | $V_{SS}$–0.1 | — | V |
| | | | Relative to $V_{DD}$ | — | $V_{DD}$+0.1 | |
| $I_{INJPAD}$ | SR | Injected input current on any pin during overload condition | — | –5 | 5 | mA |
| $I_{INJSUM}$ | SR | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | |
| $TV_{DD}$ | SR | $V_{DD}$ slope to ensure correct power up[6] | — | — | 0.25 | V/µs |
| $T_{A}$ C-Grade Part | SR | Ambient temperature under bias | $f_{CPU} \leq 64$ MHz | –40 | 85 | °C |
| $T_{J}$ C-Grade Part | SR | Junction temperature under bias | | –40 | 110 | |
| $T_{A}$ V-Grade Part | SR | Ambient temperature under bias | | –40 | 105 | |
| $T_{J}$ V-Grade Part | SR | Junction temperature under bias | | –40 | 130 | |
| $T_{A}$ M-Grade Part | SR | Ambient temperature under bias | | –40 | 125 | |
| $T_{J}$ M-Grade Part | SR | Junction temperature under bias | | –40 | 150 | |

1 100 nF capacitance needs to be provided between each $V_{DD}/V_{SS}$ pair.

2 Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

3 330 nF capacitance needs to be provided between each $V_{DD_LV}/V_{SS_LV}$ supply pair.

4 100 nF capacitance needs to be provided between $V_{DD_BV}$ and the nearest $V_{SS_LV}$ (higher value may be needed depending on external regulator characteristics).

5 1 µF (electrolithic/tantalum) + 47 nF (ceramic) capacitance needs to be provided between $V_{DD_ADC}/V_{SS_ADC}$ pair. Another ceramic cap of 10 nF with low inductance package can be added.

6 Guaranteed by device validation.

## NOTE

RAM data retention is guaranteed with $V_{DD_LV}$ not below 1.08 V.



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## 2.14 Thermal characteristics

### 2.14.1 Package thermal characteristics

**Table 14. LQFP thermal characteristics[1]**

| Symbol | | C | Parameter | Conditions[2] | Pin count | Value | Unit |
|---|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | CC | D | Thermal resistance, junction-to-ambient natural convection[3] | Single-layer board - 1s | 64 | 60 | °C/W |
| | | | | | 100 | 64 | |
| | | | | | 144 | 64 | |
| | | | | Four-layer board - 2s2p | 64 | 42 | |
| | | | | | 100 | 51 | |
| | | | | | 144 | 49 | |
| $R_{\theta JB}$ | CC | D | Thermal resistance, junction-to-board[4] | Single-layer board - 1s | 64 | 24 | °C/W |
| | | | | | 100 | 36 | |
| | | | | | 144 | 37 | |
| | | | | Four-layer board - 2s2p | 64 | 24 | |
| | | | | | 100 | 34 | |
| | | | | | 144 | 35 | |
| $R_{\theta JC}$ | CC | D | Thermal resistance, junction-to-case[5] | Single-layer board - 1s | 64 | 11 | °C/W |
| | | | | | 100 | 22 | |
| | | | | | 144 | 22 | |
| | | | | Four-layer board - 2s2p | 64 | 11 | |
| | | | | | 100 | 22 | |
| | | | | | 144 | 22 | |
| $\Psi_{JB}$ | CC | D | Junction-to-board thermal characterization parameter, natural convection | Single-layer board - 1s | 64 | TBD | °C/W |
| | | | | | 100 | 33 | |
| | | | | | 144 | 34 | |
| | | | | Four-layer board - 2s2p | 64 | TBD | |
| | | | | | 100 | 34 | |
| | | | | | 144 | 35 | |
| $\Psi_{JC}$ | CC | D | Junction-to-case thermal characterization parameter, natural convection | Single-layer board - 1s | 64 | TBD | °C/W |
| | | | | | 100 | 9 | |
| | | | | | 144 | 10 | |
| | | | | Four-layer board - 2s2p | 64 | TBD | |
| | | | | | 100 | 9 | |
| | | | | | 144 | 10 | |

1 Thermal characteristics are based on simulation.



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2 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C

3 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

4 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

5 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

### 2.14.2 Power considerations

The average chip-junction temperature, $T_J$, in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \textit{Eqn. 1}$$

Where:

$T_A$ is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

$P_D$ is the sum of $P_{INT}$ and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

$P_{INT}$ is the product of $I_{DD}$ and $V_{DD}$, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2 \quad \textit{Eqn. 3}$$

Where:

K is a constant for the particular part, which may be determined from Equation 3 by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ may be obtained by solving equations 1 and 2 iteratively for any value of $T_A$.

## 2.15 I/O pad electrical characteristics

### 2.15.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. There are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and the external 32 kHz crystal oscillator (SXOSC) providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.



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## 2.15.2 I/O input DC characteristics

Table 15 provides input DC electrical characteristics as described in Figure 7.

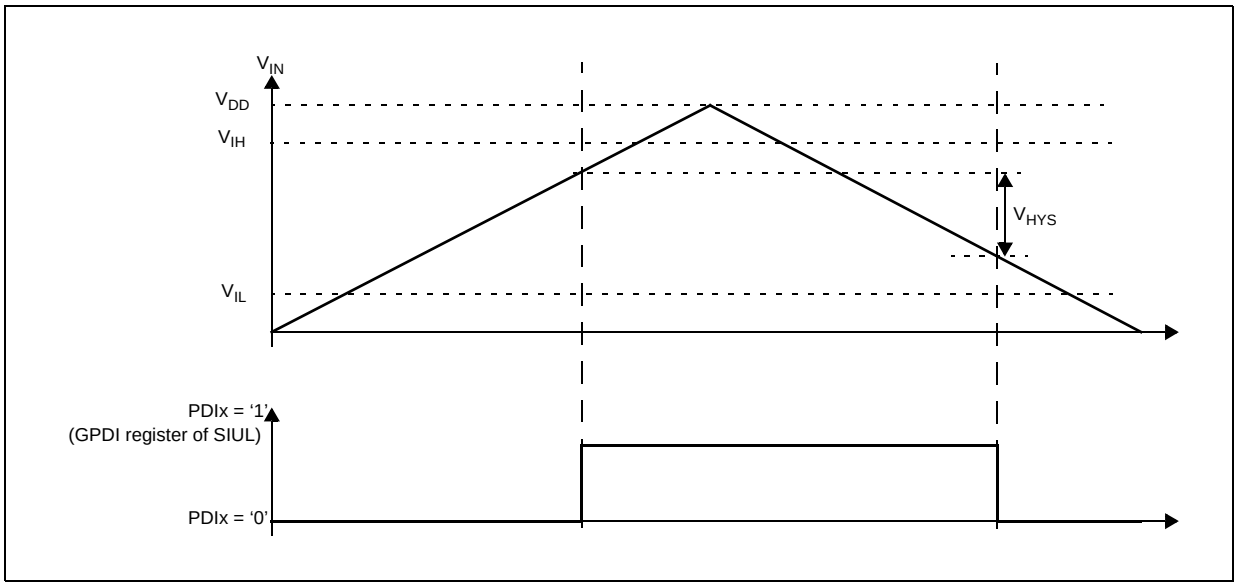


**Figure 7. I/O input DC electrical characteristics definition**

**Table 15. I/O input DC electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{IH}$ | SR | P | Input high level CMOS (Schmitt Trigger) | — | | $0.65V_{DD}$ | — | $V_{DD}+0.4$ | V |
| $V_{IL}$ | SR | P | Input low level CMOS (Schmitt Trigger) | — | | –0.4 | — | $0.35V_{DD}$ | |
| $V_{HYS}$ | CC | C | Input hysteresis CMOS (Schmitt Trigger) | — | | $0.1V_{DD}$ | — | — | |
| $I_{LKG}$ | CC | D | Digital input leakage | No injection on adjacent pin | $T_A$ = –40 °C | — | 2 | 200 | nA |
| | | D | | | $T_A$ = 25 °C | — | 2 | 200 | |
| | | D | | | $T_A$ = 85 °C | — | 5 | 300 | |
| | | D | | | $T_A$ = 105 °C | — | 12 | 500 | |
| | | P | | | $T_A$ = 125 °C | — | 70 | 1000 | |
| $W_{FI}$[2] | SR | P | Wakeup input filtered pulse | — | | — | — | 40 | ns |
| $W_{NFI}$[2] | SR | P | Wakeup input not filtered pulse | — | | 1000 | — | — | ns |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.



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## 2.15.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 16 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 17 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 18 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 19 provides output driver characteristics for I/O pads when in FAST configuration.

**Table 16. I/O pull-up/pull-down DC electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $\|I_{WPU}\|$ | CC | P | Weak pull-up current absolute value | $V_{IN} = V_{IL}$, $V_{DD}$ = 5.0 V ± 10% | PAD3V5V = 0 | 10 | — | 150 | µA |
| | | C | | | PAD3V5V = 1[2] | 10 | — | 250 | |
| | | P | | $V_{IN} = V_{IL}$, $V_{DD}$ = 3.3 V ± 10% | PAD3V5V = 1 | 10 | — | 150 | |
| $\|I_{WPD}\|$ | CC | P | Weak pull-down current absolute value | $V_{IN} = V_{IH}$, $V_{DD}$ = 5.0 V ± 10% | PAD3V5V = 0 | 10 | — | 150 | µA |
| | | C | | | PAD3V5V = 1 | 10 | — | 250 | |
| | | P | | $V_{IN} = V_{IH}$, $V_{DD}$ = 3.3 V ± 10% | PAD3V5V = 1 | 10 | — | 150 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.

2 The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

**Table 17. SLOW configuration output buffer electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{OH}$ | CC | P | Output high level SLOW configuration | Push Pull | $I_{OH}$ = –2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | 0.8$V_{DD}$ | — | — | V |
| | | C | | | $I_{OH}$ = –2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | 0.8$V_{DD}$ | — | — | |
| | | C | | | $I_{OH}$ = –1 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | $V_{DD}$–0.8 | — | — | |
| $V_{OL}$ | CC | P | Output low level SLOW configuration | Push Pull | $I_{OL}$ = 2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | 0.1$V_{DD}$ | V |
| | | C | | | $I_{OL}$ = 2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | — | — | 0.1$V_{DD}$ | |
| | | C | | | $I_{OL}$ = 1 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.



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**Table 18. MEDIUM configuration output buffer electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{OH}$ | CC | C | Output high level MEDIUM configuration | Push Pull | $I_{OH}$ = –3.8 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | $0.8V_{DD}$ | — | — | V |
| | | P | | | $I_{OH}$ = –2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | $0.8V_{DD}$ | — | — | |
| | | C | | | $I_{OH}$ = –1 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | $0.8V_{DD}$ | — | — | |
| | | C | | | $I_{OH}$ = –1 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | $V_{DD}$–0.8 | — | — | |
| | | C | | | $I_{OH}$ = –100 µA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | $0.8V_{DD}$ | — | — | |
| $V_{OL}$ | CC | C | Output low level MEDIUM configuration | Push Pull | $I_{OL}$ = 3.8 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | $0.2V_{DD}$ | V |
| | | P | | | $I_{OL}$ = 2 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | $0.1V_{DD}$ | |
| | | C | | | $I_{OL}$ = 1 mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | — | — | $0.1V_{DD}$ | |
| | | C | | | $I_{OL}$ = 1 mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |
| | | C | | | $I_{OL}$ = 100 µA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | $0.1V_{DD}$ | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

**Table 19. FAST configuration output buffer electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{OH}$ | CC | P | Output high level FAST configuration | Push Pull | $I_{OH}$ = –14mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | $0.8V_{DD}$ | — | — | V |
| | | C | | | $I_{OH}$ = –7mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | $0.8V_{DD}$ | — | — | |
| | | C | | | $I_{OH}$ = –11mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | $V_{DD}$–0.8 | — | — | |



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**Table 19. FAST configuration output buffer electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $V_{OL}$ | CC | P | Output low level FAST configuration | Push Pull | $I_{OL}$ = 14mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | $0.1V_{DD}$ | V |
| | | C | | | $I_{OL}$ = 7mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | — | — | $0.1V_{DD}$ | |
| | | C | | | $I_{OL}$ = 11mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when $V_{DD}$ = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

## 2.15.4 Output pin transition times

**Table 20. Output pin transition times**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $t_{tr}$ | CC | D | Output transition time output pin[2] SLOW configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 50 | ns |
| | | T | | $C_L$ = 50 pF | | — | — | 100 | |
| | | D | | $C_L$ = 100 pF | | — | — | 125 | |
| | | D | | $C_L$ = 25 pF | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 50 | |
| | | T | | $C_L$ = 50 pF | | — | — | 100 | |
| | | D | | $C_L$ = 100 pF | | — | — | 125 | |
| $t_{tr}$ | CC | D | Output transition time output pin[2] MEDIUM configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1 | — | — | 10 | ns |
| | | T | | $C_L$ = 50 pF | | — | — | 20 | |
| | | D | | $C_L$ = 100 pF | | — | — | 40 | |
| | | D | | $C_L$ = 25 pF | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1 | — | — | 12 | |
| | | T | | $C_L$ = 50 pF | | — | — | 25 | |
| | | D | | $C_L$ = 100 pF | | — | — | 40 | |
| $t_{tr}$ | CC | D | Output transition time output pin[2] FAST configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 4 | ns |
| | | | | $C_L$ = 50 pF | | — | — | 6 | |
| | | | | $C_L$ = 100 pF | | — | — | 12 | |
| | | | | $C_L$ = 25 pF | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 4 | |
| | | | | $C_L$ = 50 pF | | — | — | 7 | |
| | | | | $C_L$ = 100 pF | | — | — | 12 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified



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[2] $C_L$ includes device and package capacitances ($C_{PKG}$ < 5 pF).

## 2.15.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a $V_{DD}/V_{SS}$ supply pair as described in Table 21.

**Table 21. I/O supply segment**

| Package | Supply segment | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| 208 MAPBGA[1] | Equivalent to 144 LQFP segment pad distribution | | | | MCKO | MDOn/MSEO |
| 144 LQFP | pin20–pin49 | pin51–pin99 | pin100–pin122 | pin 123–pin19 | — | — |
| 100 LQFP | pin16–pin35 | pin37–pin69 | pin70–pin83 | pin 84–pin15 | — | — |
| 64 LQFP | pin8–pin26 | pin28–pin55 | pin56–pin7 | — | — | — |

[1] 208 MAPBGA available only as development package for Nexus2+

Table 22 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the $I_{AVGSEG}$ maximum value.

**Table 22. I/O consumption**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{SWTSLW}$[2] | CC | D | Dynamic I/O current for SLOW configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 20 | mA |
| | | | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 16 | |
| $I_{SWTMED}$[2] | CC | D | Dynamic I/O current for MEDIUM configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 29 | mA |
| | | | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 17 | |
| $I_{SWTFST}$[2] | CC | D | Dynamic I/O current for FAST configuration | $C_L$ = 25 pF | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 110 | mA |
| | | | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 50 | |
| $I_{RMSSLW}$ | CC | D | Root mean square I/O current for SLOW configuration | $C_L$ = 25 pF, 2 MHz | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 2.3 | mA |
| | | | | $C_L$ = 25 pF, 4 MHz | | — | — | 3.2 | |
| | | | | $C_L$ = 100 pF, 2 MHz | | — | — | 6.6 | |
| | | | | $C_L$ = 25 pF, 2 MHz | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 1.6 | |
| | | | | $C_L$ = 25 pF, 4 MHz | | — | — | 2.3 | |
| | | | | $C_L$ = 100 pF, 2 MHz | | — | — | 4.7 | |



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**Table 22. I/O consumption (continued)**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{RMSMED}$ | CC | D | Root mean square I/O current for MEDIUM configuration | $C_L$ = 25 pF, 13 MHz | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 6.6 | mA |
| | | | | $C_L$ = 25 pF, 40 MHz | | — | — | 13.4 | |
| | | | | $C_L$ = 100 pF, 13 MHz | | — | — | 18.3 | |
| | | | | $C_L$ = 25 pF, 13 MHz | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 5 | |
| | | | | $C_L$ = 25 pF, 40 MHz | | — | — | 8.5 | |
| | | | | $C_L$ = 100 pF, 13 MHz | | — | — | 11 | |
| $I_{RMSFST}$ | CC | D | Root mean square I/O current for FAST configuration | $C_L$ = 25 pF, 40 MHz | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 22 | mA |
| | | | | $C_L$ = 25 pF, 64 MHz | | — | — | 33 | |
| | | | | $C_L$ = 100 pF, 40 MHz | | — | — | 56 | |
| | | | | $C_L$ = 25 pF, 40 MHz | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 14 | |
| | | | | $C_L$ = 25 pF, 64 MHz | | — | — | 20 | |
| | | | | $C_L$ = 100 pF, 40 MHz | | — | — | 35 | |
| $I_{AVGSEG}$ | SR | D | Sum of all the static I/O current within a supply segment | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | | — | — | 70 | mA |
| | | | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | | — | — | 65 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to125 °C, unless otherwise specified

2 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 23 provides the weight of concurrent switching I/Os.

Due to the dynamic current limitations, the sum of the weight of concurrent switching I/Os on a single segment must not exceed 100% to ensure device functionality.

**Table 23. I/O weight[1]**

| Supply segment | | | Pad | 144/100 LQFP | | | | 64 LQFP | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | |
| 144 LQFP | 100 LQFP | 64 LQFP[2] | | SRC[3] = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| 4 | 4 | 3 | PB[3] | 10% | — | 12% | — | 10% | — | 12% | — |
| | | | PC[9] | 10% | — | 12% | — | 10% | — | 12% | — |
| | | — | PC[14] | 9% | — | 11% | — | — | — | — | — |
| | | — | PC[15] | 9% | 13% | 11% | 12% | — | — | — | — |
| | — | — | PG[5] | 9% | — | 11% | — | — | — | — | — |
| | — | — | PG[4] | 9% | 12% | 10% | 11% | — | — | — | — |
| | — | — | PG[3] | 9% | — | 10% | — | — | — | — | — |



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**Table 23. I/O weight[1] (continued)**

| Supply segment | | | Pad | 144/100 LQFP | | | | 64 LQFP | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | |
| 144 LQFP | 100 LQFP | 64 LQFP[2] | | SRC[3] = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| 4 | — | — | PG[2] | 8% | 12% | 10% | 10% | — | — | — | — |
| | 4 | 3 | PA[2] | 8% | — | 9% | — | 8% | — | 9% | — |
| | | — | PE[0] | 8% | — | 9% | — | — | — | — | — |
| | | 3 | PA[1] | 7% | — | 9% | — | 7% | — | 9% | — |
| | | — | PE[1] | 7% | 10% | 8% | 9% | — | — | — | — |
| | | — | PE[8] | 7% | 9% | 8% | 8% | — | — | — | — |
| | | — | PE[9] | 6% | — | 7% | — | — | — | — | — |
| | | — | PE[10] | 6% | — | 7% | — | — | — | — | — |
| | | 3 | PA[0] | 5% | 8% | 6% | 7% | 5% | 8% | 6% | 7% |
| | | — | PE[11] | 5% | — | 6% | — | — | — | — | — |
| 1 | — | — | PG[9] | 9% | — | 10% | — | — | — | — | — |
| | — | — | PG[8] | 9% | — | 11% | — | — | — | — | — |
| | 1 | — | PC[11] | 9% | — | 11% | — | — | — | — | — |
| | | 1 | PC[10] | 9% | 13% | 11% | 12% | 9% | 13% | 11% | 12% |
| | — | — | PG[7] | 10% | 14% | 11% | 12% | — | — | — | — |
| | — | — | PG[6] | 10% | 14% | 12% | 12% | — | — | — | — |
| | 1 | 1 | PB[0] | 10% | 14% | 12% | 12% | 10% | 14% | 12% | 12% |
| | | | PB[1] | 10% | — | 12% | — | 10% | — | 12% | — |
| | — | — | PF[9] | 10% | — | 12% | — | — | — | — | — |
| | — | — | PF[8] | 10% | 15% | 12% | 13% | — | — | — | — |
| | — | — | PF[12] | 10% | 15% | 12% | 13% | — | — | — | — |
| | 1 | 1 | PC[6] | 10% | — | 12% | — | 10% | — | 12% | — |
| | | | PC[7] | 10% | — | 12% | — | 10% | — | 12% | — |
| | — | — | PF[10] | 10% | 14% | 12% | 12% | — | — | — | — |
| | — | — | PF[11] | 10% | — | 11% | — | — | — | — | — |
| | 1 | 1 | PA[15] | 9% | 12% | 10% | 11% | 9% | 12% | 10% | 11% |
| | — | — | PF[13] | 8% | — | 10% | — | — | — | — | — |
| | 1 | 1 | PA[14] | 8% | 11% | 9% | 10% | 8% | 11% | 9% | 10% |
| | | | PA[4] | 8% | — | 9% | — | 8% | — | 9% | — |
| | | | PA[13] | 7% | 10% | 9% | 9% | 7% | 10% | 9% | 9% |
| | | | PA[12] | 7% | — | 8% | — | 7% | — | 8% | — |



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**Table 23. I/O weight[1] (continued)**

| Supply segment | | | Pad | 144/100 LQFP | | | | 64 LQFP | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | |
| 144 LQFP | 100 LQFP | 64 LQFP[2] | | SRC[3] = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| 2 | 2 | 2 | PB[9] | 1% | — | 1% | — | 1% | — | 1% | — |
| | | | PB[8] | 1% | — | 1% | — | 1% | — | 1% | — |
| | | | PB[10] | 6% | — | 7% | — | 6% | — | 7% | — |
| | — | — | PF[0] | 6% | — | 7% | — | — | — | — | — |
| | — | — | PF[1] | 7% | — | 8% | — | — | — | — | — |
| | — | — | PF[2] | 7% | — | 8% | — | — | — | — | — |
| | — | — | PF[3] | 7% | — | 9% | — | — | — | — | — |
| | — | — | PF[4] | 8% | — | 9% | — | — | — | — | — |
| | — | — | PF[5] | 8% | — | 10% | — | — | — | — | — |
| | — | — | PF[6] | 8% | — | 10% | — | — | — | — | — |
| | — | — | PF[7] | 9% | — | 10% | — | — | — | — | — |
| | 2 | — | PD[0] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[1] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[2] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[3] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[4] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[5] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[6] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[7] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[8] | 1% | — | 1% | — | — | — | — | — |
| | | 2 | PB[4] | 1% | — | 1% | — | 1% | — | 1% | — |
| | | | PB[5] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | | PB[6] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | | PB[7] | 1% | — | 1% | — | 1% | — | 2% | — |
| | | — | PD[9] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[10] | 1% | — | 1% | — | — | — | — | — |
| | | — | PD[11] | 1% | — | 1% | — | — | — | — | — |
| | | 2 | PB[11] | 11% | — | 13% | — | 17% | — | 21% | — |
| | | — | PD[12] | 11% | — | 13% | — | — | — | — | — |
| | | 2 | PB[12] | 11% | — | 13% | — | 18% | — | 21% | — |
| | | — | PD[13] | 10% | — | 12% | — | — | — | — | — |



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**Table 23. I/O weight[1] (continued)**

| Supply segment | | | Pad | 144/100 LQFP | | | | 64 LQFP | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | |
| 144 LQFP | 100 LQFP | 64 LQFP[2] | | SRC[3] = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| 2 | 2 | 2 | PB[13] | 10% | — | 12% | — | 18% | — | 21% | — |
| | | — | PD[14] | 10% | — | 12% | — | — | — | — | — |
| | | 2 | PB[14] | 10% | — | 12% | — | 18% | — | 21% | — |
| | | — | PD[15] | 10% | — | 11% | — | — | — | — | — |
| | | 2 | PB[15] | 9% | — | 11% | — | 18% | — | 21% | — |
| | | | PA[3] | 9% | — | 11% | — | 18% | — | 21% | — |
| | — | — | PG[13] | 9% | 13% | 10% | 11% | — | — | — | — |
| | — | — | PG[12] | 9% | 12% | 10% | 11% | — | — | — | — |
| | — | — | PH[0] | 5% | 8% | 6% | 7% | — | — | — | — |
| | — | — | PH[1] | 5% | 7% | 6% | 6% | — | — | — | — |
| | — | — | PH[2] | 5% | 6% | 5% | 6% | — | — | — | — |
| | — | — | PH[3] | 4% | 6% | 5% | 5% | — | — | — | — |
| | — | — | PG[1] | 4% | — | 4% | — | — | — | — | — |
| | — | — | PG[0] | 3% | 4% | 4% | 4% | — | — | — | — |
| 3 | — | — | PF[15] | 3% | — | 4% | — | — | — | — | — |
| | — | — | PF[14] | 4% | 5% | 5% | 5% | — | — | — | — |
| | — | — | PE[13] | 4% | — | 5% | — | — | — | — | — |
| | 3 | 2 | PA[7] | 5% | — | 6% | — | 16% | — | 19% | — |
| | | | PA[8] | 5% | — | 6% | — | 16% | — | 19% | — |
| | | | PA[9] | 5% | — | 6% | — | 15% | — | 18% | — |
| | | | PA[10] | 6% | — | 7% | — | 15% | — | 18% | — |
| | | | PA[11] | 6% | — | 8% | — | 14% | — | 17% | — |
| | | — | PE[12] | 7% | — | 8% | — | — | — | — | — |
| | — | — | PG[14] | 7% | — | 8% | — | — | — | — | — |
| | — | — | PG[15] | 7% | 10% | 8% | 9% | — | — | — | — |
| | — | — | PE[14] | 7% | — | 8% | — | — | — | — | — |
| | — | — | PE[15] | 7% | 9% | 8% | 8% | — | — | — | — |
| | — | — | PG[10] | 6% | — | 8% | — | — | — | — | — |
| | — | — | PG[11] | 6% | 9% | 7% | 8% | — | — | — | — |
| | 3 | 2 | PC[3] | 6% | — | 7% | — | 7% | — | 9% | — |
| | | | PC[2] | 6% | 8% | 7% | 7% | 6% | 9% | 8% | 8% |



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**Table 23. I/O weight[1] (continued)**

| Supply segment | | | Pad | 144/100 LQFP | | | | 64 LQFP | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Weight 5 V | | Weight 3.3 V | | Weight 5 V | | Weight 3.3 V | |
| 144 LQFP | 100 LQFP | 64 LQFP[2] | | SRC[3] = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 | SRC = 0 | SRC = 1 |
| 3 | 3 | 2 | PA[5] | 5% | 7% | 6% | 6% | 6% | 8% | 7% | 7% |
| | | | PA[6] | 5% | — | 6% | — | 5% | — | 6% | — |
| | | | PH[10] | 4% | 6% | 5% | 5% | 5% | 7% | 6% | 6% |
| | | | PC[1] | 5% | — | 5% | — | 5% | — | 5% | — |
| 4 | 4 | 3 | PC[0] | 6% | 9% | 7% | 8% | 6% | 9% | 7% | 8% |
| | | | PH[9] | 7 | 7 | 8 | 8 | 7 | 7 | 8 | 8 |
| | | — | PE[2] | 7% | 10% | 9% | 9% | — | — | — | — |
| | | — | PE[3] | 8% | 11% | 9% | 9% | — | — | — | — |
| | | 3 | PC[5] | 8% | 11% | 9% | 10% | 8% | 11% | 9% | 10% |
| | | | PC[4] | 8% | 12% | 10% | 10% | 8% | 12% | 10% | 10% |
| | | — | PE[4] | 8% | 12% | 10% | 11% | — | — | — | — |
| | | — | PE[5] | 9% | 12% | 10% | 11% | — | — | — | — |
| | — | — | PH[4] | 9% | 13% | 11% | 11% | — | — | — | — |
| | — | — | PH[5] | 9% | — | 11% | — | — | — | — | — |
| | — | — | PH[6] | 9% | 13% | 11% | 12% | — | — | — | — |
| | — | — | PH[7] | 9% | 13% | 11% | 12% | — | — | — | — |
| | — | — | PH[8] | 10% | 14% | 11% | 12% | — | — | — | — |
| | 4 | — | PE[6] | 10% | 14% | 12% | 12% | — | — | — | — |
| | | — | PE[7] | 10% | 14% | 12% | 12% | — | — | — | — |
| | | — | PC[12] | 10% | 14% | 12% | 13% | — | — | — | — |
| | | — | PC[13] | 10% | — | 12% | — | — | — | — | — |
| | | 3 | PC[8] | 10% | — | 12% | — | 10% | — | 12% | — |
| | | | PB[2] | 10% | 15% | 12% | 13% | 10% | 15% | 12% | 13% |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to125 °C, unless otherwise specified

2 Segments shown apply to MPC560xB devices only

3 SRC: “Slew Rate Control” bit in SIU_PCR

## 2.16 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.



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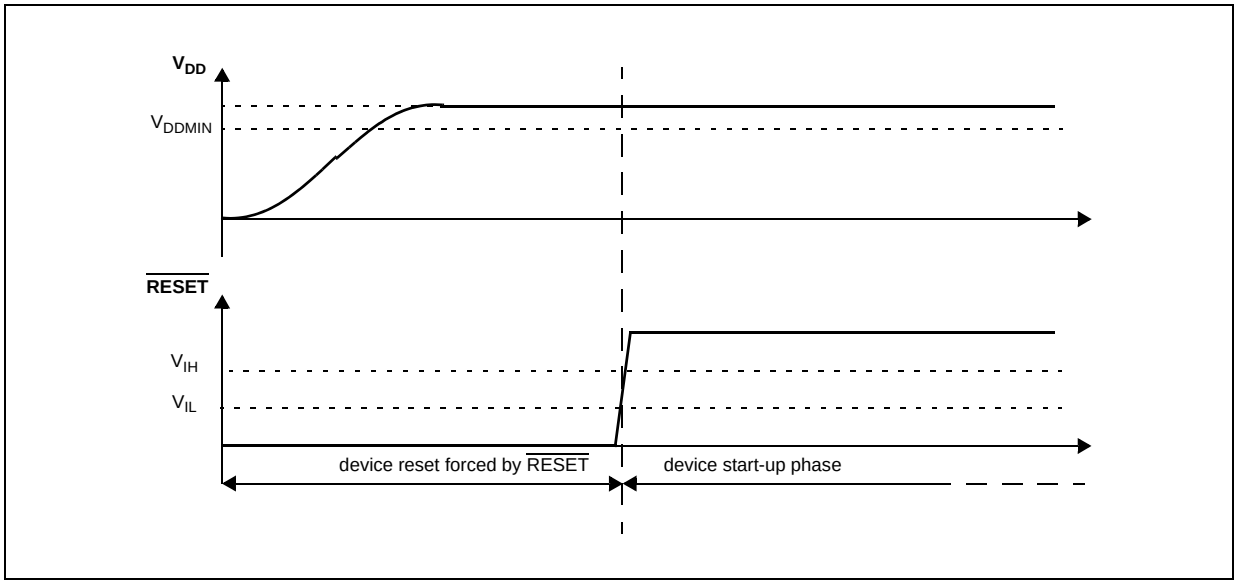


**Figure 8. Start-up reset requirements**

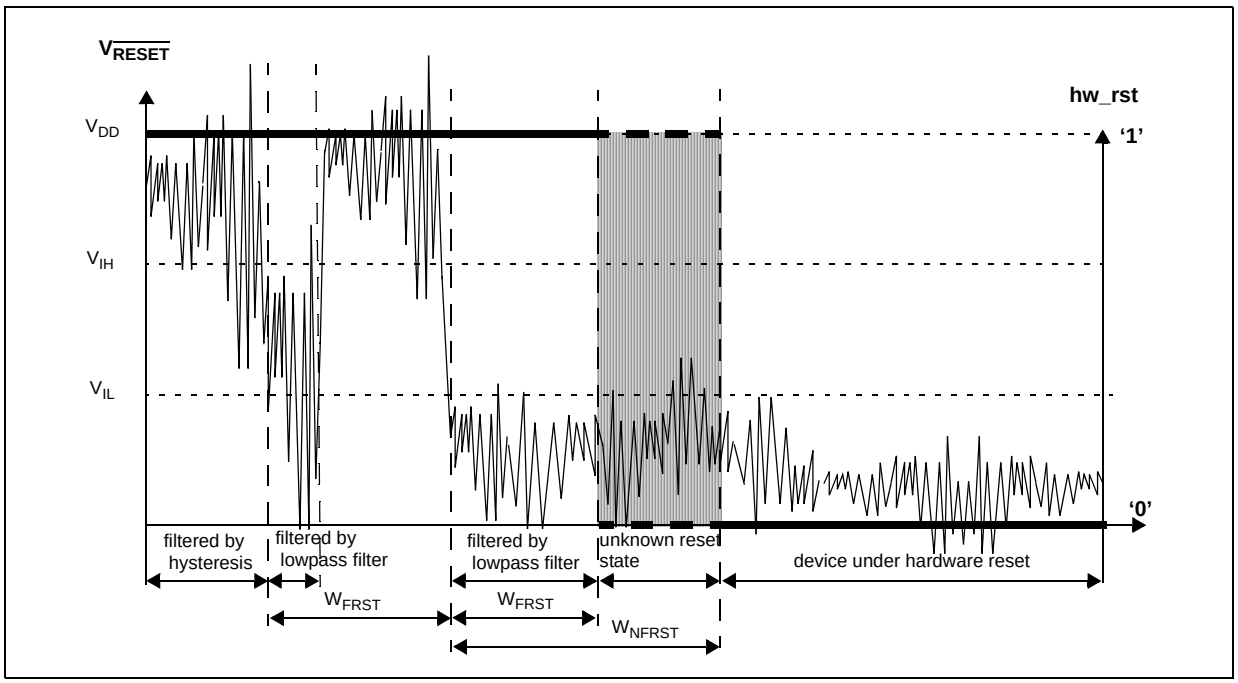


**Figure 9. Noise filtering on reset signal**

**Table 24. Reset electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{IH}$ | SR | P | Input High Level CMOS (Schmitt Trigger) | — | $0.65V_{DD}$ | — | $V_{DD}+0.4$ | V |



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**Table 24. Reset electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{IL}$ | SR | P | Input low Level CMOS (Schmitt Trigger) | — | –0.4 | — | $0.35V_{DD}$ | V |
| $V_{HYS}$ | CC | C | Input hysteresis CMOS (Schmitt Trigger) | — | $0.1V_{DD}$ | — | — | V |
| $V_{OL}$ | CC | P | Output low level | Push Pull, $I_{OL}$ = 2mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 (recommended) | — | — | $0.1V_{DD}$ | V |
| | | C | | Push Pull, $I_{OL}$ = 1mA, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | — | — | $0.1V_{DD}$ | |
| | | C | | Push Pull, $I_{OL}$ = 1mA, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 (recommended) | — | — | 0.5 | |
| $t_{tr}$ | CC | D | Output transition time output pin[3] | $C_L$ = 25pF, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 10 | ns |
| | | | | $C_L$ = 50pF, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 20 | |
| | | | | $C_L$ = 100pF, $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | — | — | 40 | |
| | | | | $C_L$ = 25pF, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 12 | |
| | | | | $C_L$ = 50pF, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 25 | |
| | | | | $C_L$ = 100pF, $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | — | — | 40 | |
| $W_{FRST}$ | SR | P | $\overline{\text{RESET}}$ input filtered pulse | — | — | — | 40 | ns |
| $W_{NFRST}$ | SR | P | $\overline{\text{RESET}}$ input not filtered pulse | — | 1000 | — | — | ns |
| $\lvert I_{WPU} \rvert$ | CC | P | Weak pull-up current absolute value | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 | 10 | — | 150 | µA |
| | | D | | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 | 10 | — | 150 | |
| | | P | | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 1[2] | 10 | — | 250 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 This transient configuration does not occurs when device is used in the $V_{DD}$ = 3.3 V ± 10% range.

3 $C_L$ includes device and package capacitance ($C_{PKG}$ < 5 pF).

## 2.17 Power management electrical characteristics

### 2.17.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply $V_{DD_LV}$ from the high voltage ballast supply $V_{DD_BV}$. The regulator itself is supplied by the common I/O supply $V_{DD}$. The following supplies are involved:



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- HV—High voltage external power supply for voltage regulator module. This must be provided externally through VDD_HV power pin.
- BV—High voltage external power supply for internal ballast module. This must be provided externally through VDD_BV power pin. Voltage values should be aligned with $V_{DD}$.
- LV—Low voltage internal power supply for core, FMPLL and flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV_COR—Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV_CFLA—Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_DFLA—Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
  - LV_PLL—Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

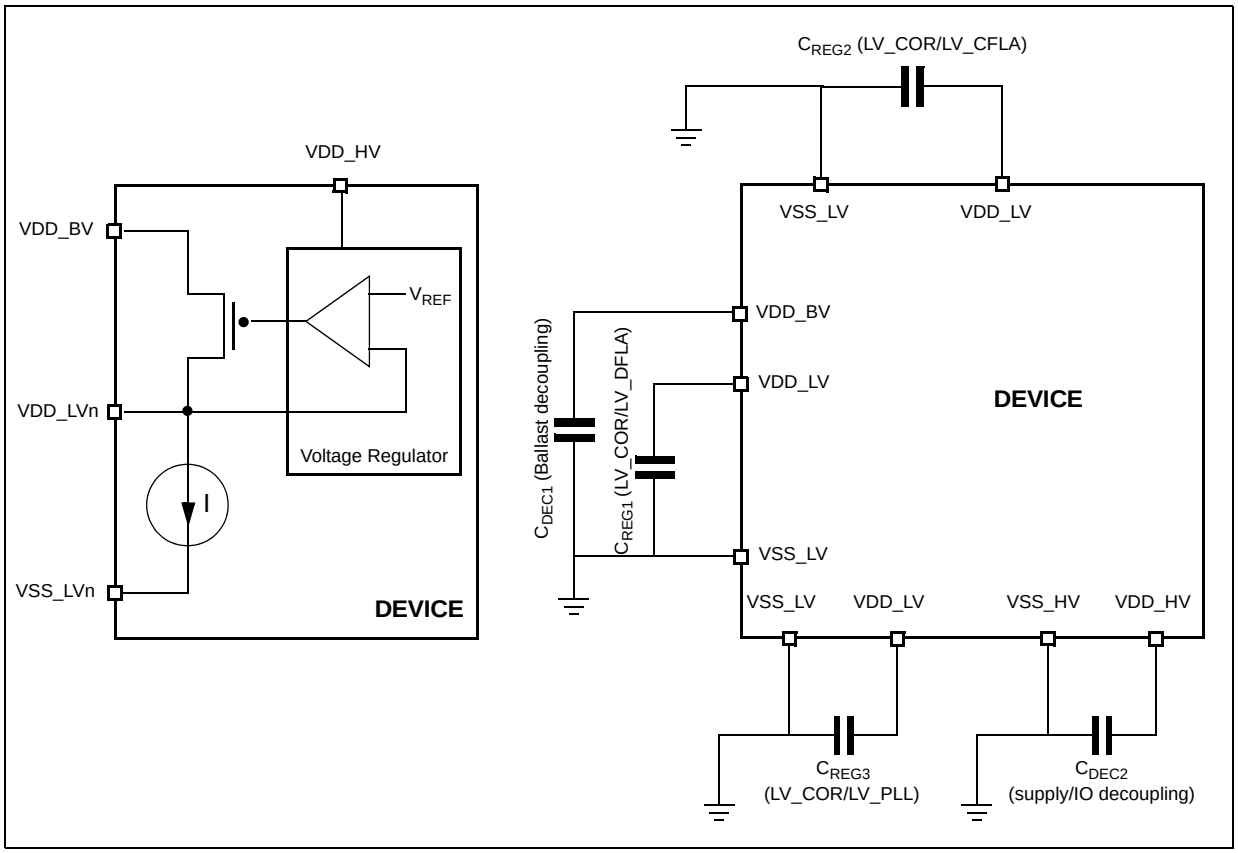


**Figure 10. Voltage regulator capacitance connection**

The internal voltage regulator requires external capacitance ($C_{REGn}$) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three $V_{DD_LV}/V_{SS_LV}$ supply pairs to ensure stable voltage (see Section 2.13, Recommended operating conditions).

The internal voltage regulator requires a controlled slew rate of both $V_{DD_HV}$ and $V_{DD_BV}$ as described in Figure 11.



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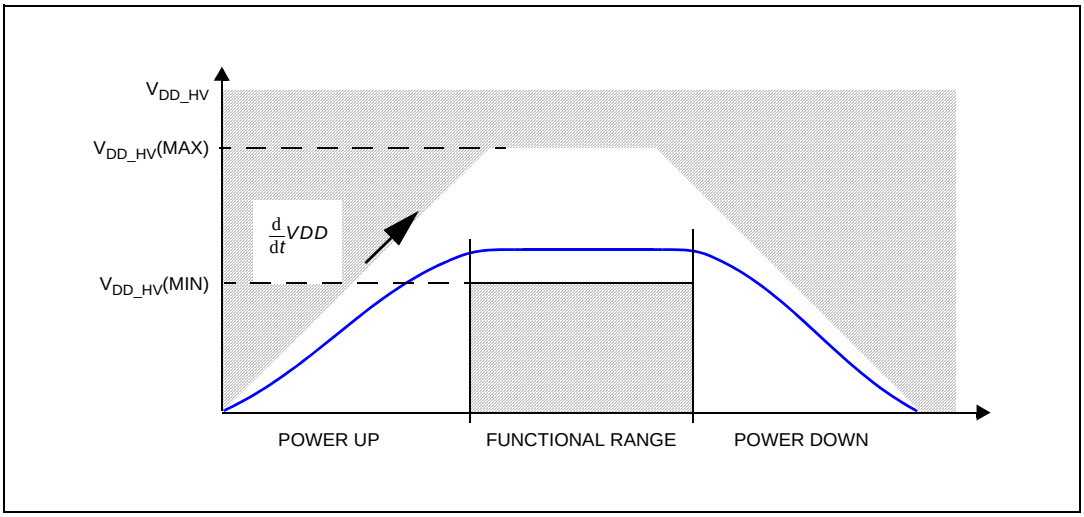


**Figure 11. $V_{DD_HV}$ and $V_{DD_BV}$ maximum slope**

When STANDBY mode is used, further constraints are applied to the both $V_{DD_HV}$ and $V_{DD_BV}$ in order to guarantee correct regulator function during STANDBY exit. This is described on Figure 12.

STANDBY regulator constraints should normally be guaranteed by implementing equivalent of CSTDBY capacitance on application board (capacitance and ESR typical values), but would actually depend on exact characteristics of application external regulator.

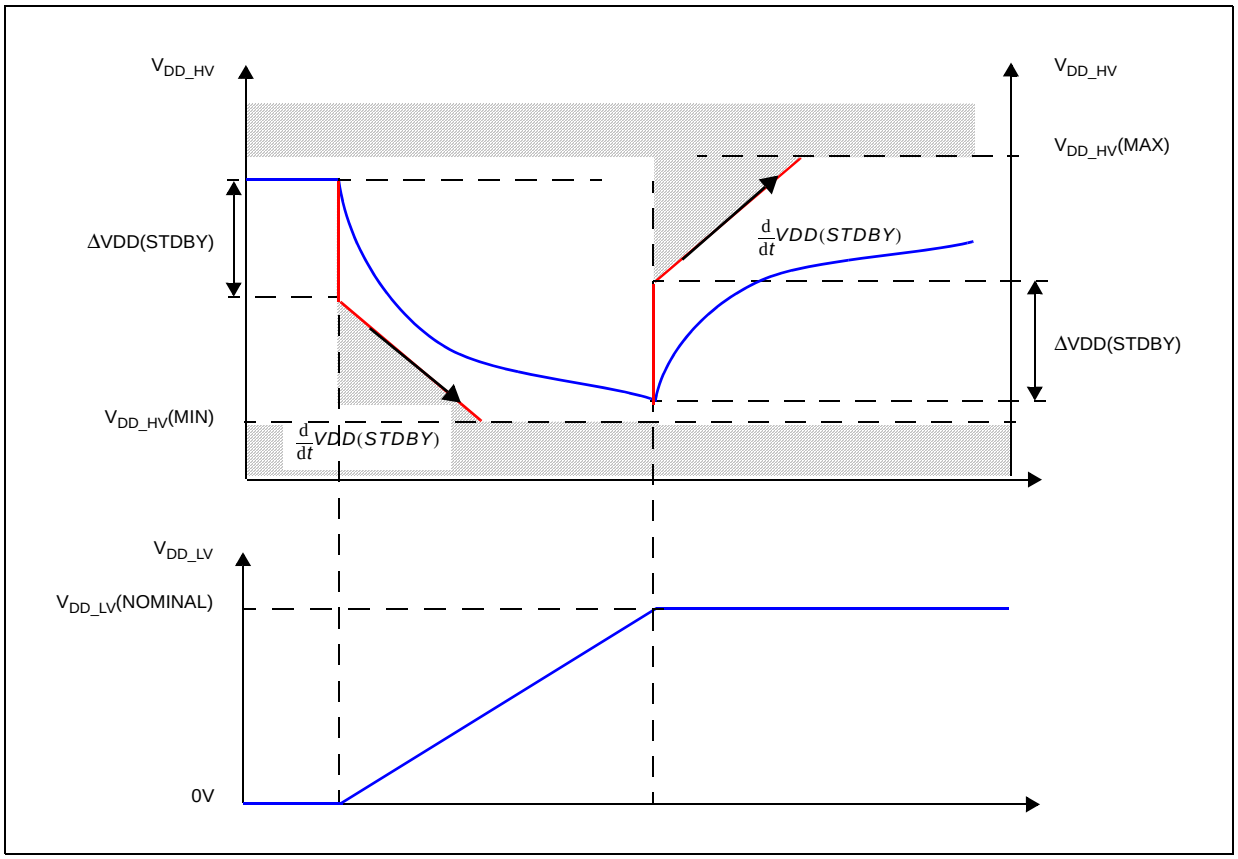


**Figure 12. $V_{DD_HV}$ and $V_{DD_BV}$ supply constraints during STANDBY mode exit**



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**Table 25. Voltage regulator electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $C_{REGn}$ | SR | — | Internal voltage regulator external capacitance | — | 200 | — | 500 | nF |
| $R_{REG}$ | SR | — | Stability capacitor equivalent serial resistance | Range: 10 kHz to 20 MHz | — | — | 0.2 | Ω |
| $C_{DEC1}$ | SR | — | Decoupling capacitance[2] ballast | $V_{DD_BV}/V_{SS_LV}$ pair: $V_{DD_BV}$ = 4.5 V to 5.5 V | 100[3] | 470[4] | — | nF |
| | | | | $V_{DD_BV}/V_{SS_LV}$ pair: $V_{DD_BV}$ = 3 V to 3.6 V | 400 | | — | |
| $C_{DEC2}$ | SR | — | Decoupling capacitance regulator supply | $V_{DD}/V_{SS}$ pair | 10 | 100 | — | nF |
| $\left\|\frac{d}{dt}VDD\right\|$ | SR | — | Maximum slope on $V_{DD}$ | | — | — | 250 | mV/µs |
| $\|\Delta_{VDD(STDBY)}\|$ | SR | — | Maximum instant variation on $V_{DD}$ during standby exit | | — | — | 30 | mV |
| $\left\|\frac{d}{dt}VDD(STDBY)\right\|$ | SR | — | Maximum slope on $V_{DD}$ during standby exit | | — | — | 15 | mV/µs |
| $V_{MREG}$ | CC | T | Main regulator output voltage | Before exiting from reset | — | 1.32 | — | V |
| | | P | | After trimming | 1.16 | 1.28 | — | |
| $I_{MREG}$ | SR | — | Main regulator current provided to $V_{DD_LV}$ domain | — | — | — | 150 | mA |
| $I_{MREGINT}$ | CC | D | Main regulator module current consumption | $I_{MREG}$ = 200 mA | — | — | 2 | mA |
| | | | | $I_{MREG}$ = 0 mA | — | — | 1 | |
| $V_{LPREG}$ | CC | P | Low power regulator output voltage | After trimming | 1.16 | 1.28 | — | V |
| $I_{LPREG}$ | SR | — | Low power regulator current provided to $V_{DD_LV}$ domain | — | — | — | 15 | mA |
| $I_{LPREGINT}$ | CC | D | Low power regulator module current consumption | $I_{LPREG}$ = 15 mA; $T_A$ = 55 °C | — | — | 600 | µA |
| | | — | | $I_{LPREG}$ = 0 mA; $T_A$ = 55 °C | — | 5 | — | |
| $V_{ULPREG}$ | CC | P | Ultra low power regulator output voltage | After trimming | 1.16 | 1.28 | — | V |
| $I_{ULPREG}$ | SR | — | Ultra low power regulator current provided to $V_{DD_LV}$ domain | — | — | — | 5 | mA |
| $I_{ULPREGINT}$ | CC | D | Ultra low power regulator module current consumption | $I_{ULPREG}$ = 5 mA; $T_A$ = 55 °C | — | — | 100 | µA |
| | | | | $I_{ULPREG}$ = 0 mA; $T_A$ = 55 °C | — | 2 | — | |



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**Table 25. Voltage regulator electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $I_{DD_BV}$ | CC | D | In-rush average current on $V_{DD_BV}$ during power-up[5] | — | — | — | 300[6] | mA |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 This capacitance value is driven by the constraints of the external voltage regulator supplying the $V_{DD_BV}$ voltage. A typical value is in the range of 470 nF.

3 This value is acceptable to guarantee operation from 4.5 V to 5.5 V

4 External regulator and capacitance circuitry must be capable of providing $I_{DD_BV}$ while maintaining supply $V_{DD_BV}$ in operating range.

5 In-rush average current is seen only for short time (maximum 20 µs) during power-up and on standby exit. It is dependant on the sum of the $C_{REGn}$ capacitances.

6 The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to $I_{MREG}$ value for minimum amount of current to be provided in cc.

The $|\Delta_{VDD(STDBY)}|$ and dVDD(STDBY)/dt system requirement can be used to define the component used for the $V_{DD}$ supply generation. The following two examples describe how to calculate capacitance size:

**Example 1. No regulator (worst case)**

The $|\Delta_{VDD(STDBY)}|$ parameter can be seen as the $V_{DD}$ voltage drop through the ESR resistance of the regulator stability capacitor when the $I_{DD_BV}$ current required to load $V_{DD_LV}$ domain during the standby exit. It is thus possible to define the maximum equivalent resistance $ESR_{STDBY}(MAX)$ of the total capacitance on the $V_{DD}$ supply:

$$ESR_{STDBY}(MAX) = |\Delta_{VDD(STDBY)}|/I_{DD_BV} = (30\ mV)/(300\ mA) = 0.1\Omega\ ^{1}$$

The dVDD(STDBY)/dt parameter can be seen as the $V_{DD}$ voltage drop at the capacitance pin (excluding ESR drop) while providing the $I_{DD_BV}$ supply required to load $V_{DD_LV}$ domain during the standby exit. It is thus possible to define the minimum equivalent capacitance $C_{STDBY}(MIN)$ of the total capacitance on the $V_{DD}$ supply:

$$C_{STDBY}(MIN) = I_{DD_BV}/dVDD(STDBY)/dt = (300\ mA)/(15\ mV/\mu s) = 20\ \mu F$$

This configuration is a worst case, with the assumption no regulator is available.

**Example 2. Simplified regulator**

The regulator should be able to provide significant amount of the current during the standby exit process. For example, in case of an ideal voltage regulator providing 200 mA current, it is possible to recalculate the equivalent $ESR_{STDBY}(MAX)$ and $C_{STDBY}(MIN)$ as follows:

$$ESR_{STDBY}(MAX) = |\Delta_{VDD(STDBY)}|/(I_{DD_BV} - 200\ mA) = (30\ mV)/(100\ mA) = 0.3\ \Omega$$

$$C_{STDBY}(MIN) = (I_{DD_BV} - 200\ mA)/dVDD(STDBY)/dt = (300\ mA - 200\ mA)/(15\ mV/\mu s) = 6.7\ \mu F$$

In case optimization is required, $C_{STDBY}(MIN)$ and $ESR_{STDBY}(MAX)$ should be calculated based on the regulator characteristics as well as the board $V_{DD}$ plane characteristics.

## 2.17.2 Low voltage detector electrical characteristics

The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the $V_{DD}$ and the $V_{DD_LV}$ voltage while device is supplied:

1. Based on typical time for standby exit sequence of 20 µs, ESR(MIN) can actually be considered at ~50 kHz.



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- POR monitors $V_{DD}$ during the power-up phase to ensure device is maintained in a safe reset state (refer to RGM Destructive Event Status (RGM_DES) Register flag F_POR in device reference manual)
- LVDHV3 monitors $V_{DD}$ to ensure device reset below minimum functional supply (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD27 in device reference manual)
- LVDHV5 monitors $V_{DD}$ when application uses device in the 5.0 V ± 10% range (refer to RGM Functional Event Status (RGM_FES) Register flag F_LVD45 in device reference manual)
- LVDLVCOR monitors power domain No. 1 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD1 in device reference manual
- LVDLVBKP monitors power domain No. 0 (refer to RGM Destructive Event Status (RGM_DES) Register flag F_LVD12_PD0 in device reference manual)

## NOTE

When enabled, power domain No. 2 is monitored through LVDLVBKP.

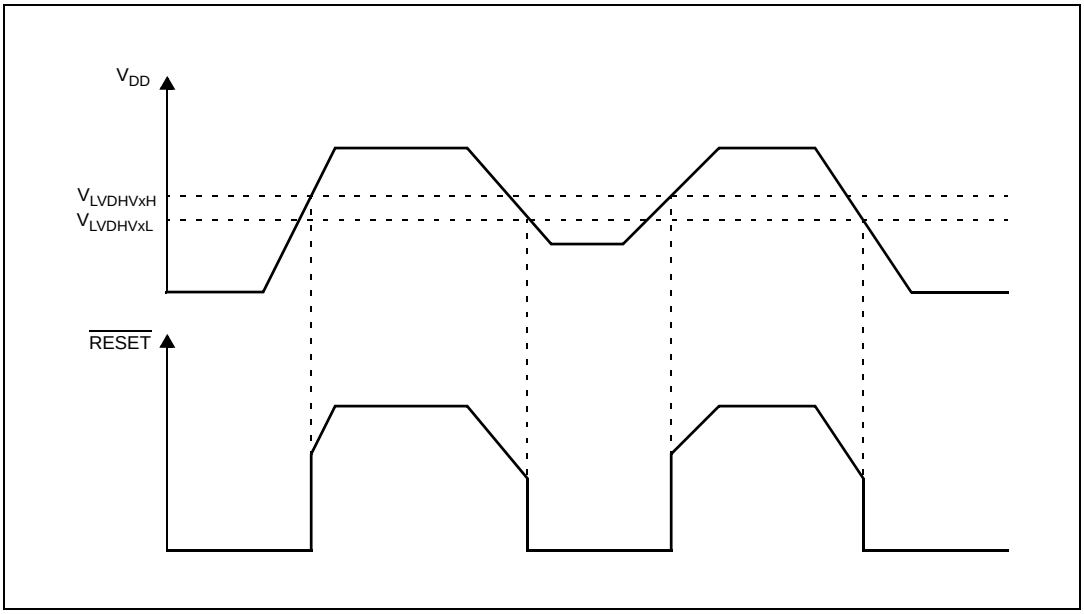


**Figure 13. Low voltage detector vs reset**

## NOTE

Figure 13 (Low voltage detector vs reset) does not apply to LVDHV5 low voltage detector because LVDHV5 is automatically disabled during reset and it must be enabled by software again. Once the device is forced to reset by LVDHV5, the LVDHV5 is disabled and reset is released as soon as internal reset sequence is completed regardless of LVDHV5H threshold.



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**Table 26. Low voltage detector electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{PORUP}$ | SR | P | Supply for functional POR module | — | 1.0 | — | 5.5 | V |
| $V_{PORH}$ | CC | P | Power-on reset threshold | $T_A$ = 25 °C, after trimming | 1.5 | — | 2.6 | |
| | | T | | — | 1.5 | — | 2.6 | |
| $V_{LVDHV3H}$ | CC | T | LVDHV3 low voltage detector high threshold | — | — | — | 2.95 | |
| $V_{LVDHV3L}$ | CC | P | LVDHV3 low voltage detector low threshold | | 2.6 | — | 2.9 | |
| $V_{LVDHV5H}$ | CC | T | LVDHV5 low voltage detector high threshold | | — | — | 4.5 | |
| $V_{LVDHV5L}$ | CC | P | LVDHV5 low voltage detector low threshold | | 3.8 | — | 4.4 | |
| $V_{LVDLVCORL}$ | CC | P | LVDLVCOR low voltage detector low threshold | | 1.08 | — | 1.16 | |
| $V_{LVDLVBKPL}$ | CC | P | LVDLVBKP low voltage detector low threshold | | 1.08 | — | 1.16 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

## 2.18 Power consumption

Table 27 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

**Table 27. Power consumption on VDD_BV and VDD_HV**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{DDMAX}$[2] | CC | D | RUN mode maximum average current | — | | — | 115 | 140[3] | mA |
| $I_{DDRUN}$[4] | CC | T | RUN mode typical average current[5] | $f_{CPU}$ = 8 MHz | | — | 7 | — | mA |
| | | T | | $f_{CPU}$ = 16 MHz | | — | 18 | — | |
| | | T | | $f_{CPU}$ = 32 MHz | | — | 29 | — | |
| | | P | | $f_{CPU}$ = 48 MHz | | — | 40 | 100 | |
| | | P | | $f_{CPU}$ = 64 MHz | | — | 51 | 125 | |
| $I_{DDHALT}$ | CC | C | HALT mode current[6] | Slow internal RC oscillator (128 kHz) running | $T_A$ = 25 °C | — | 8 | 15 | mA |
| | | P | | | $T_A$ = 125 °C | — | 14 | 25 | |
| $I_{DDSTOP}$ | CC | P | STOP mode current[7] | Slow internal RC oscillator (128 kHz) running | $T_A$ = 25 °C | — | 180 | 700[8] | µA |
| | | D | | | $T_A$ = 55 °C | — | 500 | — | |
| | | D | | | $T_A$ = 85 °C | — | 1 | 6[8] | mA |
| | | D | | | $T_A$ = 105 °C | — | 2 | 9[8] | |
| | | P | | | $T_A$ = 125 °C | — | 4.5 | 12[8] | |



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**Table 27. Power consumption on VDD_BV and VDD_HV (continued)**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{DDSTDBY2}$ | CC | P | STANDBY2 mode current[9] | Slow internal RC oscillator (128 kHz) running | $T_A$ = 25 °C | — | 30 | 100 | µA |
| | | D | | | $T_A$ = 55 °C | — | 75 | — | |
| | | D | | | $T_A$ = 85 °C | — | 180 | 700 | |
| | | D | | | $T_A$ = 105 °C | — | 315 | 1000 | |
| | | P | | | $T_A$ = 125 °C | — | 560 | 1700 | |
| $I_{DDSTDBY1}$ | CC | T | STANDBY1 mode current[10] | Slow internal RC oscillator (128 kHz) running | $T_A$ = 25 °C | — | 20 | 60 | µA |
| | | D | | | $T_A$ = 55 °C | — | 45 | — | |
| | | D | | | $T_A$ = 85 °C | — | 100 | 350 | |
| | | D | | | $T_A$ = 105 °C | — | 165 | 500 | |
| | | D | | | $T_A$ = 125 °C | — | 280 | 900 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 $I_{DDMAX}$ is drawn only from the $V_{DD_BV}$ pin. Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

3 Higher current may be sinked by device during power-up and standby exit. Please refer to in rush current on Table 25.

4 $I_{DDRUN}$ is drawn only from the $V_{DD_BV}$ pin. RUN current measured with typical application with accesses on both flash and RAM.

5 Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.

6 Data Flash Power Down. Code Flash in Low Power. SIRC (128 kHz) and FIRC (16 MHz) on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clock gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 clock gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication). RTC/API ON. PIT ON. STM ON. ADC ON but not conversion except 2 analog watchdog.

7 Only for the “P” classification: No clock, FIRC (16 MHz) off, SIRC (128 kHz) on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

8 When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

9 Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.

10 ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.



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# 2.19 Flash memory electrical characteristics

## 2.19.1 Program/Erase characteristics

Table 28 shows the program and erase characteristics.

**Table 28. Program and erase specifications**

| Symbol | | C | Parameter | Value | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Initial max[2] | Max[3] | |
| $T_{dwprogram}$ | CC | C | Double word (64 bits) program time[4] | — | 22 | 50 | 500 | µs |
| $T_{16Kpperase}$ | | | 16 KB block preprogram and erase time | — | 300 | 500 | 5000 | ms |
| $T_{32Kpperase}$ | | | 32 KB block preprogram and erase time | — | 400 | 600 | 5000 | ms |
| $T_{128Kpperase}$ | | | 128 KB block preprogram and erase time | — | 800 | 1300 | 7500 | ms |
| $T_{esus}$ | CC | D | Erase suspend latency | — | — | 30 | 30 | µs |

1 Typical program and erase times assume nominal supply values and operation at 25 °C.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

**Table 29. Flash module life**

| Symbol | | C | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| P/E | CC | C | Number of program/erase cycles per block over the operating temperature range ($T_J$) | 16 KB blocks | 100,000 | — | — | cycles |
| | | | | 32 KB blocks | 10,000 | 100,000 | — | |
| | | | | 128 KB blocks | 1,000 | 100,000 | — | |
| Retention | CC | C | Minimum data retention at 85 °C average ambient temperature[1] | Blocks with 0–1,000 P/E cycles | 20 | — | — | years |
| | | | | Blocks with 1,001–10,000 P/E cycles | 10 | — | — | |
| | | | | Blocks with 10,001–100,000 P/E cycles | 5 | — | — | |

1 Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.



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**Table 30. Flash read access timing**

| Symbol | | C | Parameter | Conditions[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{READ}$ | CC | P | Maximum frequency for Flash reading | 2 wait states | 64 | MHz |
| | | C | | 1 wait state | 40 | |
| | | C | | 0 wait states | 20 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

## 2.19.2 Flash power supply DC characteristics

Table 31 shows the power supply DC characteristics on external supply.

**Table 31. Flash memory power supply DC electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $I_{FREAD}$[2] | CC | D | Sum of the current consumption on VDD_HV and VDD_BV on read access | Code flash memory module read $f_{CPU}$ = 64 MHz[3] | — | 15 | 33 | mA |
| | | | | Data flash memory module read $f_{CPU}$ = 64 MHz[3] | — | 15 | 33 | |
| $I_{FMOD}$[2] | CC | D | Sum of the current consumption on VDD_HV and VDD_BV on matrix modification (program/erase) | Program/Erase ongoing while reading code flash memory registers $f_{CPU}$ = 64 MHz[3] | — | 15 | 33 | mA |
| | | | | Program/Erase ongoing while reading data flash memory registers $f_{CPU}$ = 64 MHz[3] | — | 15 | 33 | |
| $I_{FLPW}$ | CC | D | Sum of the current consumption on VDD_HV and VDD_BV | During code flash memory low-power mode | — | — | 900 | µA |
| | | | | During data flash memory low-power mode | — | — | 900 | |
| $I_{FPWD}$ | CC | D | Sum of the current consumption on VDD_HV and VDD_BV | During code flash memory power-down mode | — | — | 150 | µA |
| | | | | During data flash memory power-down mode | — | — | 150 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 This value is only relative to the actual duration of the read cycle

3 $f_{CPU}$ 64 MHz can be achieved only at up to 105 °C



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## 2.19.3 Start-up/Switch-off timings

**Table 32. Start-up time/Switch-off time**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $T_{FLARSTEXIT}$ | CC | T | Delay for Flash module to exit reset mode | Code Flash | — | — | 125 | µs |
| | | T | | Data Flash | — | — | 125 | |
| $T_{FLALPEXIT}$ | CC | T | Delay for Flash module to exit low-power mode | Code Flash | — | — | 0.5 | |
| | | T | | Data Flash | — | — | 0.5 | |
| $T_{FLAPDEXIT}$ | CC | T | Delay for Flash module to exit power-down mode | Code Flash | — | — | 30 | |
| | | T | | Data Flash | — | — | 30 | |
| $T_{FLALPENTRY}$ | CC | T | Delay for Flash module to enter low-power mode | Code Flash | — | — | 0.5 | |
| | | T | | Data Flash | — | — | 0.5 | |
| $T_{FLAPDENTRY}$ | CC | T | Delay for Flash module to enter power-down mode | Code Flash | — | — | 1.5 | |
| | | T | | Data Flash | — | — | 1.5 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

## 2.20 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

### 2.20.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations: The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers...)
- Prequalification trials: Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

### 2.20.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.



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**Table 33. EMI radiated emission measurement[1,2]**

| Symbol | | C | Parameter | Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| — | SR | — | Scan range | — | | 0.150 | — | 1000 | MHz |
| $f_{CPU}$ | SR | — | Operating frequency | — | | — | 64 | — | MHz |
| $V_{DD_LV}$ | SR | — | LV operating voltages | — | | — | 1.28 | — | V |
| $S_{EMI}$ | CC | T | Peak level | $V_{DD}$ = 5 V, $T_A$ = 25 °C, LQFP144 package Test conforming to IEC 61967-2, $f_{OSC}$ = 8 MHz/$f_{CPU}$ = 64 MHz | No PLL frequency modulation | — | — | 18 | dBµV |
| | | | | | ±2% PLL frequency modulation | — | — | 14 | dBµV |

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

## 2.20.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

### 2.20.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**Table 34. ESD absolute maximum ratings[1] [2]**

| Symbol | | C | Ratings | Conditions | Class | Max value | Unit |
|---|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | CC | T | Electrostatic discharge voltage (Human Body Model) | $T_A$ = 25 °C conforming to AEC-Q100-002 | H1C | 2000 | V |
| $V_{ESD(MM)}$ | CC | T | Electrostatic discharge voltage (Machine Model) | $T_A$ = 25 °C conforming to AEC-Q100-003 | M2 | 200 | |
| $V_{ESD(CDM)}$ | CC | T | Electrostatic discharge voltage (Charged Device Model) | $T_A$ = 25 °C conforming to AEC-Q100-011 | C3A | 500 | |
| | | | | | | 750 (corners) | |

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

### 2.20.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.



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These tests are compliant with the EIA/JESD 78 IC latch-up standard.

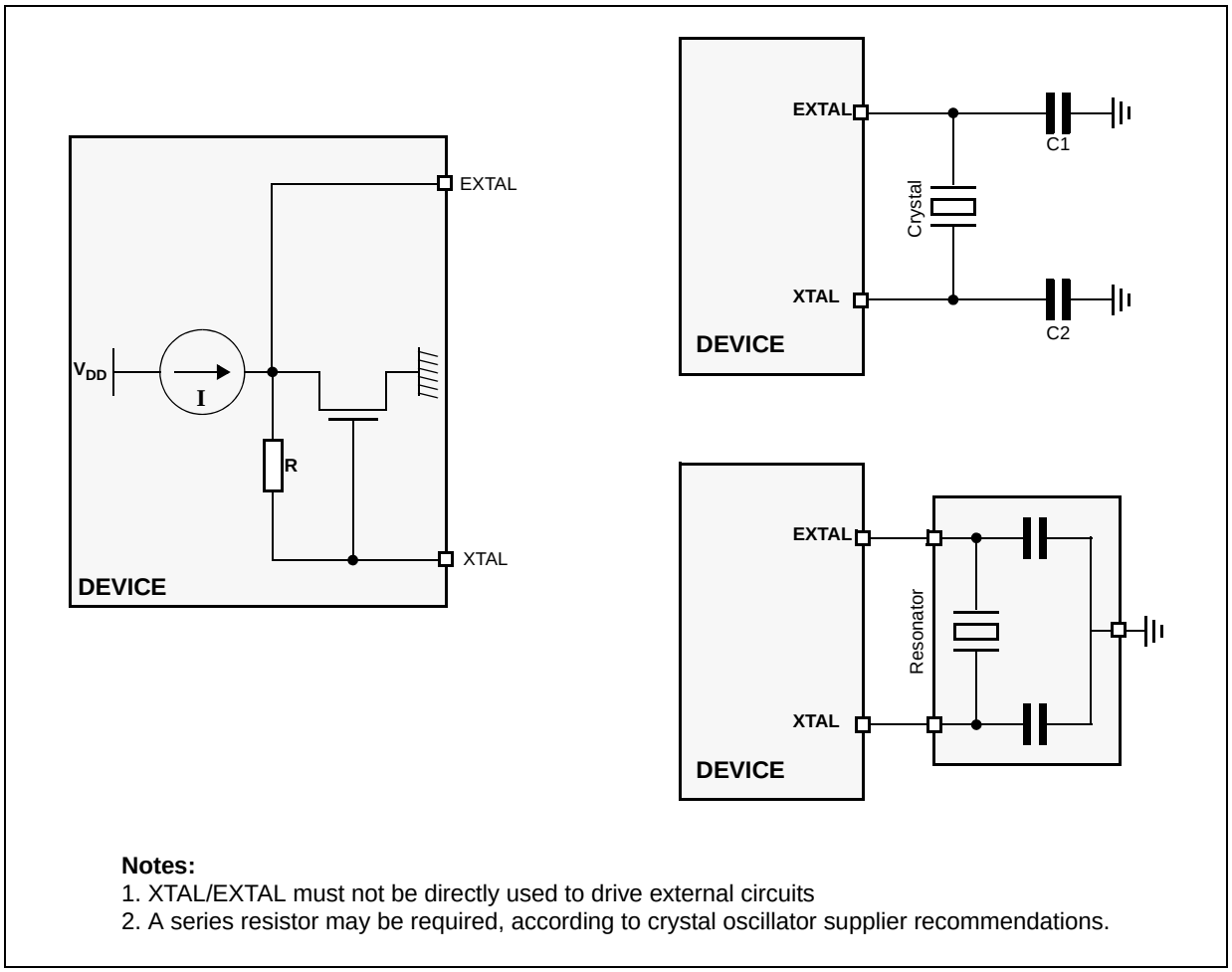
**Table 35. Latch-up results**

| Symbol | | C | Parameter | Conditions | Class |
|---|---|---|---|---|---|
| LU | CC | T | Static latch-up class | $T_A$ = 125 °C conforming to JESD 78 | II level A |

## 2.21 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 14 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 36 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.




**Notes:**
1. XTAL/EXTAL must not be directly used to drive external circuits
2. A series resistor may be required, according to crystal oscillator supplier recommendations.

**Figure 14. Crystal oscillator and resonator connection scheme**



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**Table 36. Crystal description**

| Nominal frequency (MHz) | NDK crystal reference | Crystal equivalent series resistance ESR Ω | Crystal motional capacitance ($C_m$) fF | Crystal motional inductance ($L_m$) mH | Load on xtalin/xtalout C1 = C2 (pF)[1] | Shunt capacitance between xtalout and xtalin C0[2] (pF) |
|---|---|---|---|---|---|---|
| 4 | NX8045GB | 300 | 2.68 | 591.0 | 21 | 2.93 |
| 8 | NX5032GA | 300 | 2.46 | 160.7 | 17 | 3.01 |
| 10 | | 150 | 2.93 | 86.6 | 15 | 2.91 |
| 12 | | 120 | 3.11 | 56.5 | 15 | 2.93 |
| 16 | | 120 | 3.90 | 25.3 | 10 | 3.00 |

1 The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

2 The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

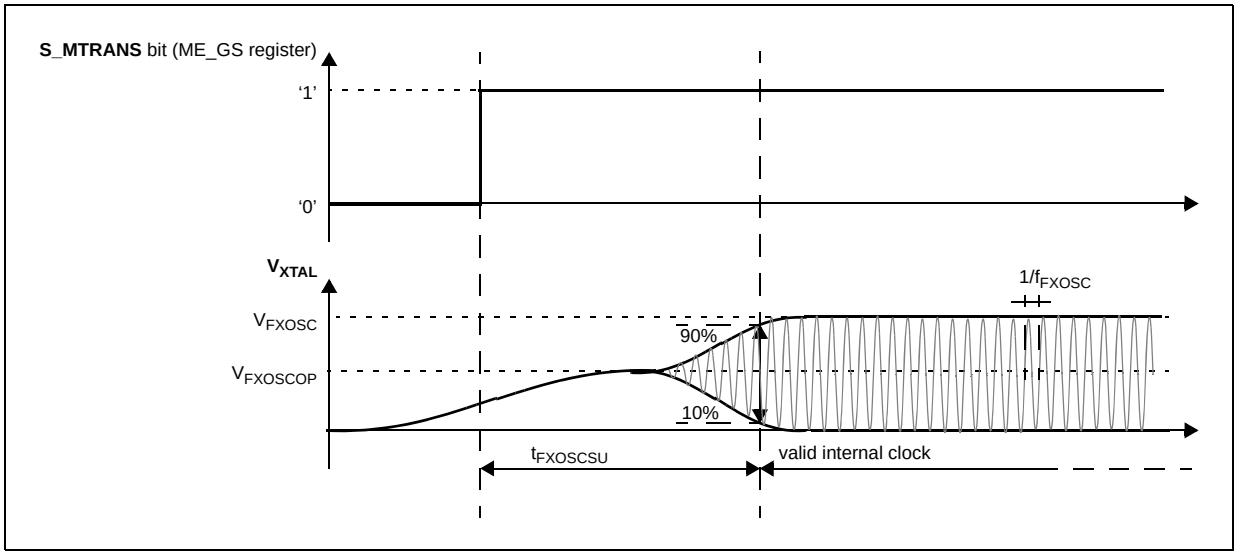


**Figure 15. Fast external crystal oscillator (4 to 16 MHz) timing diagram**



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**Table 37. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{FXOSC}$ | SR | — | Fast external crystal oscillator frequency | — | 4.0 | — | 16.0 | MHz |
| $g_{mFXOSC}$ | CC | C | Fast external crystal oscillator transconductance | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0 | 2.2 | — | 8.2 | mA/V |
| | CC | P | | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0 | 2.0 | — | 7.4 | |
| | CC | C | | $V_{DD}$ = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1 | 2.7 | — | 9.7 | |
| | CC | C | | $V_{DD}$ = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1 | 2.5 | — | 9.2 | |
| $V_{FXOSC}$ | CC | T | Oscillation amplitude at EXTAL | $f_{OSC}$ = 4 MHz, OSCILLATOR_MARGIN = 0 | 1.3 | — | — | V |
| | | | | $f_{OSC}$ = 16 MHz, OSCILLATOR_MARGIN = 1 | 1.3 | — | — | |
| $V_{FXOSCOP}$ | CC | C | Oscillation operating point | — | — | 0.95 | — | V |
| $I_{FXOSC}$[2] | CC | T | Fast external crystal oscillator consumption | — | — | 2 | 3 | mA |
| $t_{FXOSCSU}$ | CC | T | Fast external crystal oscillator start-up time | $f_{OSC}$ = 4 MHz, OSCILLATOR_MARGIN = 0 | — | — | 6 | ms |
| | | | | $f_{OSC}$ = 16 MHz, OSCILLATOR_MARGIN = 1 | — | — | 1.8 | |
| $V_{IH}$ | SR | P | Input high level CMOS (Schmitt Trigger) | Oscillator bypass mode | $0.65V_{DD}$ | — | $V_{DD}$+0.4 | V |
| $V_{IL}$ | SR | P | Input low level CMOS (Schmitt Trigger) | Oscillator bypass mode | –0.4 | — | $0.35V_{DD}$ | V |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified

2 Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals)

## 2.22 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.



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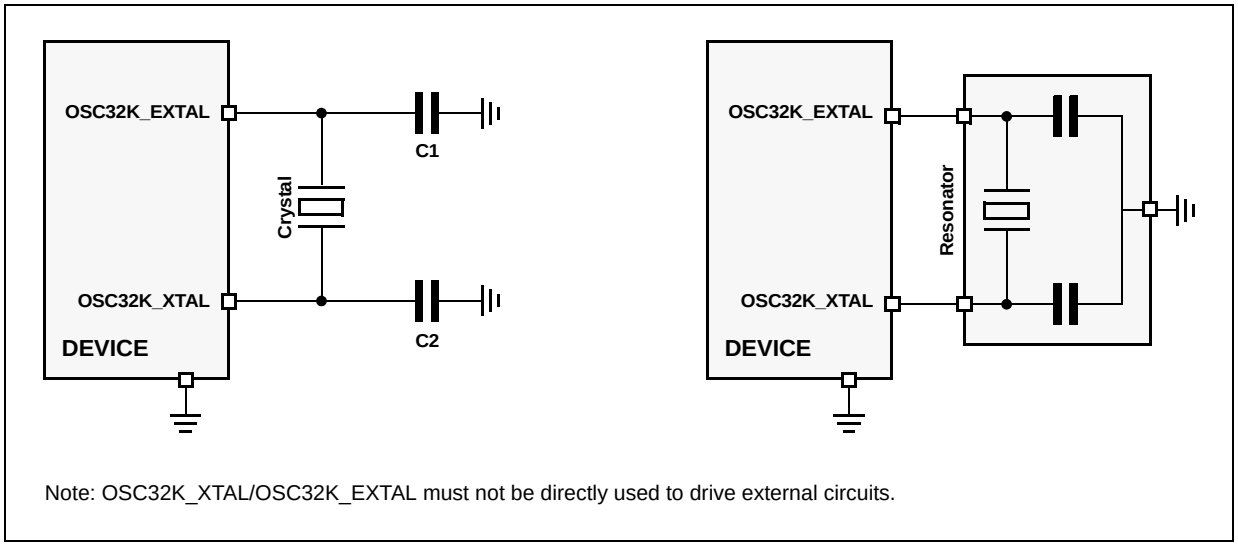


**Figure 16. Crystal oscillator and resonator connection scheme**

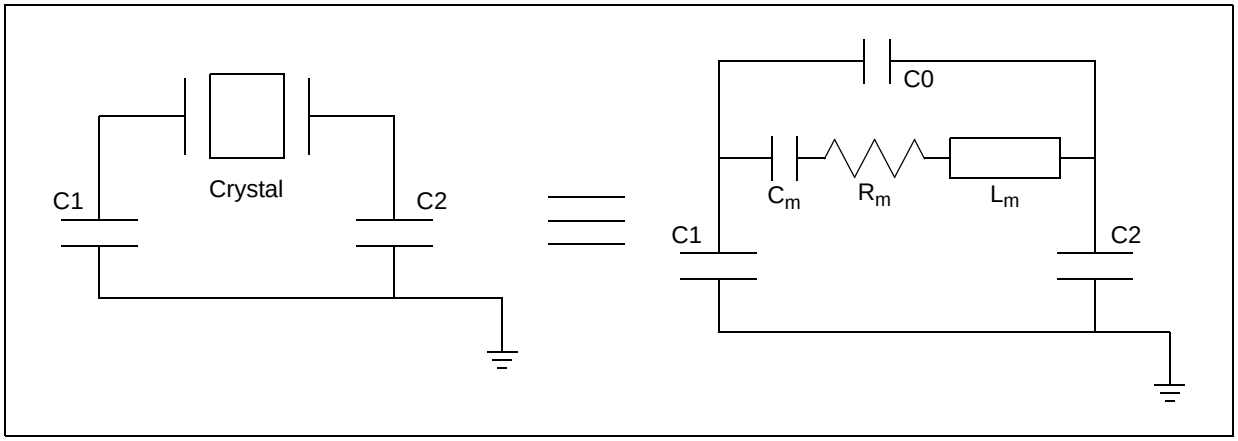


**Figure 17. Equivalent circuit of a quartz crystal**

**Table 38. Crystal motional characteristics[1]**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $L_m$ | Motional inductance | — | — | 11.796 | — | KH |
| $C_m$ | Motional capacitance | — | — | 2 | — | fF |
| C1/C2 | Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground[2] | — | 18 | — | 28 | pF |
| $R_m$[3] | Motional resistance | AC coupled @ C0 = 2.85 pF[4] | — | — | 65 | kΩ |
| | | AC coupled @ C0 = 4.9 pF[4] | — | — | 50 | |
| | | AC coupled @ C0 = 7.0 pF[4] | — | — | 35 | |
| | | AC coupled @ C0 = 9.0 pF[4] | — | — | 30 | |

1 Crystal used: Epson Toyocom MC306



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2 This is the recommended range of load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

3 Maximum ESR ($R_m$) of the crystal is 50 kΩ

4 C0 includes a parasitic capacitance of 2.0 pF between OSC32K_XTAL and OSC32K_EXTAL pins

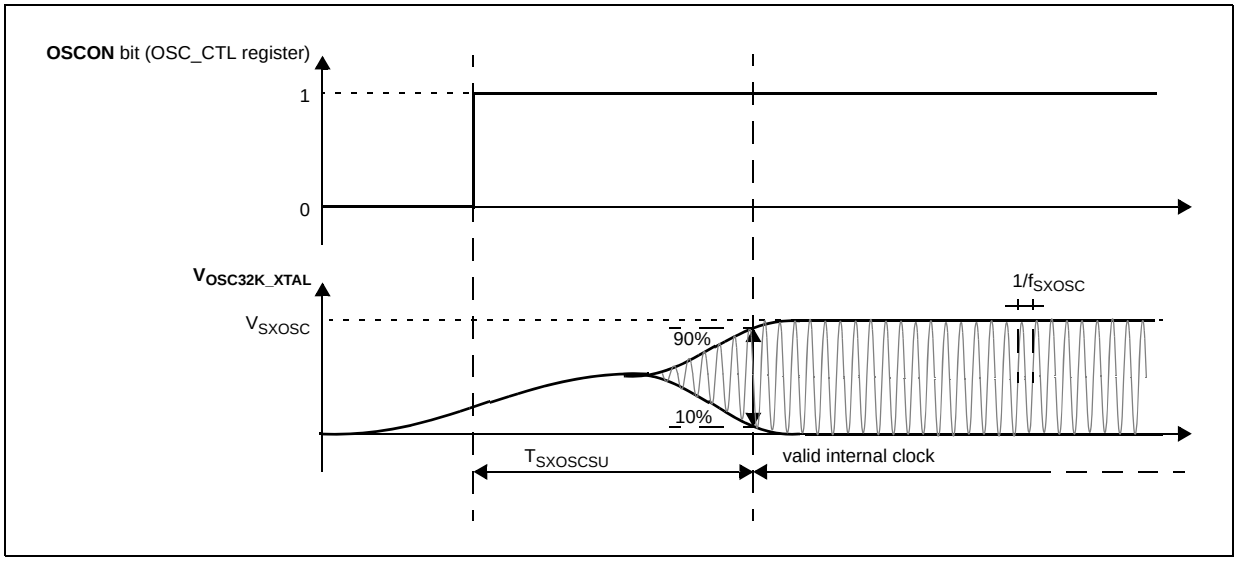


**Figure 18. Slow external crystal oscillator (32 kHz) timing diagram**

**Table 39. Slow external crystal oscillator (32 kHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{SXOSC}$ | SR | — | Slow external crystal oscillator frequency | — | 32 | 32.768 | 40 | kHz |
| $V_{SXOSC}$ | CC | T | Oscillation amplitude | — | — | 2.1 | — | V |
| $I_{SXOSCBIAS}$ | CC | T | Oscillation bias current | — | — | 2.5 | — | µA |
| $I_{SXOSC}$ | CC | T | Slow external crystal oscillator consumption | — | — | — | 8 | µA |
| $T_{SXOSCSU}$ | CC | T | Slow external crystal oscillator start-up time | — | — | — | 2[2] | s |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified. Values are specified for no neighbor GPIO pin activity. If oscillator is enabled (OSC32K_XTAL and OSC32K_EXTAL pins), neighboring pins should not toggle.

2 Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal.

## 2.23 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.



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**Table 40. FMPLL electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{PLLIN}$ | SR | — | FMPLL reference clock[2] | — | 4 | — | 64 | MHz |
| $\Delta_{PLLIN}$ | SR | — | FMPLL reference clock duty cycle[2] | — | 40 | — | 60 | % |
| $f_{PLLOUT}$ | CC | D | FMPLL output clock frequency | — | 16 | — | 64 | MHz |
| $f_{VCO}$[3] | CC | P | VCO frequency without frequency modulation | — | 256 | — | 512 | MHz |
| | | C | VCO frequency with frequency modulation | — | 245 | — | 533 | |
| $f_{CPU}$ | SR | — | System clock frequency | — | — | — | 64 | MHz |
| $f_{FREE}$ | CC | P | Free-running frequency | — | 20 | — | 150 | MHz |
| $t_{LOCK}$ | CC | P | FMPLL lock time | Stable oscillator ($f_{PLLIN}$ = 16 MHz) | — | 40 | 100 | µs |
| $\Delta t_{STJIT}$ | CC | — | FMPLL short term jitter[4] | $f_{sys}$ maximum | –4 | — | 4 | % |
| $\Delta t_{LTJIT}$ | CC | — | FMPLL long term jitter | $f_{PLLIN}$ = 16 MHz (resonator), $f_{PLLCLK}$ @ 64 MHz, 4000 cycles | — | — | 10 | ns |
| $I_{PLL}$ | CC | C | FMPLL consumption | $T_A$ = 25 °C | — | — | 4 | mA |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.

2 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify $f_{PLLIN}$ and $\Delta_{PLLIN}$.

3 Frequency modulation is considered ±4%

4 Short term jitter is measured on the clock rising edge at cycle n and n+4.

## 2.24 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator. This is used as the default clock at the power-up of the device.

**Table 41. Fast internal RC oscillator (16 MHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{FIRC}$ | CC | P | Fast internal RC oscillator high frequency | $T_A$ = 25 °C, trimmed | — | 16 | — | MHz |
| | SR | — | | — | 12 | | 20 | |
| $I_{FIRCRUN}$[2], | CC | T | Fast internal RC oscillator high frequency current in running mode | $T_A$ = 25 °C, trimmed | — | — | 200 | µA |
| $I_{FIRCPWD}$ | CC | D | Fast internal RC oscillator high frequency current in power down mode | $T_A$ = 125 °C | — | — | 10 | µA |



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**Table 41. Fast internal RC oscillator (16 MHz) electrical characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{FIRCSTOP}$ | CC | T | Fast internal RC oscillator high frequency and system clock current in stop mode | $T_A$ = 25 °C | sysclk = off | — | 500 | — | µA |
| | | | | | sysclk = 2 MHz | — | 600 | — | |
| | | | | | sysclk = 4 MHz | — | 700 | — | |
| | | | | | sysclk = 8 MHz | — | 900 | — | |
| | | | | | sysclk = 16 MHz | — | 1250 | — | |
| $t_{FIRCSU}$ | CC | C | Fast internal RC oscillator start-up time | $V_{DD}$ = 5.0 V ± 10% | | — | 1.1 | 2.0 | µs |
| $\Delta_{FIRCPRE}$ | CC | T | Fast internal RC oscillator precision after software trimming of $f_{FIRC}$ | $T_A$ = 25 °C | | –1 | — | +1 | % |
| $\Delta_{FIRCTRIM}$ | CC | T | Fast internal RC oscillator trimming step | $T_A$ = 25 °C | | — | 1.6 | | % |
| $\Delta_{FIRCVAR}$ | CC | P | Fast internal RC oscillator variation in over temperature and supply with respect to $f_{FIRC}$ at $T_A$ = 25 °C in high-frequency configuration | — | | –5 | — | +5 | % |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

## 2.25 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

**Table 42. Slow internal RC oscillator (128 kHz) electrical characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $f_{SIRC}$ | CC | P | Slow internal RC oscillator low frequency | $T_A$ = 25 °C, trimmed | — | 128 | — | kHz |
| | SR | — | | — | 100 | — | 150 | |
| $I_{SIRC}$[2], | CC | C | Slow internal RC oscillator low frequency current | $T_A$ = 25 °C, trimmed | — | — | 5 | µA |
| $t_{SIRCSU}$ | CC | P | Slow internal RC oscillator start-up time | $T_A$ = 25 °C, $V_{DD}$ = 5.0 V ± 10% | — | 8 | 12 | µs |
| $\Delta_{SIRCPRE}$ | CC | C | Slow internal RC oscillator precision after software trimming of $f_{SIRC}$ | $T_A$ = 25 °C | –2 | — | +2 | % |
| $\Delta_{SIRCTRIM}$ | CC | C | Slow internal RC oscillator trimming step | — | — | 2.7 | — | |
| $\Delta_{SIRCVAR}$ | CC | C | Slow internal RC oscillator variation in temperature and supply with respect to $f_{SIRC}$ at $T_A$ = 55 °C in high frequency configuration | High frequency configuration | –10 | — | +10 | % |



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1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.
2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.



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# 2.26 ADC electrical characteristics

## 2.26.1 Introduction

The device provides a 10-bit Successive Approximation Register (SAR) analog-to-digital converter.

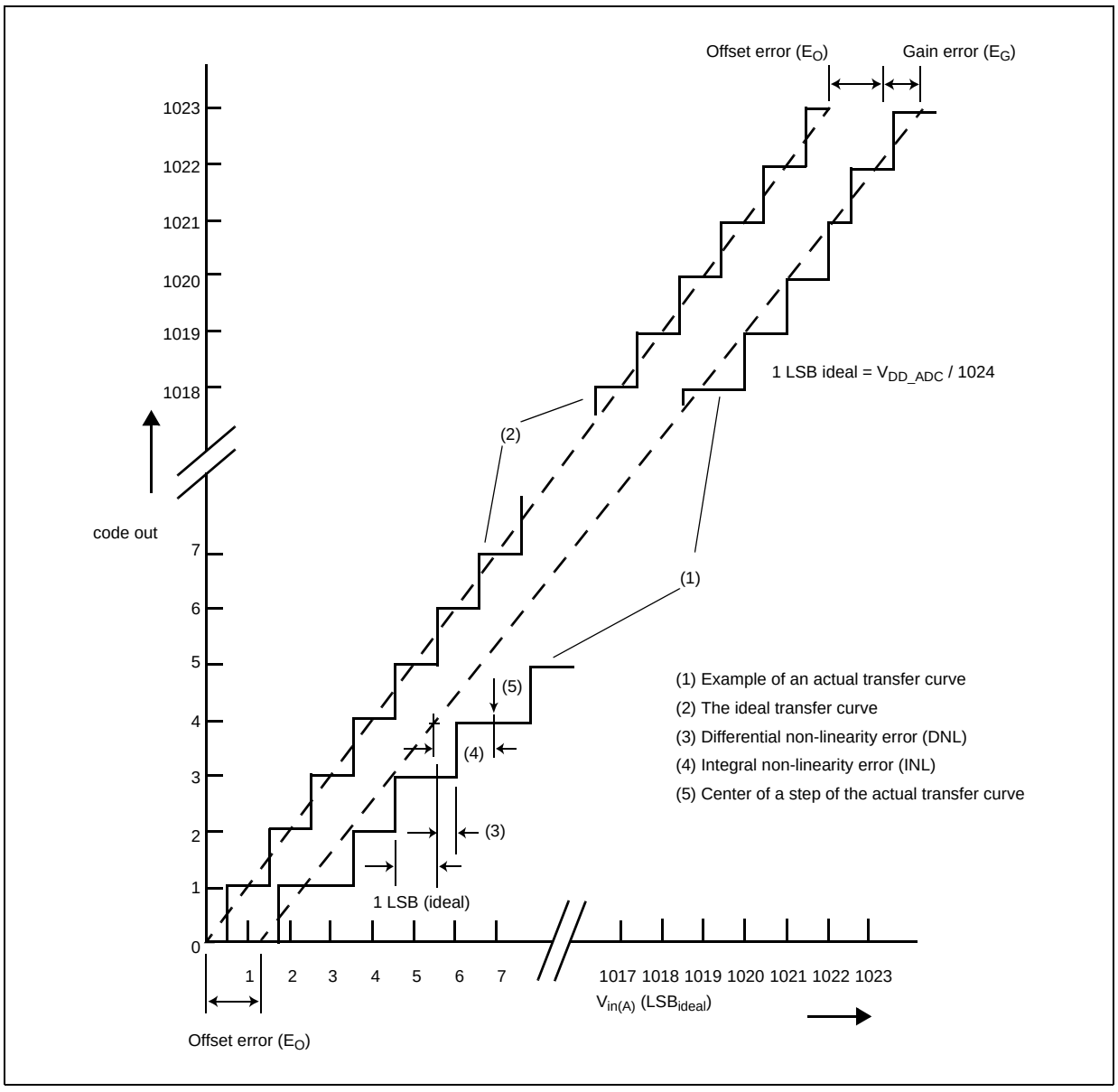


**Figure 19. ADC characteristic and error definitions**

## 2.26.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as



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possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: being $C_S$ and $C_{p2}$ substantially two switched capacitances, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with $C_S$+$C_{p2}$ equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_c \times (C_S+C_{p2}))$, where $f_c$ represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S$+$C_{p2}$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the Equation 4:

***Eqn. 4***

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on a resistive path.

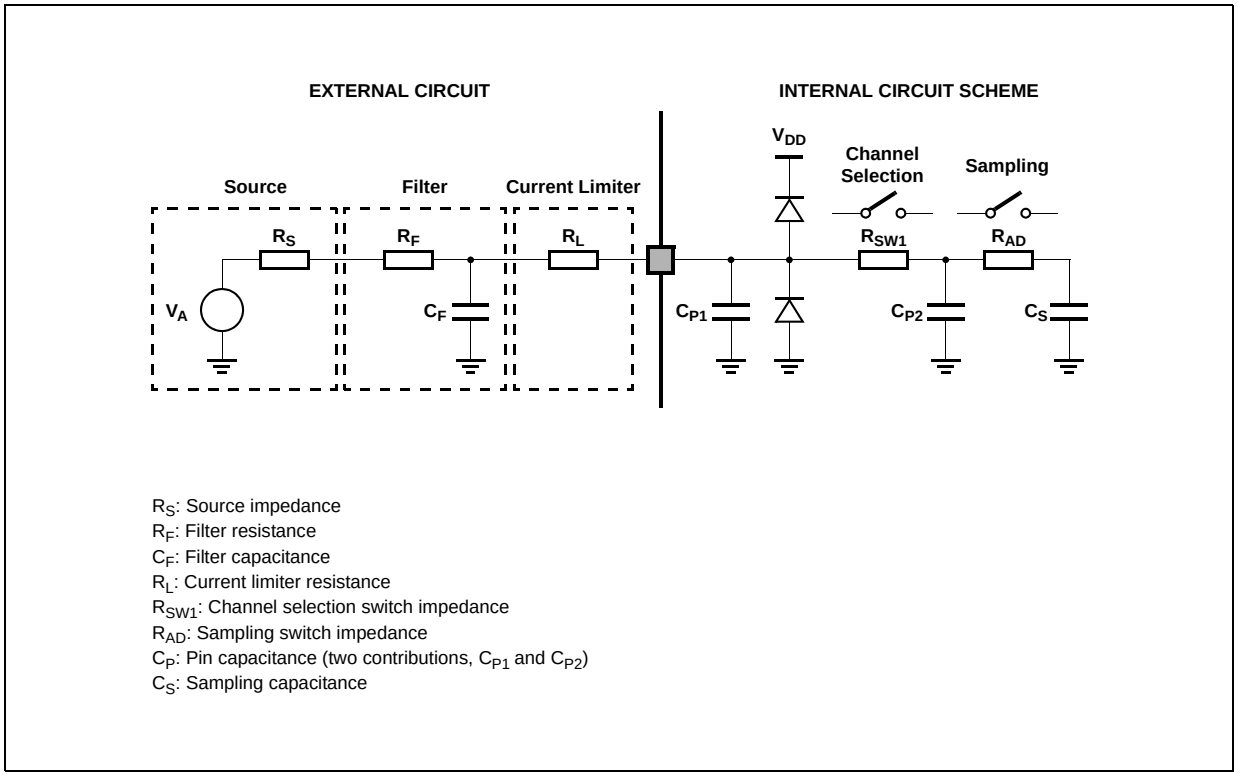


**Figure 20. Input equivalent circuit (precise channels)**



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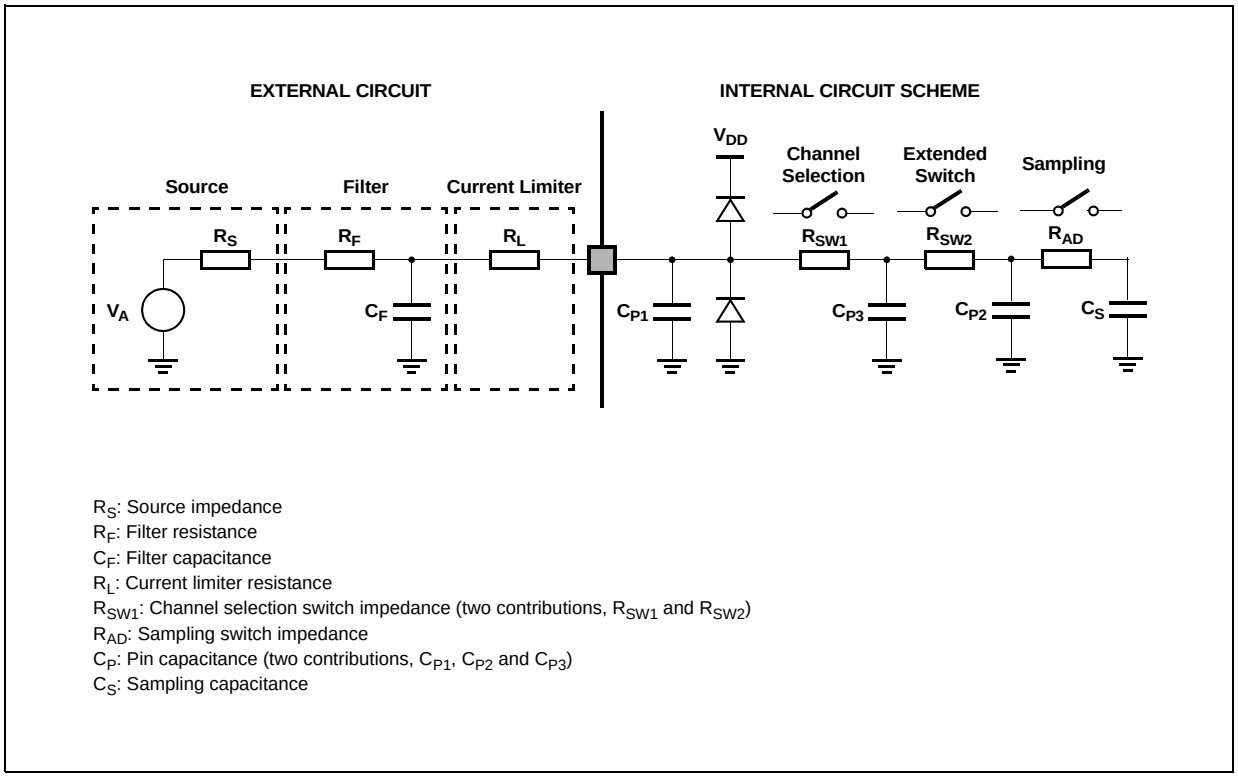


**Figure 21. Input equivalent circuit (extended channels)**

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances $C_F$, $C_{P1}$ and $C_{P2}$ are initially charged at the source voltage $V_A$ (refer to the equivalent circuit in Figure 20): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

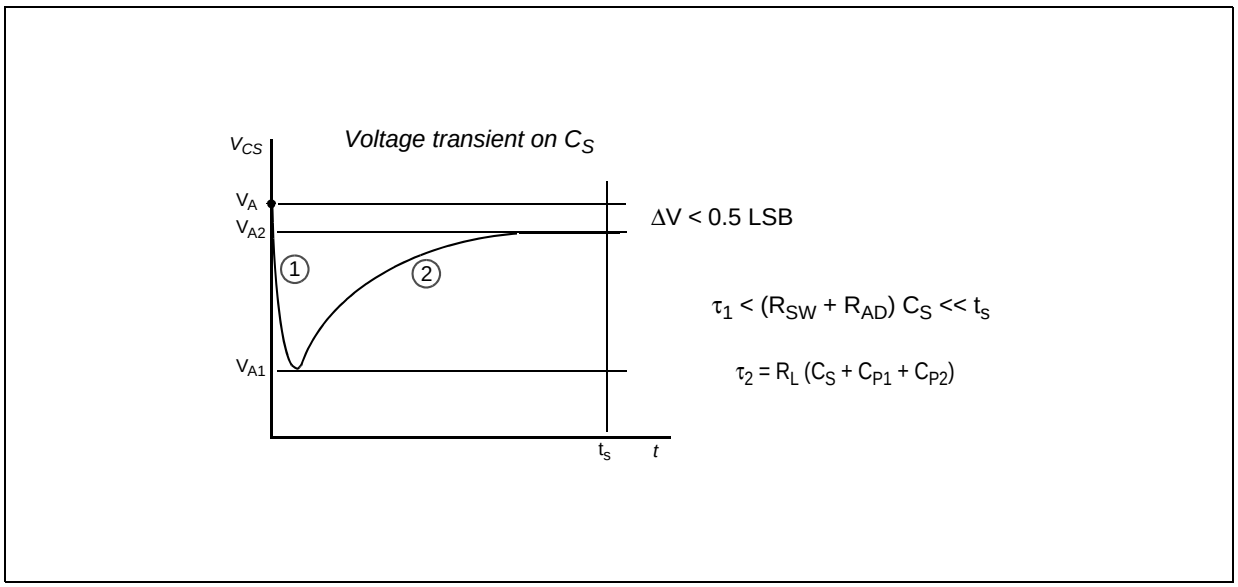


**Figure 22. Transient behavior during sampling phase**

In particular two different transient periods can be distinguished:



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1. A first and quick charge transfer from the internal capacitance $C_{P1}$ and $C_{P2}$ to the sampling capacitance $C_S$ occurs ($C_S$ is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which $C_{P2}$ is reported in parallel to $C_{P1}$ (call $C_P = C_{P1} + C_{P2}$), the two capacitances $C_P$ and $C_S$ are in series, and the time constant is

***Eqn. 5***

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only $C_S$ as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time $t_s$ is always much longer than the internal time constant:

***Eqn. 6***

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll t_s$$

The charge of $C_{P1}$ and $C_{P2}$ is redistributed also on $C_S$, determining a new value of the voltage $V_{A1}$ on the capacitance according to Equation 7:

***Eqn. 7***

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also $C_F$ (that is typically bigger than the on-chip capacitance) through the resistance $R_L$: again considering the worst case in which $C_{P2}$ and $C_S$ were in parallel to $C_{P1}$ (since the time constant in reality would be faster), the time constant is:

***Eqn. 8***

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time $t_s$, a constraints on $R_L$ sizing is obtained:

***Eqn. 9***

$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

Of course, $R_L$ shall be sized also according to the current limitation constraints, in combination with $R_S$ (source impedance) and $R_F$ (filter resistance). Being $C_F$ definitively bigger than $C_{P1}$, $C_{P2}$ and $C_S$, then the final voltage $V_{A2}$ (at the end of the charge transfer transient) will be much higher than $V_{A1}$. Equation 10 must be respected (charge balance assuming now $C_S$ already charged at $V_{A1}$):

***Eqn. 10***

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on $C_S$ with respect to the ideal source $V_A$; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time ($t_s$). The filter is typically designed to act as anti-aliasing.



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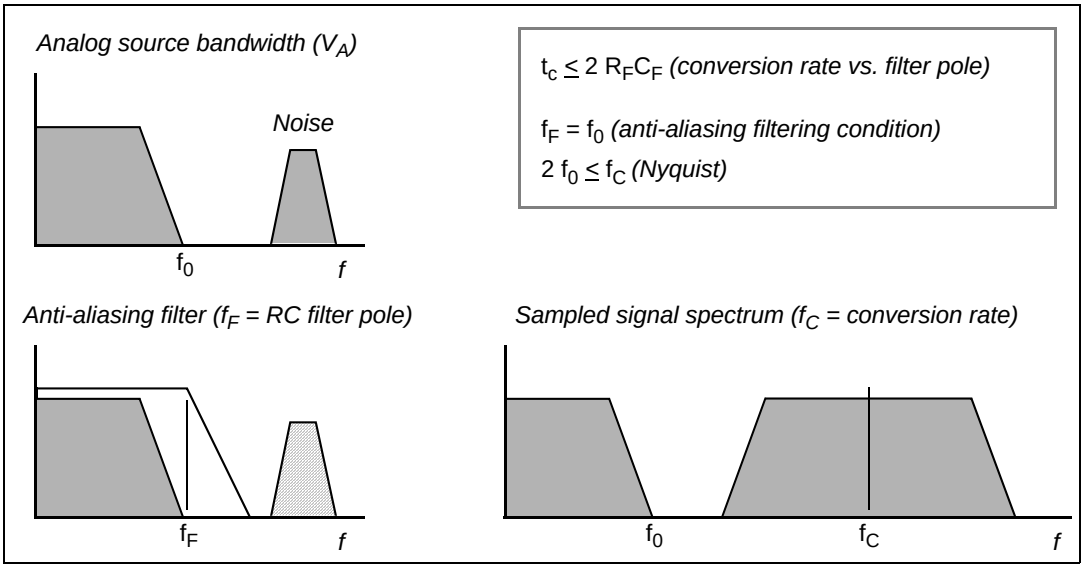


**Figure 23. Spectral representation of input signal**

Calling $f_0$ the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, $f_F$), according to the Nyquist theorem the conversion rate $f_C$ must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period ($t_c$). Again the conversion period $t_c$ is longer than the sampling time $t_s$, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time $t_s$, so the charge level on $C_S$ cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on $C_S$; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on $C_S$:

***Eqn. 11***

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when $V_A$ is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on $C_F$ value:

***Eqn. 12***

$$C_F > 2048 \bullet C_S$$



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## 2.26.3 ADC electrical characteristics

**Table 43. ADC input leakage current**

| Symbol | | C | Parameter | Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $I_{LKG}$ | CC | D | Input leakage current | $T_A$ = –40 °C | No current injection on adjacent pin | — | 1 | 70 | nA |
| | | D | | $T_A$ = 25 °C | | — | 1 | 70 | |
| | | D | | $T_A$ = 85 °C | | — | 3 | 100 | |
| | | D | | $T_A$ = 105 °C | | — | 8 | 200 | |
| | | P | | $T_A$ = 125 °C | | — | 45 | 400 | |

**Table 44. ADC conversion characteristics**

| Symbol | | C | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| $V_{SS_ADC}$ | SR | — | Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground ($V_{SS}$)[2] | — | –0.1 | — | 0.1 | V |
| $V_{DD_ADC}$ | SR | — | Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground ($V_{SS}$) | — | $V_{DD}$–0.1 | — | $V_{DD}$+0.1 | V |
| $V_{AINx}$ | SR | — | Analog input voltage[3] | — | $V_{SS_ADC}$–0.1 | — | $V_{DD_ADC}$+0.1 | V |
| $f_{ADC}$ | SR | — | ADC analog frequency | — | 6 | — | 32 + 4% | MHz |
| $\Delta_{ADC_SYS}$ | SR | — | ADC digital clock duty cycle (ipg_clk) | ADCLKSEL = 1[4] | 45 | — | 55 | % |
| $I_{ADCPWD}$ | SR | — | ADC0 consumption in power down mode | — | — | — | 50 | µA |
| $I_{ADCRUN}$ | SR | — | ADC0 consumption in running mode | — | — | — | 4 | mA |
| $t_{ADC_PU}$ | SR | — | ADC power up delay | — | — | — | 1.5 | µs |
| $t_s$ | CC | T | Sampling time[5] | $f_{ADC}$ = 32 MHz, INPSAMP = 17 | 0.5 | — | | µs |
| | | | | $f_{ADC}$ = 6 MHz, INPSAMP = 255 | — | — | 42 | |
| $t_c$ | CC | P | Conversion time[6] | $f_{ADC}$ = 32 MHz, INPCMP = 2 | 0.625 | — | | µs |
| $C_S$ | CC | D | ADC input sampling capacitance | — | — | — | 3 | pF |
| $C_{P1}$ | CC | D | ADC input pin capacitance 1 | — | — | — | 3 | pF |
| $C_{P2}$ | CC | D | ADC input pin capacitance 2 | — | — | — | 1 | pF |



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**Table 44. ADC conversion characteristics (continued)**

| Symbol | | C | Parameter | Conditions[1] | | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | |
| $C_{P3}$ | CC | D | ADC input pin capacitance 3 | — | | — | — | 1 | pF |
| $R_{SW1}$ | CC | D | Internal resistance of analog source | — | | — | — | 3 | kΩ |
| $R_{SW2}$ | CC | D | Internal resistance of analog source | — | | — | — | 2 | kΩ |
| $R_{AD}$ | CC | D | Internal resistance of analog source | — | | — | — | 2 | kΩ |
| $I_{INJ}$ | SR | — | Input current Injection | Current injection on one ADC input, different from the converted one | $V_{DD}$ = 3.3 V ± 10% | –5 | — | 5 | mA |
| | | | | | $V_{DD}$ = 5.0 V ± 10% | –5 | — | 5 | |
| \| INL \| | CC | T | Absolute value for integral non-linearity | No overload | | — | 0.5 | 1.5 | LSB |
| \| DNL \| | CC | T | Absolute differential non-linearity | No overload | | — | 0.5 | 1.0 | LSB |
| \| $E_O$ \| | CC | T | Absolute offset error | — | | — | 0.5 | — | LSB |
| \| $E_G$ \| | CC | T | Absolute gain error | — | | — | 0.6 | — | LSB |
| TUEp | CC | P | Total unadjusted error[7] for precise channels, input only pins | Without current injection | | –2 | 0.6 | 2 | LSB |
| | | T | | With current injection | | –3 | | 3 | |
| TUEx | CC | T | Total unadjusted error[7] for extended channel | Without current injection | | –3 | 1 | 3 | LSB |
| | | T | | With current injection | | –4 | | 4 | |

1 $V_{DD}$ = 3.3 V ± 10% / 5.0 V ± 10%, $T_A$ = –40 to 125 °C, unless otherwise specified.

2 Analog and digital $V_{SS}$ **must** be common (to be tied together externally).

3 $V_{AINx}$ may exceed $V_{SS_ADC}$ and $V_{DD_ADC}$ limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

4 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

5 During the sampling time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_s$. After the end of the sampling time $t_s$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_s$ depend on programming.

6 This parameter does not include the sampling time $t_s$, but only the time for determining the digital result and the time to load the result's register with the conversion result.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.



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# 2.27 On-chip peripherals

## 2.27.1 Current consumption

**Table 45. On-chip peripherals current consumption[1]**

| Symbol | | C | Parameter | Conditions | | Typical value[2] | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD_BV(CAN)}$ | CC | T | CAN (FlexCAN) supply current on VDD_BV | Bitrate: 500 Kbyte/s | Total (static + dynamic) consumption:<br>• FlexCAN in loop-back mode<br>• XTAL @ 8 MHz used as CAN engine clock source<br>• Message sending period is 580 µs | 8 * $f_{periph}$ + 85 | µA |
| | | | | Bitrate: 125 Kbyte/s | | 8 * $f_{periph}$ + 27 | |
| $I_{DD_BV(eMIOS)}$ | CC | T | eMIOS supply current on VDD_BV | Static consumption:<br>• eMIOS channel OFF<br>• Global prescaler enabled | | 29 * $f_{periph}$ | µA |
| | | | | Dynamic consumption:<br>• It does not change varying the frequency (0.003 mA) | | 3 | |
| $I_{DD_BV(SCI)}$ | CC | T | SCI (LINFlex) supply current on VDD_BV | Total (static + dynamic) consumption:<br>• LIN mode<br>• Baudrate: 20 Kbyte/s | | 5 * $f_{periph}$ + 31 | µA |
| $I_{DD_BV(SPI)}$ | CC | T | SPI (DSPI) supply current on VDD_BV | Ballast static consumption (only clocked) | | 1 | µA |
| | | | | Ballast dynamic consumption (continuous communication):<br>• Baudrate: 2 Mbit/s<br>• Transmission every 8 µs<br>• Frame: 16 bits | | 16 * $f_{periph}$ | |
| $I_{DD_BV(ADC)}$ | CC | T | ADC supply current on VDD_BV | $V_{DD}$ = 5.5 V | Ballast static consumption (no conversion) | 41 * $f_{periph}$ | µA |
| | | | | | Ballast dynamic consumption (continuous conversion)[3] | 5 * $f_{periph}$ | |
| $I_{DD_HV_ADC(ADC)}$ | CC | T | ADC supply current on VDD_HV_ADC | $V_{DD}$ = 5.5 V | Analog static consumption (no conversion) | 2 * $f_{periph}$ | µA |
| | | | | | Analog dynamic consumption (continuous conversion) | 75 * $f_{periph}$ + 32 | |
| $I_{DD_HV(FLASH)}$ | CC | T | Code Flash + Data Flash supply current on VDD_HV | $V_{DD}$ = 5.5 V | — | 8.21 | mA |
| $I_{DD_HV(PLL)}$ | CC | T | PLL supply current on VDD_HV | $V_{DD}$ = 5.5 V | — | 30 * $f_{periph}$ | µA |

1 Operating conditions: $T_A$ = 25 °C, $f_{periph}$ = 8 MHz to 64 MHz

2 $f_{periph}$ is an absolute value.

3 During the conversion, the total current consumption is given from the sum of the static and dynamic consumption, i.e., (41 + 5) * $f_{periph}$.



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## 2.27.2 DSPI characteristics

**Table 46. DSPI characteristics[1]**

| No. | Symbol | | C | Parameter | | DSPI0/DSPI1 | | | DSPI2 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Typ | Max | Min | Typ | Max | |
| 1 | $t_{SCK}$ | SR | D | SCK cycle time | Master mode (MTFE = 0) | 125 | — | — | 333 | — | — | ns |
| | | | D | | Slave mode (MTFE = 0) | 125 | — | — | 333 | — | — | |
| | | | D | | Master mode (MTFE = 1) | 83 | — | — | 125 | — | — | |
| | | | D | | Slave mode (MTFE = 1) | 83 | — | — | 125 | — | — | |
| — | $f_{DSPI}$ | SR | D | DSPI digital controller frequency | | — | — | $f_{CPU}$ | — | — | $f_{CPU}$ | MHz |
| — | $\Delta t_{CSC}$ | CC | D | Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1⟶0 | Master mode | — | — | 130[2] | — | — | 15[3] | ns |
| — | $\Delta t_{ASC}$ | CC | D | Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1⟶1 | Master mode | — | — | 130[3] | — | — | 130[3] | ns |
| 2 | $t_{CSCext}$[4] | SR | D | CS to SCK delay | Slave mode | 32 | — | — | 32 | — | — | ns |
| 3 | $t_{ASCext}$[5] | SR | D | After SCK delay | Slave mode | $1/f_{DSPI} + 5$ | — | — | $1/f_{DSPI} + 5$ | — | — | ns |
| 4 | $t_{SDC}$ | CC | D | SCK duty cycle | Master mode | — | $t_{SCK}/2$ | — | — | $t_{SCK}/2$ | — | ns |
| | | SR | D | | Slave mode | $t_{SCK}/2$ | — | — | $t_{SCK}/2$ | — | — | |
| 5 | $t_A$ | SR | D | Slave access time | Slave mode | — | — | $1/f_{DSPI} + 70$ | — | — | $1/f_{DSPI} + 130$ | ns |
| 6 | $t_{DI}$ | SR | D | Slave SOUT disable time | Slave mode | 7 | — | — | 7 | — | — | ns |
| 7 | $t_{PCSC}$ | SR | D | PCSx to $\overline{PCSS}$ time | | 0 | — | — | 0 | — | — | ns |
| 8 | $t_{PASC}$ | SR | D | $\overline{PCSS}$ to PCSx time | | 0 | — | — | 0 | — | — | ns |
| 9 | $t_{SUI}$ | SR | D | Data setup time for inputs | Master mode | 43 | — | — | 145 | — | — | ns |
| | | | | | Slave mode | 5 | — | — | 5 | — | — | |
| 10 | $t_{HI}$ | SR | D | Data hold time for inputs | Master mode | 0 | — | — | 0 | — | — | ns |
| | | | | | Slave mode | $2^6$ | — | — | $2^6$ | — | — | |
| 11 | $t_{SUO}$[7] | CC | D | Data valid after SCK edge | Master mode | — | — | 32 | — | — | 50 | ns |
| | | | | | Slave mode | — | — | 52 | — | — | 160 | |
| 12 | $t_{HO}$[7] | CC | D | Data hold time for outputs | Master mode | 0 | — | — | 0 | — | — | ns |
| | | | | | Slave mode | 8 | — | — | 13 | — | — | |

1 Operating conditions: $C_L$ = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns.

2 Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.



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3 Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.

4 The $t_{CSC}$ delay value is configurable through a register. When configuring $t_{CSC}$ (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than $\Delta t_{CSC}$ to ensure positive $t_{CSCext}$.

5 The $t_{ASC}$ delay value is configurable through a register. When configuring $t_{ASC}$ (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than $\Delta t_{ASC}$ to ensure positive $t_{ASCext}$.

6 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of the DSPI_MCR.

7 SCK and SOUT configured as MEDIUM pad



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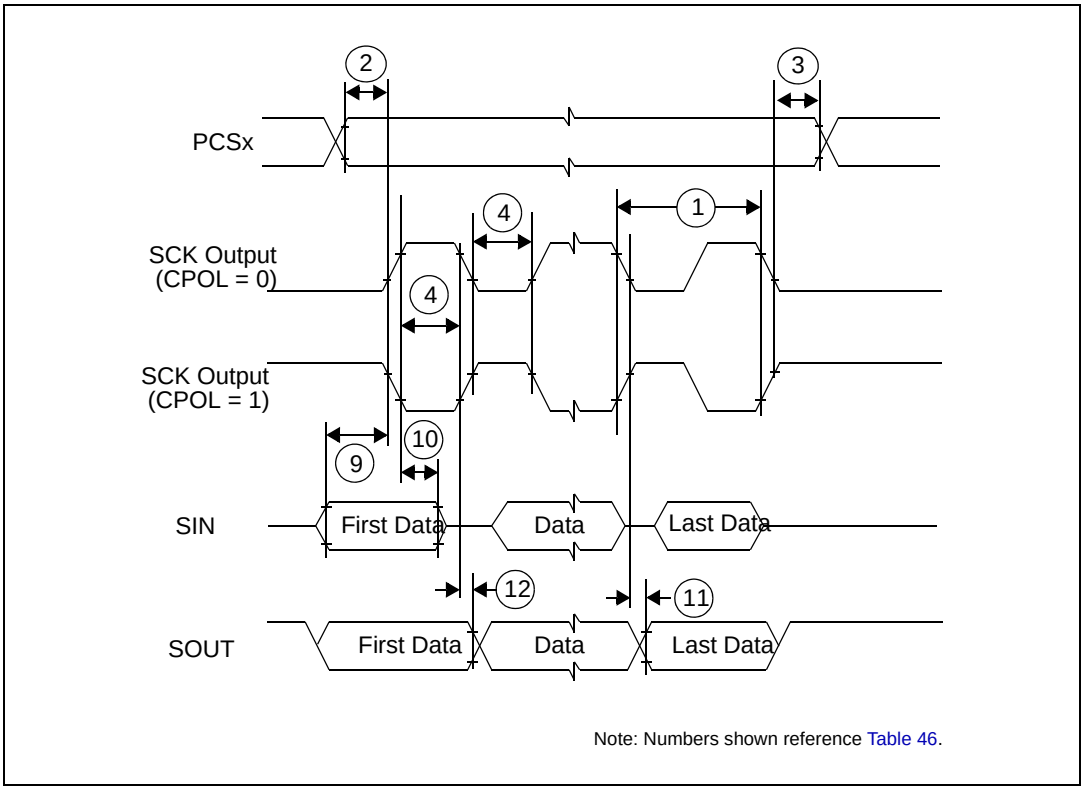


**Figure 24. DSPI classic SPI timing – master, CPHA = 0**

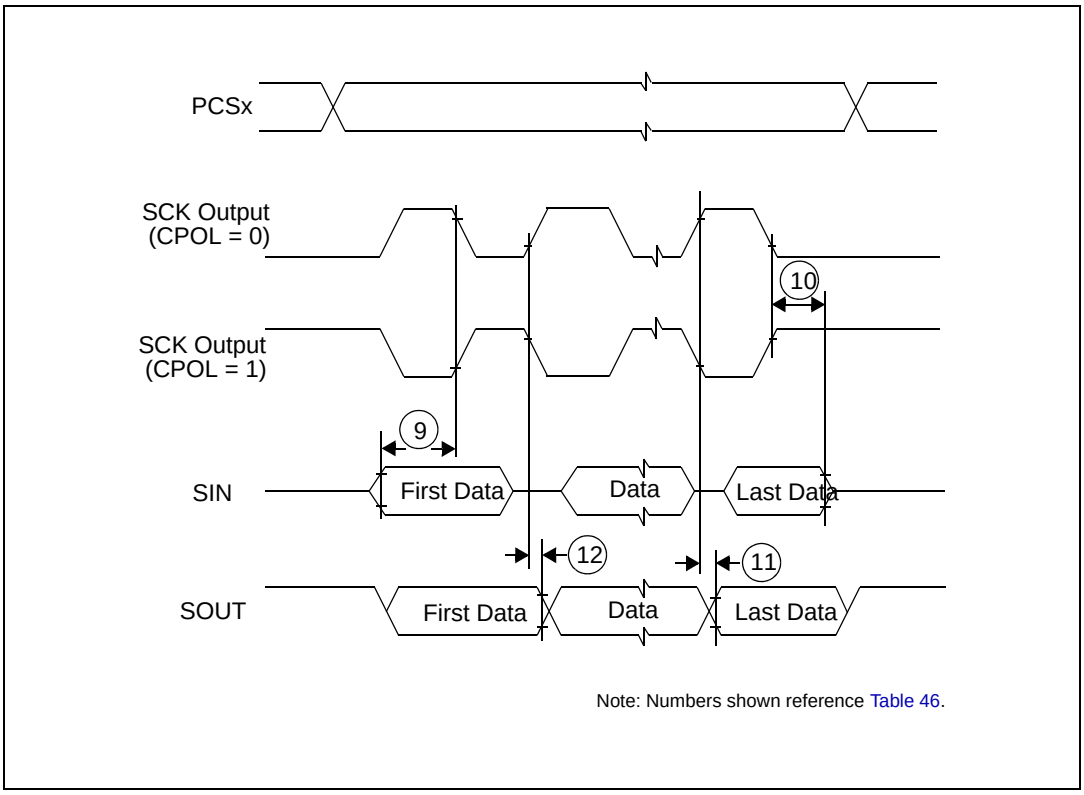


**Figure 25. DSPI classic SPI timing – master, CPHA = 1**



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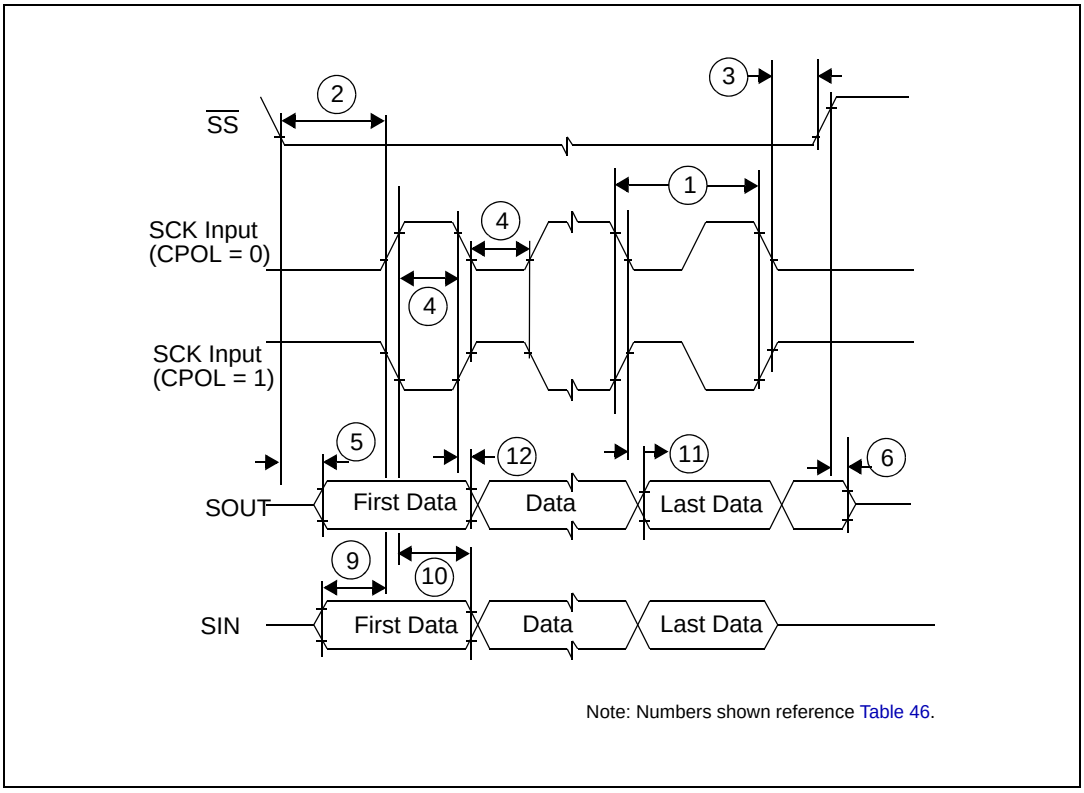


**Figure 26. DSPI classic SPI timing – slave, CPHA = 0**

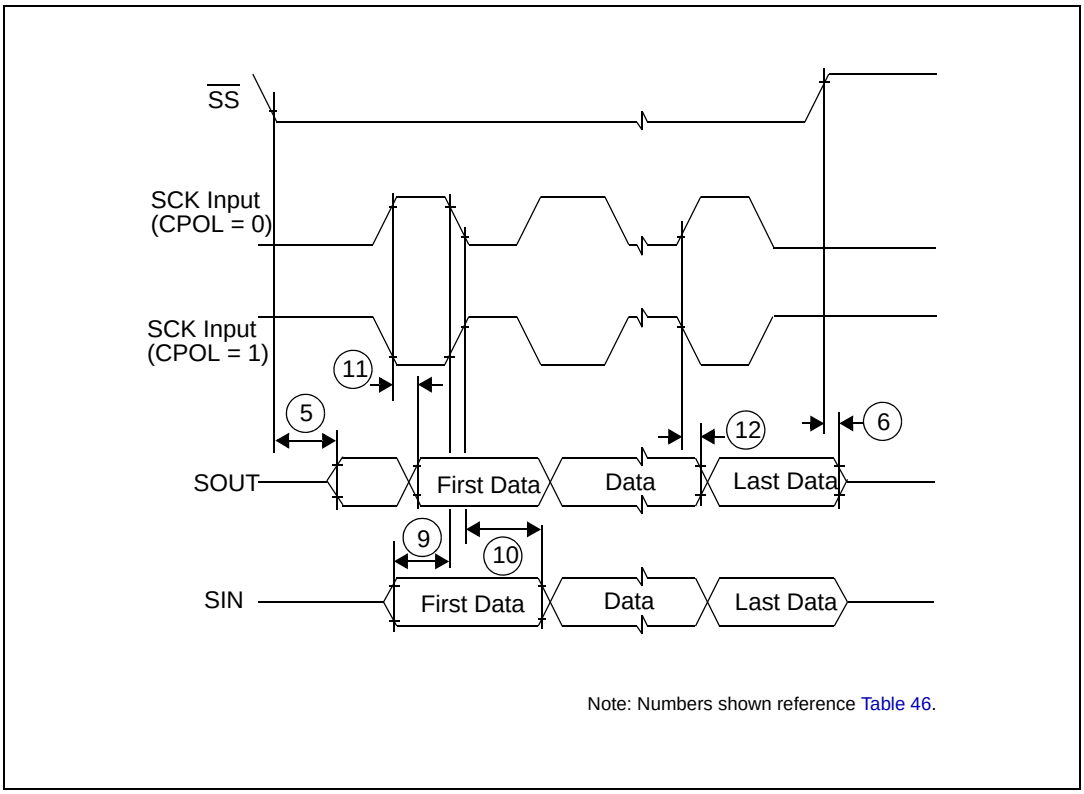


**Figure 27. DSPI classic SPI timing – slave, CPHA = 1**



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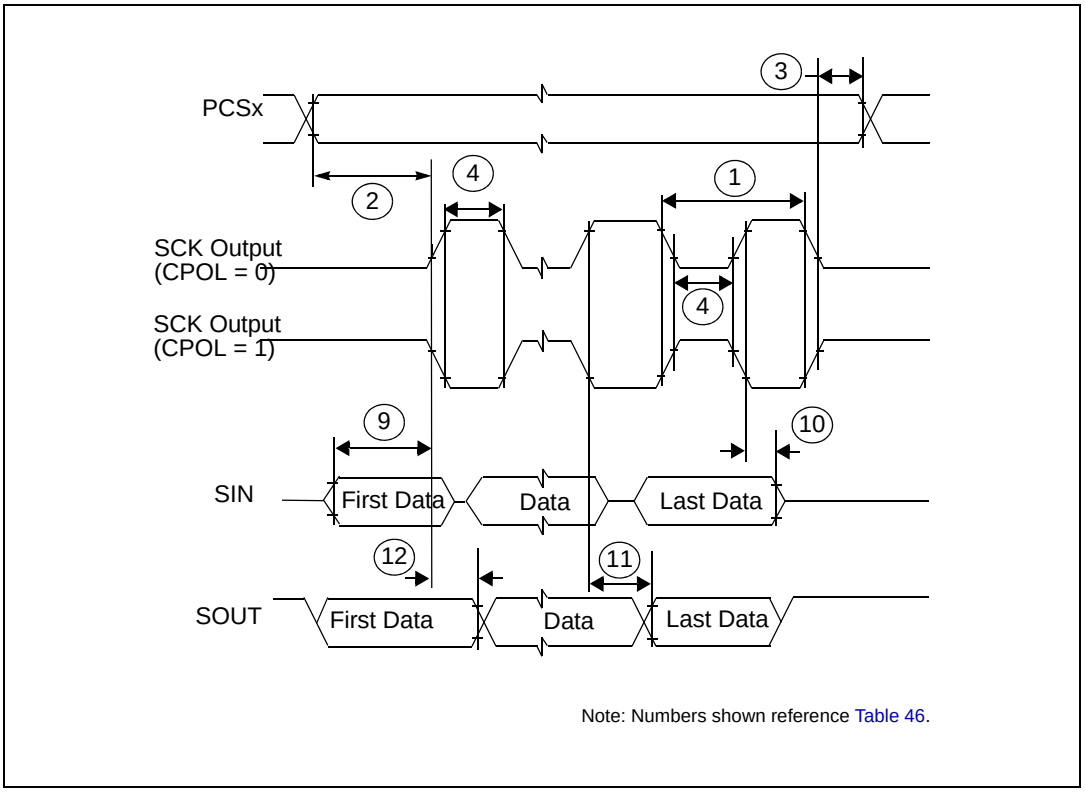


**Figure 28. DSPI modified transfer format timing – master, CPHA = 0**

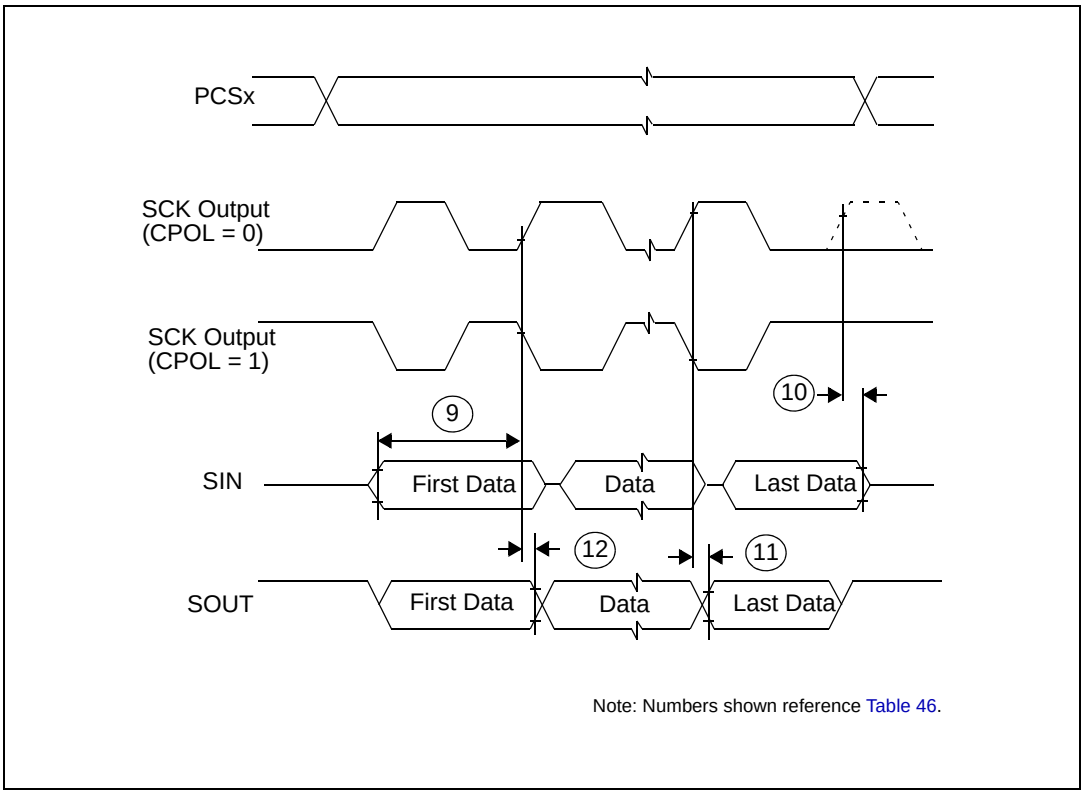


**Figure 29. DSPI modified transfer format timing – master, CPHA = 1**



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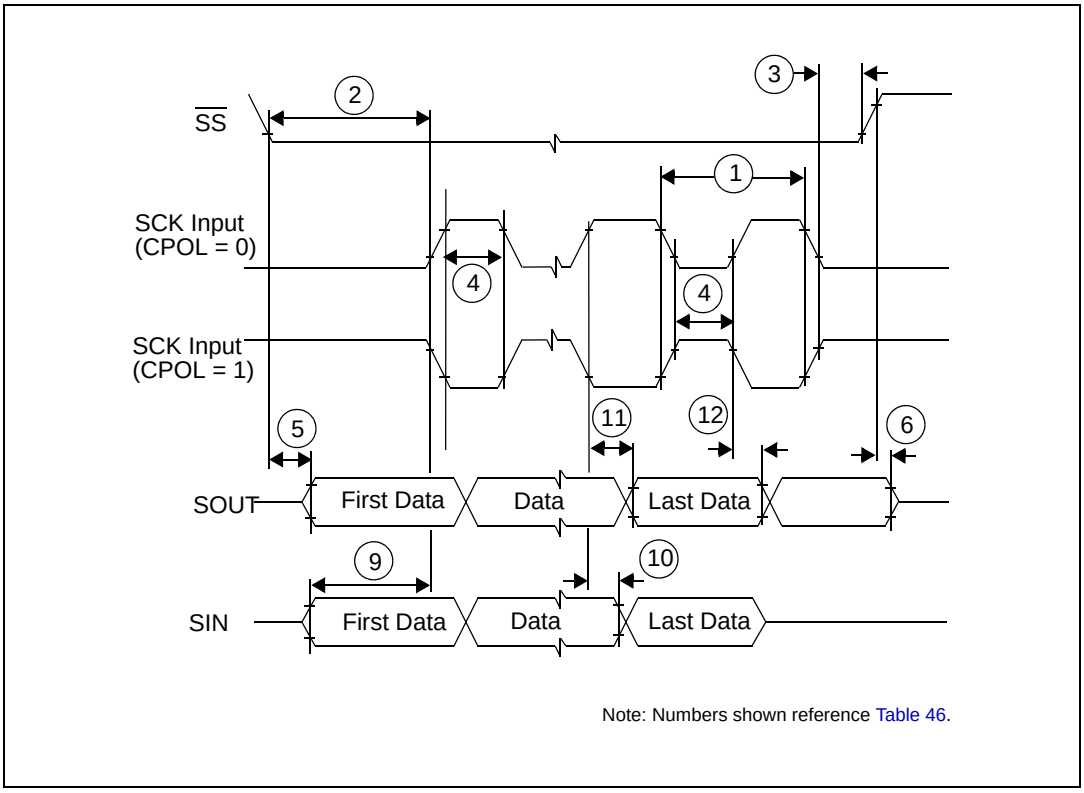


**Figure 30. DSPI modified transfer format timing – slave, CPHA = 0**

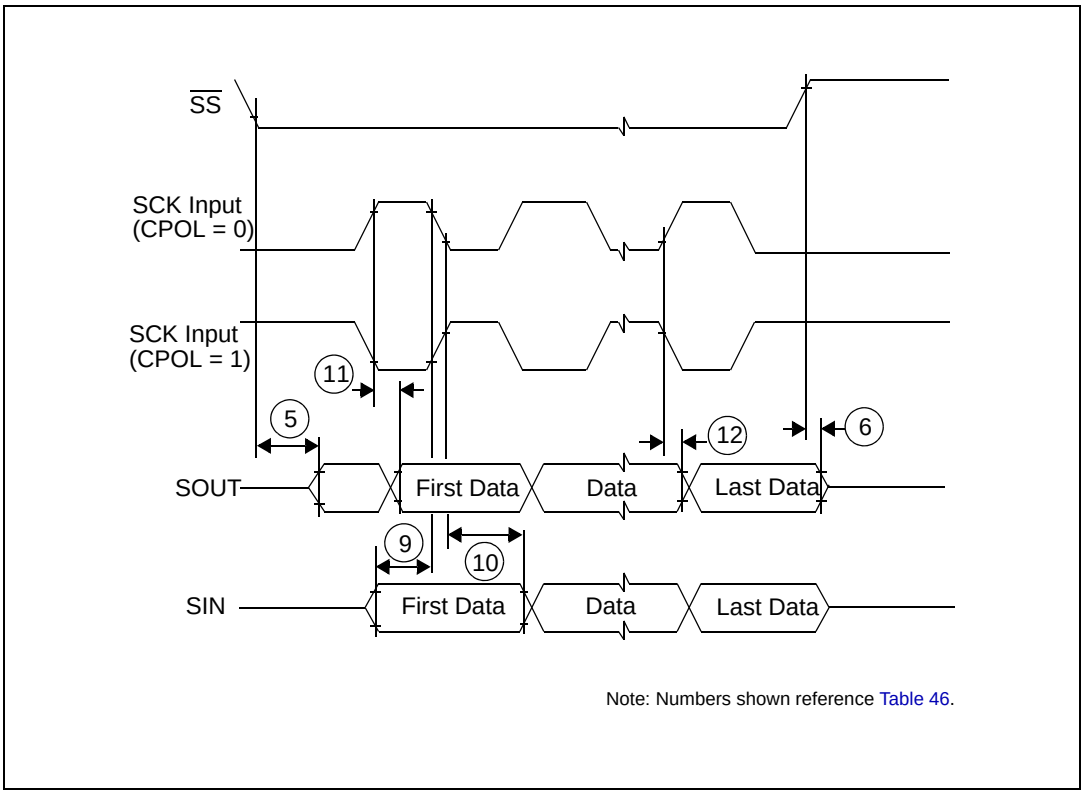


**Figure 31. DSPI modified transfer format timing – slave, CPHA = 1**



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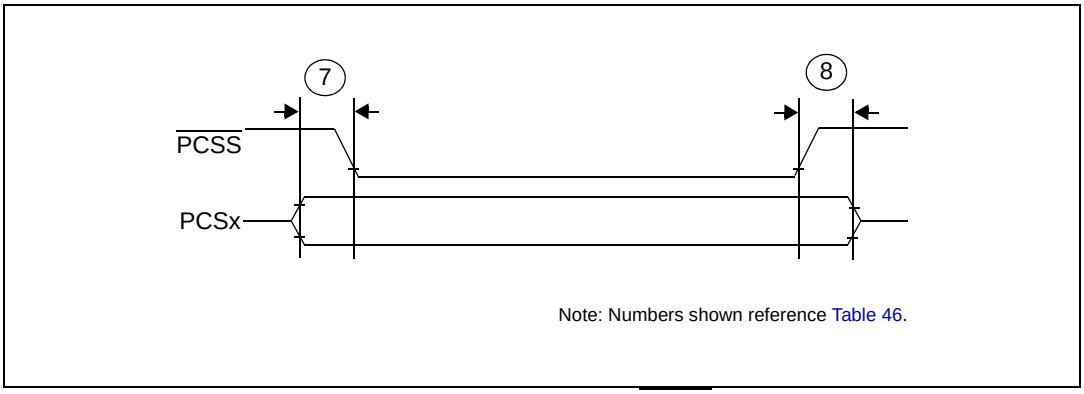


**Figure 32. DSPI PCS strobe (PCSS) timing**

## 2.27.3 Nexus characteristics

**Table 47. Nexus characteristics**

| No. | Symbol | | C | Parameter | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| 1 | $t_{TCYC}$ | CC | D | TCK cycle time | 64 | — | — | ns |
| 2 | $t_{MCYC}$ | CC | D | MCKO cycle time | 32 | — | — | ns |
| 3 | $t_{MDOV}$ | CC | D | MCKO low to MDO data valid | — | — | 8 | ns |
| 4 | $t_{MSEOV}$ | CC | D | MCKO low to MSEO_b data valid | — | — | 8 | ns |
| 5 | $t_{EVTOV}$ | CC | D | MCKO low to EVTO data valid | — | — | 8 | ns |
| 10 | $t_{NTDIS}$ | CC | D | TDI data setup time | 15 | — | — | ns |
| | $t_{NTMSS}$ | CC | D | TMS data setup time | 15 | — | — | ns |
| 11 | $t_{NTDIH}$ | CC | D | TDI data hold time | 5 | — | — | ns |
| | $t_{NTMSH}$ | CC | D | TMS data hold time | 5 | — | — | ns |
| 12 | $t_{TDOV}$ | CC | D | TCK low to TDO data valid | 35 | — | — | ns |
| 13 | $t_{TDOI}$ | CC | D | TCK low to TDO data invalid | 6 | — | — | ns |



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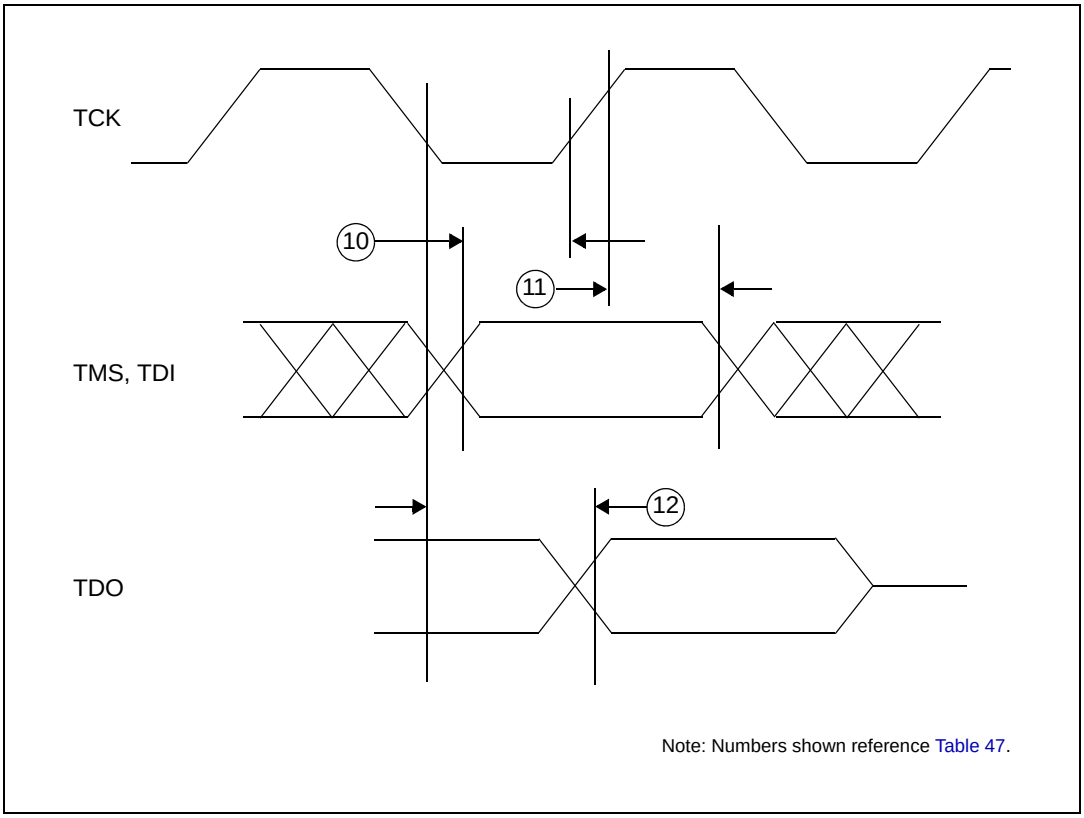


**Figure 33. Nexus TDI, TMS, TDO timing**

## 2.27.4 JTAG characteristics

**Table 48. JTAG characteristics**

| No. | Symbol | | C | Parameter | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ | Max | |
| 1 | $t_{JCYC}$ | CC | D | TCK cycle time | 64 | — | — | ns |
| 2 | $t_{TDIS}$ | CC | D | TDI setup time | 15 | — | — | ns |
| 3 | $t_{TDIH}$ | CC | D | TDI hold time | 5 | — | — | ns |
| 4 | $t_{TMSS}$ | CC | D | TMS setup time | 15 | — | — | ns |
| 5 | $t_{TMSH}$ | CC | D | TMS hold time | 5 | — | — | ns |
| 6 | $t_{TDOV}$ | CC | D | TCK low to TDO valid | — | — | 33 | ns |
| 7 | $t_{TDOI}$ | CC | D | TCK low to TDO invalid | 6 | — | — | ns |



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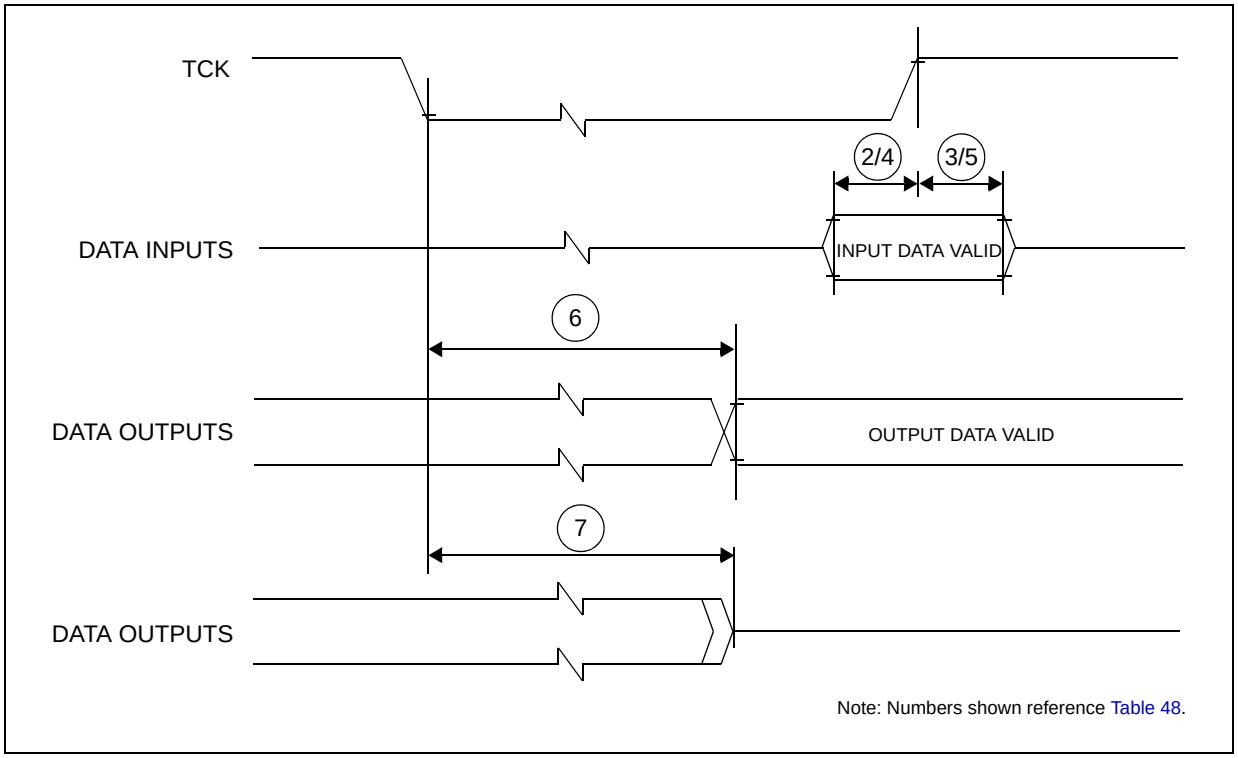


**Figure 34. Timing diagram – JTAG boundary scan**

# 3 Package characteristics

## 3.1 Package mechanical data



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### 3.1.1 64 LQFP

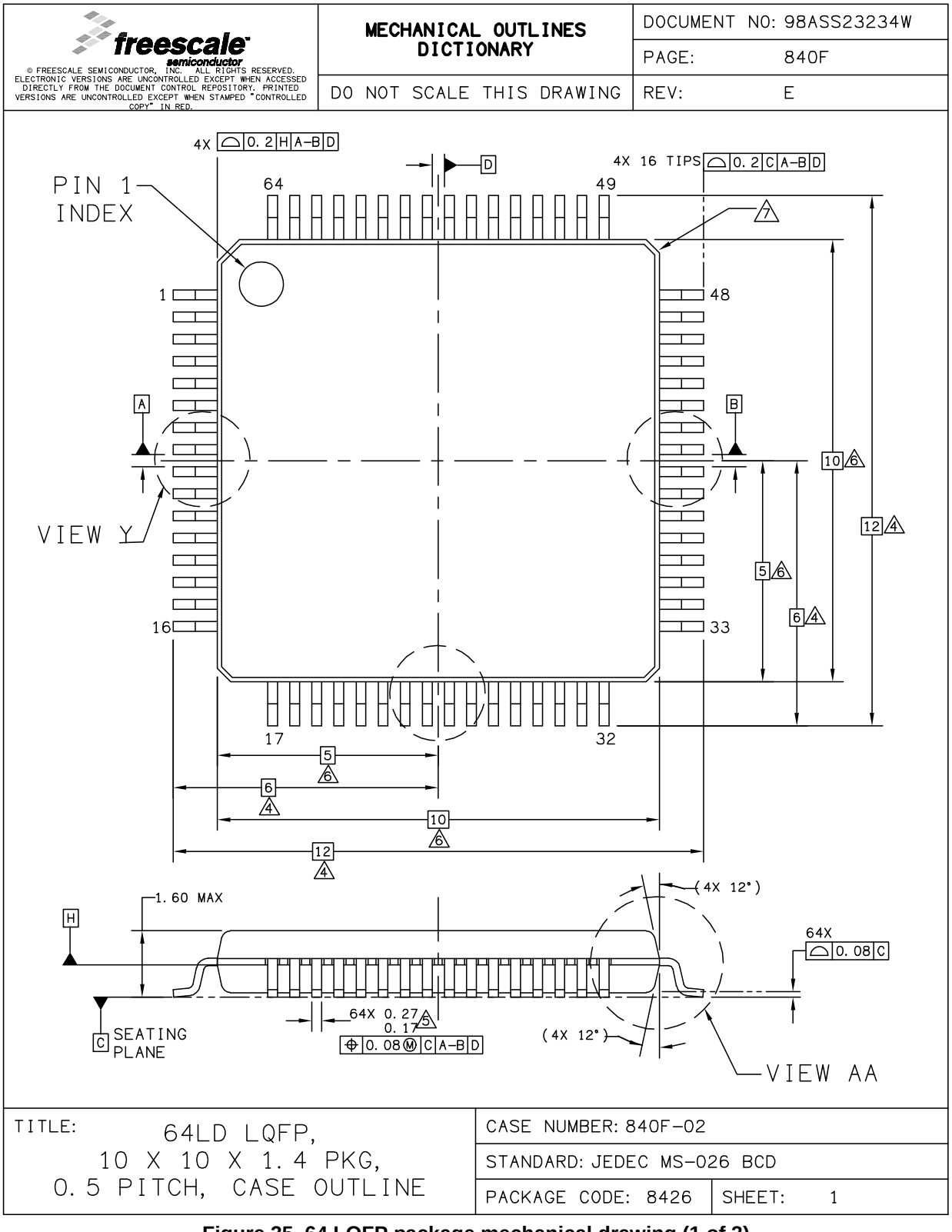


**Figure 35. 64 LQFP package mechanical drawing (1 of 3)**



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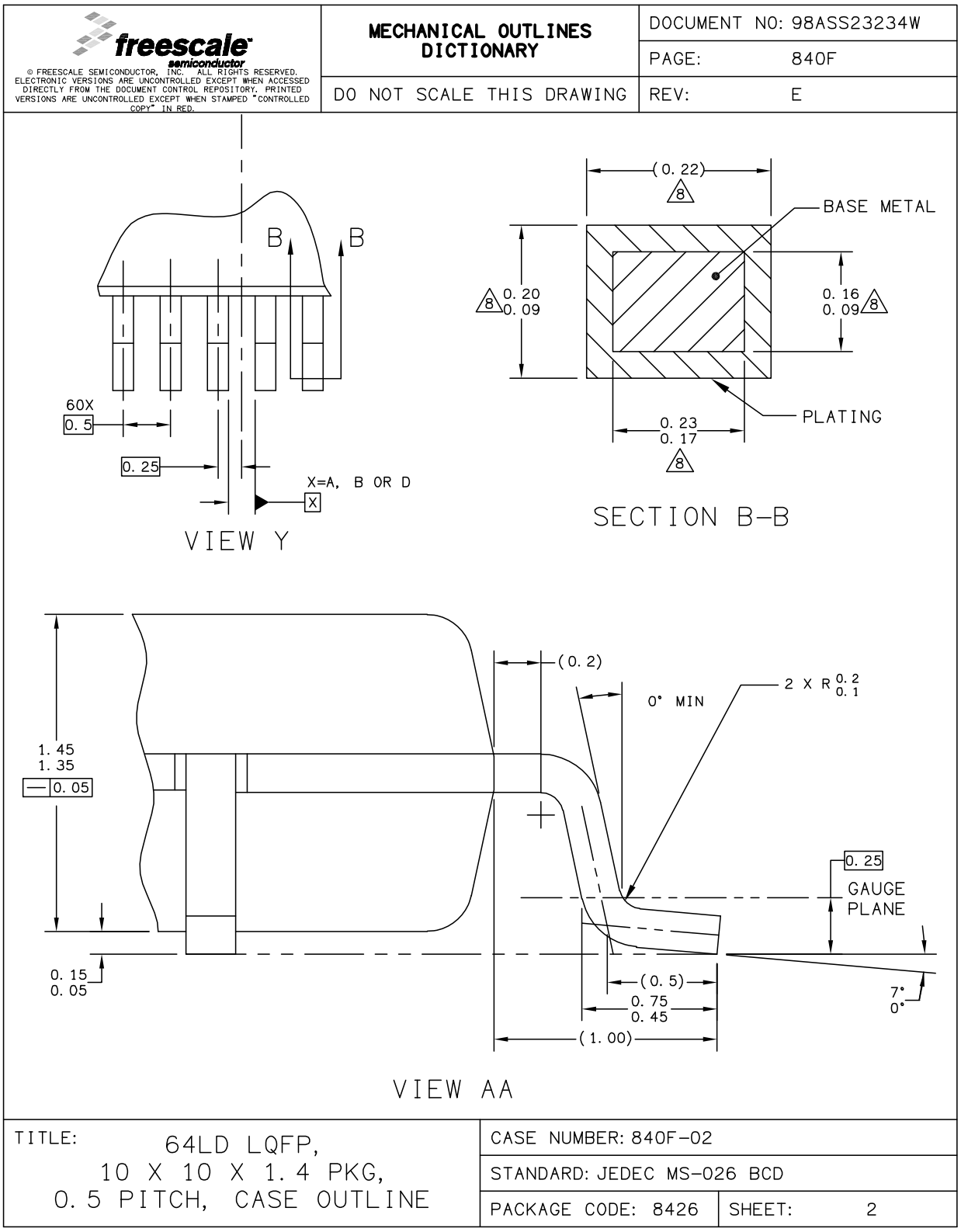


**Figure 36. 64 LQFP package mechanical drawing (2 of 3)**



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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

| TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE | CASE NUMBER: 840F–02 | |
|---|---|---|
| | STANDARD: JEDEC MS–026 BCD | |
| | PACKAGE CODE: 8426 | SHEET: 3 |

**Figure 37. 64 LQFP package mechanical drawing (3 of 3)**



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## 3.1.2 100 LQFP

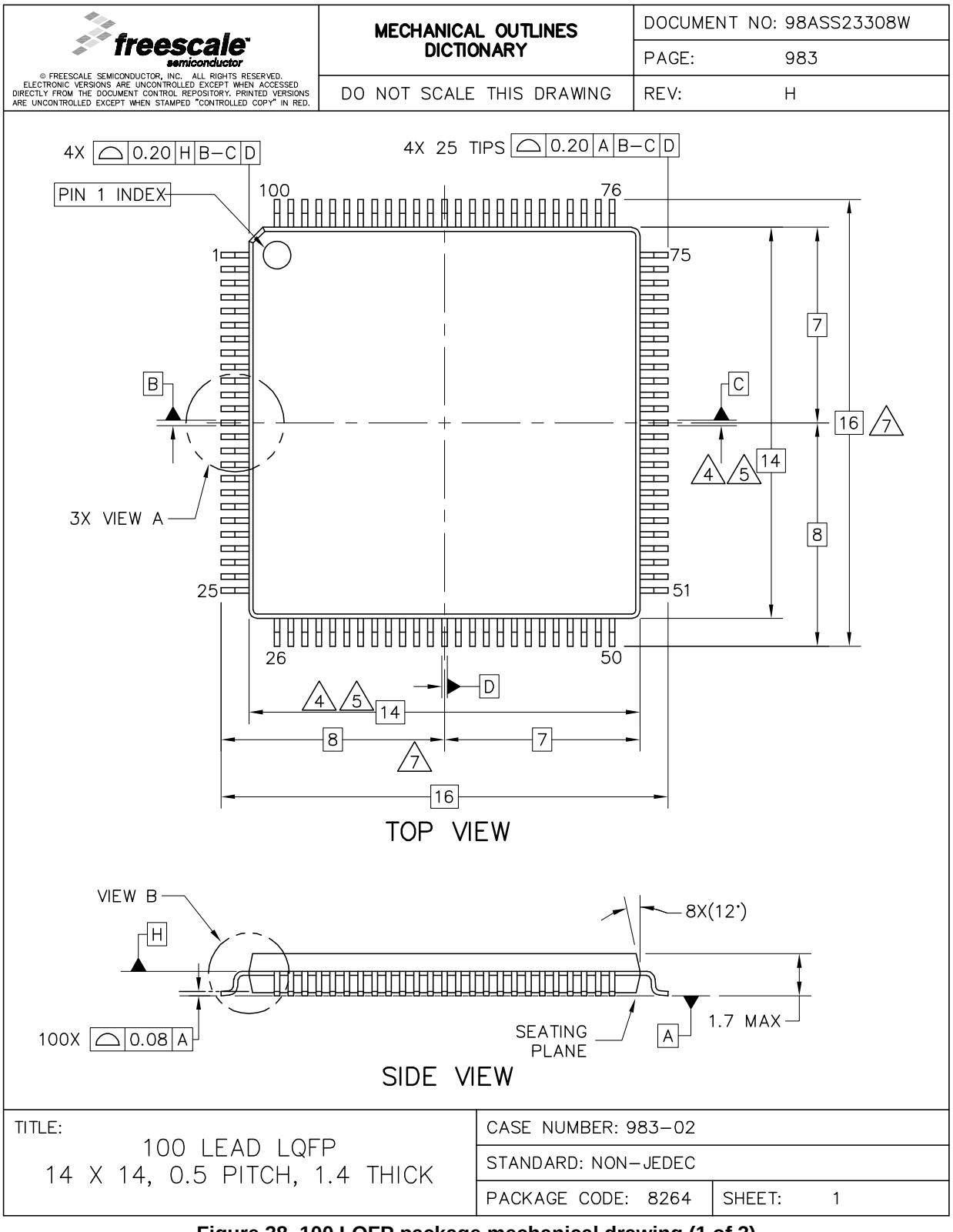


**Figure 38. 100 LQFP package mechanical drawing (1 of 3)**



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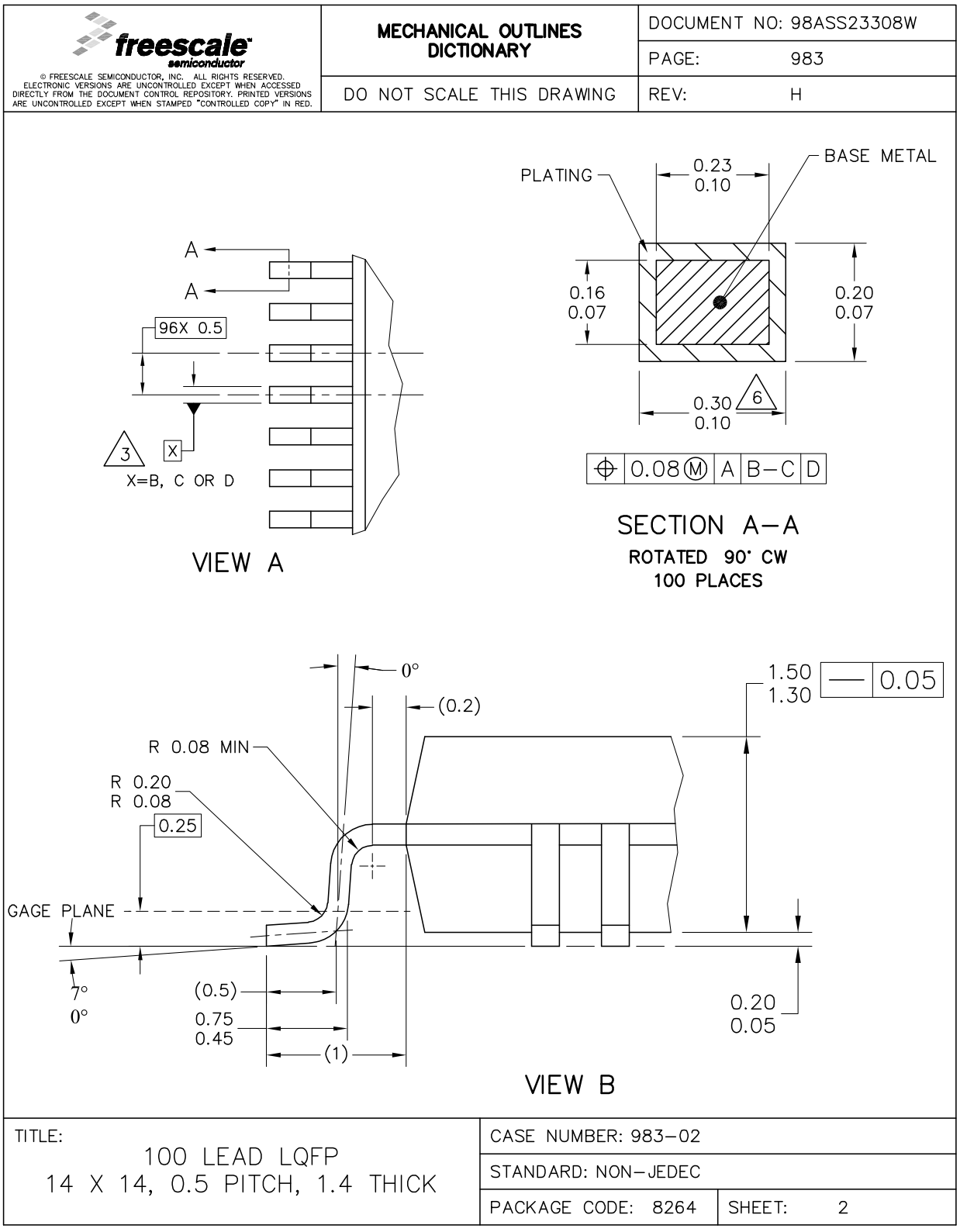


**Figure 39. 100 LQFP package mechanical drawing (2 of 3)**



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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.

5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

| | | |
|---|---|---|
| TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK | CASE NUMBER: 983–02 | |
| | STANDARD: NON–JEDEC | |
| | PACKAGE CODE: 8264 | SHEET: 3 |

**Figure 40. 100 LQFP package mechanical drawing (3 of 3)**



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### 3.1.3 144 LQFP

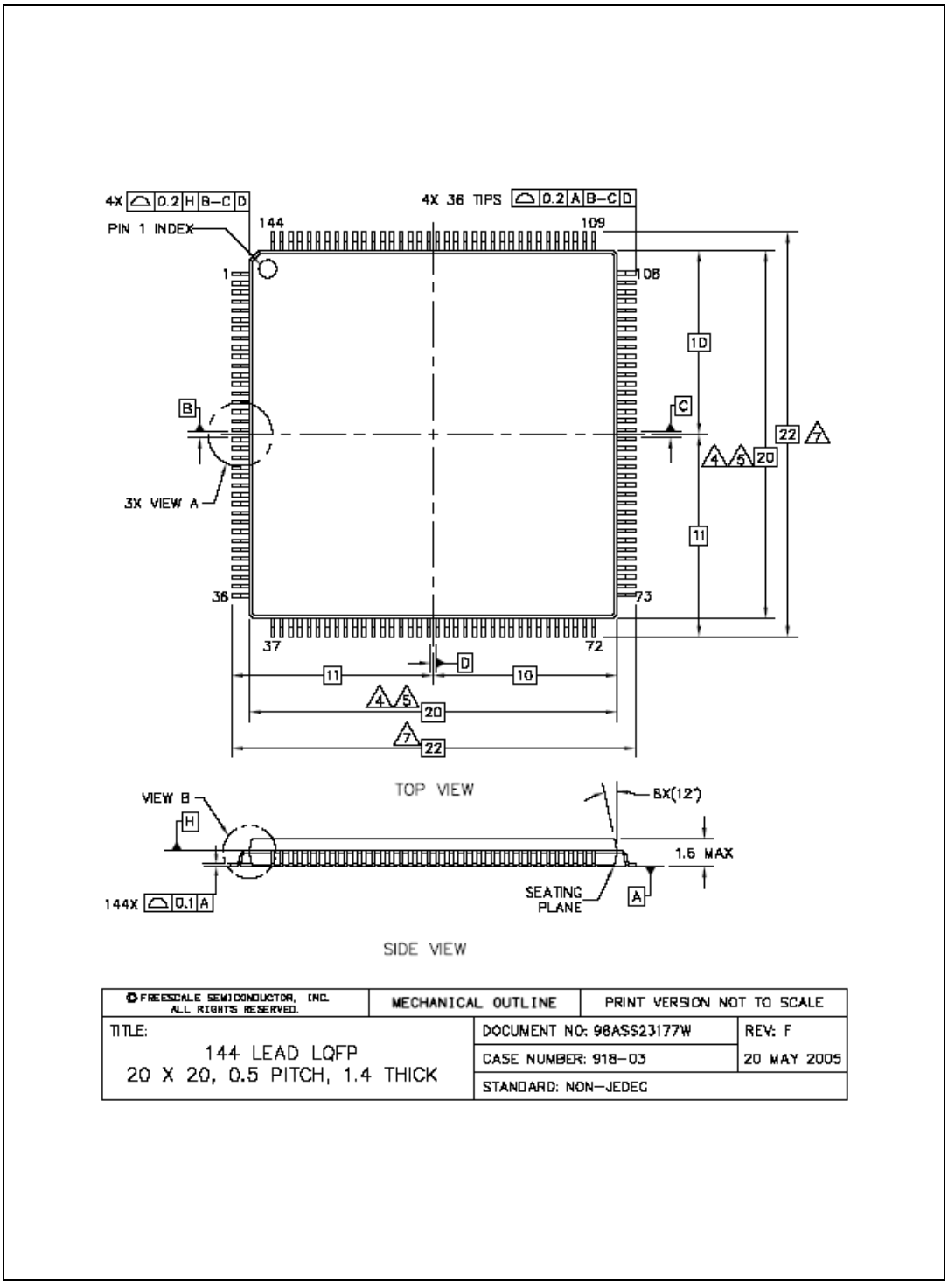


**Figure 41. 144 LQFP package mechanical drawing (1 of 2)**



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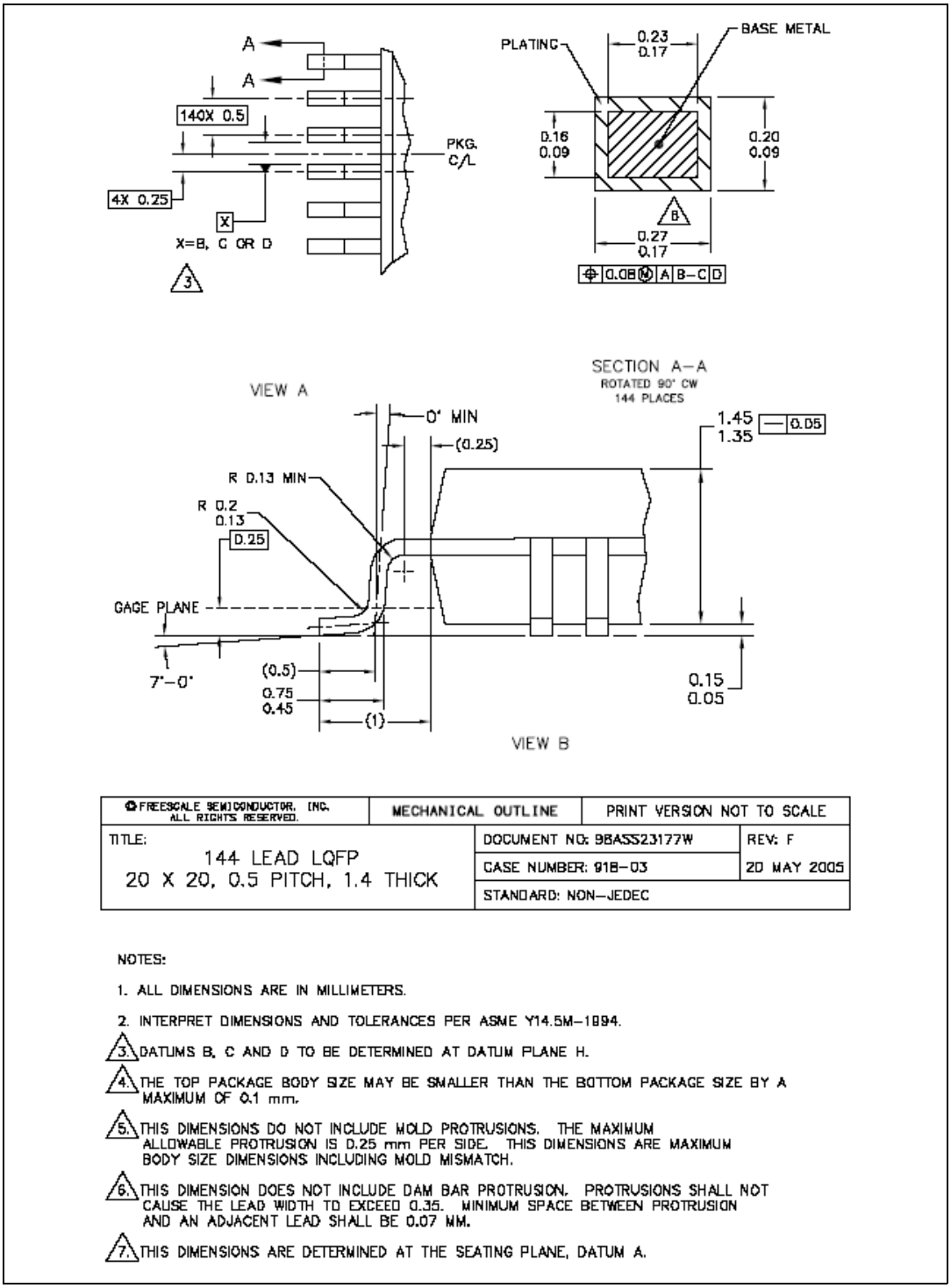


**Figure 42. 144 LQFP package mechanical drawing (2 of 2)**



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## 3.1.4 208 MAPBGA

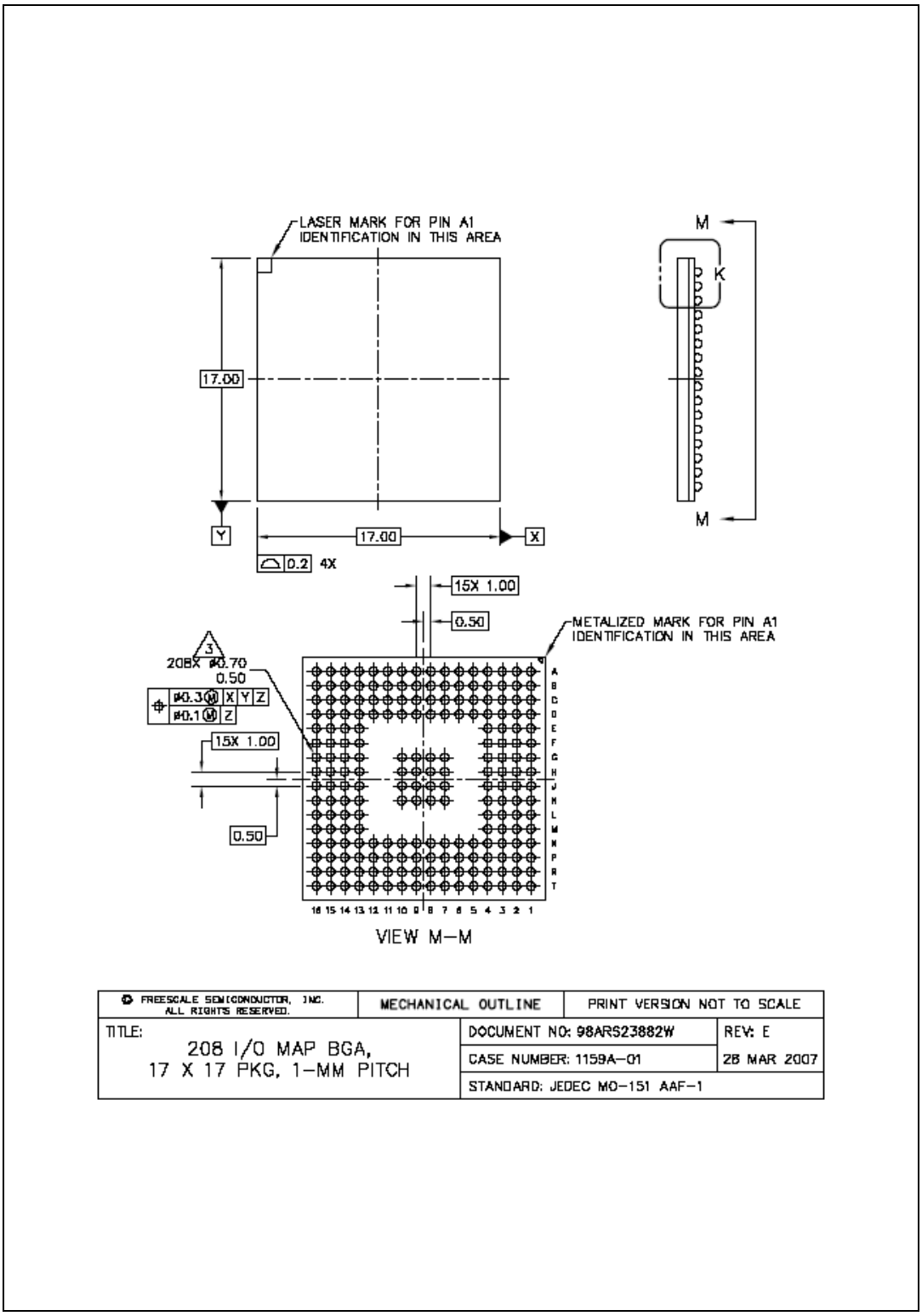


**Figure 43. 208 MAPBGA package mechanical drawing (1 of 2)**



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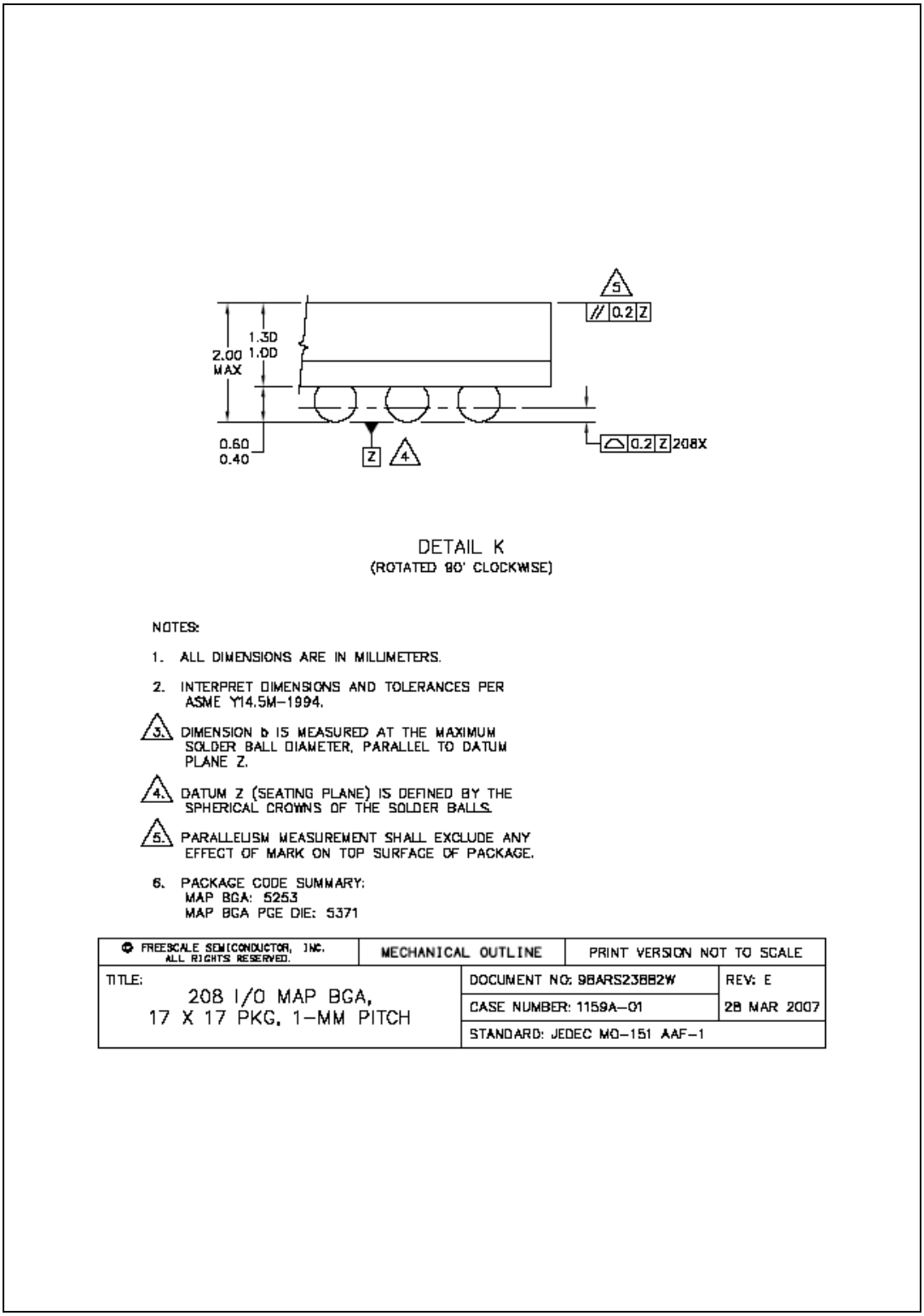


**Figure 44. 208 MAPBGA package mechanical drawing (2 of 2)**



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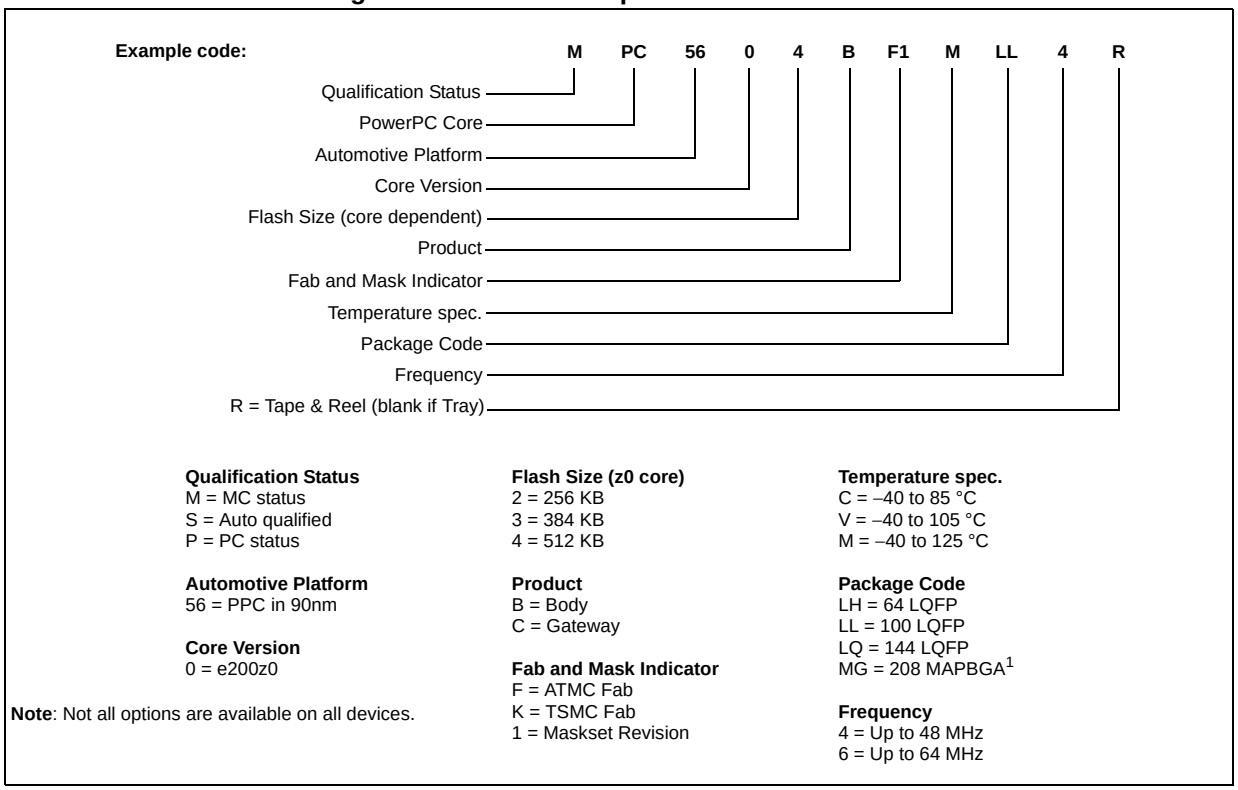
# 4 Ordering information

**Figure 45. Commercial product code structure**




1 208 MAPBGA available only as development package for Nexus2+

# 5 Document revision history

Table 49 summarizes revisions to this document.

**Table 49. Revision history**

| Revision | Date | Description of Changes |
|---|---|---|
| 1 | 04-Apr-2008 | Initial release. |



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**Table 49. Revision history (continued)**

| Revision | Date | Description of Changes |
|---|---|---|
| 2 | 06-Mar-2009 | Made minor editing and formatting changes to improve readability<br>Harmonized oscillator naming throughout document<br>Features:<br>—Replaced 32 KB with 48 KB as max SRAM size<br>—Updated description of INTC<br>—Changed max number of GPIO pins from 121 to 123<br>Updated Section 1.2, Description<br>Updated Table 3<br>Added Section , Block diagram<br>Section 2, Package pinouts and signal descriptions: Removed signal descriptions (these are found in the device reference manual)<br>Updated Figure 5:<br>—Replaced VPP with VSS_HV on pin 18<br>—Added MA[1] as AF3 for PC[10] (pin 28)<br>—Added MA[0] as AF2 for PC[3] (pin 116)<br>—Changed description for pin 120 to PH[10] / GPIO[122] / TMS<br>—Changed description for pin 127 to PH[9] / GPIO[121] / TCK<br>—Replaced NMI[0] with NMI on pin 11<br>Updated Figure 4:<br>—Replaced VPP with VSS_HV on pin 14<br>—Added MA[1] as AF3 for PC[10] (pin 22)<br>—Added MA[0] as AF2 for PC[3] (pin 77)<br>—Changed description for pin 81 to PH[10] / GPIO[122] / TMS<br>—Changed description for pin 88 to PH[9] / GPIO[121] / TCK<br>—Removed E1UC[19] from pin 76<br>—Replaced [11] with WKUP[11] for PB[3] (pin 1)<br>—Replaced NMI[0] with NMI on pin 7<br>Updated Figure 6:<br>—Changed description for ball B8 from TCK to PH[9]<br>—Changed description for ball B9 from TMS to PH[10]<br>—Updated descriptions for balls R9 and T9<br>Added Section 2.10, Parameter classification and tagged parameters in tables where appropriate<br>Added Section 2.11, NVUSRO register<br>Updated Table 11<br>Section 2.13, Recommended operating conditions: Added note on RAM data retention to end of section<br>Updated Table 12 and Table 13<br>Added Section 2.14.1, Package thermal characteristics<br>Updated Section 2.14.2, Power considerations<br>Updated Figure 7 |



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**Table 49. Revision history (continued)**

| Revision | Date | Description of Changes |
|---|---|---|
| 2 (cont.) | 06-Mar-2009 | Updated Table 15, Table 16, Table 17, Table 18 and Table 19<br>Added Section 2.15.4, Output pin transition times<br>Updated Table 22<br>Updated Figure 8<br>Updated Table 24<br>Section 2.17.1, Voltage regulator electrical characteristics: Amended description of LV_PLL<br>Figure 10: Exchanged position of symbols $C_{DEC1}$ and $C_{DEC2}$<br>Updated Table 25<br>Added Figure 13<br>Updated Table 26 and Table 27<br>Updated Section 2.19, Flash memory electrical characteristics<br>Added Section 2.20, Electromagnetic compatibility (EMC) characteristics<br>Updated Section 2.21, Fast external crystal oscillator (4 to 16 MHz) electrical characteristics<br>Updated Section 2.22, Slow external crystal oscillator (32 kHz) electrical characteristics<br>Updated Table 40, Table 41 and Table 42<br>Added Section 2.27, On-chip peripherals<br>Added Table 43<br>Updated Table 44<br>Updated Table 47<br>Added Section Appendix A, Abbreviations |



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**Table 49. Revision history (continued)**

| Revision | Date | Description of Changes |
|---|---|---|
| 4 | 06-Aug-2009 | Updated Figure 6<br>Table 11<br>• $V_{DD_ADC}$: changed min value for “relative to $V_{DD}$” condition<br>• $V_{IN}$: changed min value for “relative to $V_{DD}$” condition<br>• $I_{CORELV}$: added new row<br>Table 13<br>• $T_{A\ C\text{-}Grade\ Part}$, $T_{J\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{J\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$, $T_{J\ M\text{-}Grade\ Part}$: added new rows<br>• Changed capacitance value in footnote<br>Table 20<br>• MEDIUM configuration: added condition for PAD3V5V = 0<br>Updated Figure 10<br>Table 25<br>• $C_{DEC1}$: changed min value<br>• $I_{MREG:}$ changed max value<br>• $I_{DD_BV}$: added max value footnote<br>Table 26<br>• $V_{LVDHV3H}$: changed max value<br>• $V_{LVDHV3L}$: added max value<br>• $V_{LVDHV5H}$: changed max value<br>• $V_{LVDHV5L}$: added max value<br>Updated Table 27<br>Table 29<br>• Retention: deleted min value footnote for “Blocks with 100,000 P/E cycles“<br>Table 37<br>• $I_{FXOSC}$: added typ value<br>Table 39<br>• $V_{SXOSC}$: changed typ value<br>• $T_{SXOSCSU}$: added max value footnote<br>Table 40<br>• $\Delta t_{LTJIT}$: added max value<br>Updated Figure 38 |



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**Table 49. Revision history (continued)**

| Revision | Date | Description of Changes |
|---|---|---|
| 5 | 02-Nov-2009 | In the “MPC5604B/C series block summary” table, added a new row.<br>In the “Absolute maximum ratings” table, changed max value of $V_{DD_BV}$, $V_{DD_ADC}$, and $V_{IN}$.<br>In the “Recommended operating conditions (3.3 V)” table, deleted min value of $TV_{DD}$.<br>In the “Reset electrical characteristics” table, changed footnotes 3 and 5.<br>In the “Voltage regulator electrical characteristics” table:<br>• $C_{REGn}$: changed max value.<br>• $C_{DEC1}$: split into 2 rows.<br>• Updated voltage values in footnote 4<br>In the “Low voltage monitor electrical characteristics” table:<br>• Updated column Conditions.<br>• $V_{LVDLVCORL}$, $V_{LVDLVBKPL}$: changed min/max value.<br>In the “Program and erase specifications” table, added initial max value of $T_{dwprogram}$.<br>In the “Flash module life” table, changed min value for blocks with 100K P/E cycles<br>In the “Flash power supply DC electrical characteristics” table:<br>• $I_{FREAD}$, $I_{FMOD}$: added typ value.<br>• Added footnote 1.<br>Added *“NVUSRO[WATCHDOG_EN] field description” section.*<br>*Section 4.18: “ADC electrical characteristics”* has been moved up in hierarchy (it was Section 4.18.5).<br>In the “ADC conversion characteristics” table, changed initial max value of $R_{AD}$.<br>In the “On-chip peripherals current consumption” table:<br>• Removed min/max from the heading.<br>• Changed unit of measurement and consequently rounded the values. |



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**Table 49. Revision history (continued)**

| Revision | Date | Description of Changes |
|---|---|---|
| 6 | 15-Mar-2010 | In the “Introduction” section, relocated a note.<br>In the “MPC5604B/C device comparison” table, added footnote regarding SCI and CAN.<br>In the “Absolute maximum ratings” table, removed the min value of $V_{IN}$ relative to $V_{DD}$.<br>In the “Recommended operating conditions (3.3 V)” table:<br>• $T_{A\ C\text{-}Grade\ Part}$, $T_{J\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{J\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$, $T_{J\ M\text{-}Grade\ Part}$: added new rows.<br>• $TV_{DD}$: made single row.<br>In the “LQFP thermal characteristics” table, added more rows.<br>Removed “208 MAPBGA thermal characteristics” table.<br>In the “I/O consumption” table:<br>• Removed $I_{DYNSEG}$ row.<br>• Added “I/O weight” table.<br>In the “Voltage regulator electrical characteristics” table:<br>• Updated the values.<br>• Removed $I_{VREGREF}$ and $I_{VREDLVD12}$.<br>• Added a note about $I_{DD_BC}$.<br>In the “Low voltage monitor electrical characteristics” table:<br>• Updated $V_{PORH}$ values.<br>• Updated $V_{LVDLVCORL}$ value.<br>Entirely updated the “Low voltage power domain electrical characteristics” table.<br>In the “Program and erase specifications” table, inserted $T_{eslat}$ row.<br>Entirely updated the “Flash power supply DC electrical characteristics” table.<br>Entirely updated the “Start-up time/Switch-off time” table.<br>In the “Crystal oscillator and resonator connection scheme” figure, relocated a note.<br>In the “Slow external crystal oscillator (32 kHz) electrical characteristics” table:<br>• Removed $g_{mSXOSC}$ row.<br>• Inserted values of $I_{SXOSCBIAS}$.<br>Entirely updated the “Fast internal RC oscillator (16 MHz) electrical characteristics” table.<br>In the “ADC conversion characteristics” table: updated the description of the conditions of $t_{ADC_PU}$ and $t_{ADC_S}$.<br>Entirely updated the “DSPI characteristics” table.<br>In the “Orderable part number summary” table, modified some orderable part number.<br>Updated the “Commercial product code structure” figure.<br>Removed the note about the condition from “Flash read access timing” table<br>Removed the notes that assert the values need to be confirmed before validation<br>Exchanged the order of “LQFP 100-pin configuration” and “LQFP 144-pin configuration”<br>Exchanged the order of “LQFP 100-pin package mechanical drawing” and “LQFP 144-pin package mechanical drawing” |



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**Table 49. Revision history (continued)**

| Revision | Date | Description of Changes |
|---|---|---|
| 7 | 05-Jul-2010 | Added 64 LQFP package information<br>Updated the “Features” section.<br>Figures “LQFP 100-pin configuration” and “LQFP 100-pin configuration”: removed alternate function information<br>Added “Functional port pin descriptions” table<br>Added eDMA block in the “MPC5604B/C series block diagram” figure<br>Deleted the “NVUSRO[WATCHDOG_EN] field description” section<br>In the “Recommended operating conditions (3.3 V)” and “Recommended operating conditions (5.0 V)” tables, deleted the conditions of $T_{A\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$<br>In the “LQFP thermal characteristics” table, rounded the values.<br>In the “RESET electrical characteristics” section, replaced “nRSTIN” with “RESET”.<br>In the “I/O input DC electrical characteristics” table:<br>• $W_{FI}$: inserted a footnote<br>• $W_{NFI}$: inserted a footnote<br>In the “Low voltage monitor electrical characteristics” table:<br>• changed min value $V_{LVDHV3L}$, from 2.7 to 2.6<br>• Inserted max value of $V_{LVDLVCORL}$<br>In the “FMPLL electrical characteristics” table, rounded the values of $f_{VCO}$.<br>In the “DSPI characteristics” table:<br>• Added $\Delta t_{ASC}$ row<br>• Update values of $t_A$<br>In the “ADC conversion characteristics” table, added “$I_{ADCPWD}$” and “$I_{ADCRUN}$” rows<br>Removed “Orderable part number summary” table. |
| 8 | 25-Nov-2010 | Editorial changes and improvements.<br>In the “MPC5604B/C device comparison” table, changed the temperature value from 105 to 125 °C, in the footnote regarding “Execution speed”.<br>In the “Recommended operating conditions (3.3 V)” and “Recommended operating conditions (5.0 V)” tables, restored the conditions of $T_{A\ C\text{-}Grade\ Part}$, $T_{A\ V\text{-}Grade\ Part}$, $T_{A\ M\text{-}Grade\ Part}$<br>In the “LQFP thermal characteristics” table, added values concerning 64 LQFP package.<br>In the “MEDIUM configuration output buffer electrical characteristics” table: fixed a typo in last row of conditions column, there was $I_{OH}$ that now is $I_{OL}$.<br>In the “Reset electrical characteristics” table, changed the parameter classification tag for $V_{OL}$ and $\lvert I_{WPU}\rvert$.<br>In the “Low voltage monitor electrical characteristics” table, changed the max value of $V_{LVDLVCORL}$ from 1.5V to 1.15V.<br>In the “Program and erase specifications” table, replaced “$T_{eslat}$” with “$T_{esus}$”.<br>In the “FMPLL electrical characteristics” table, changed the parameter classification tag for $f_{VCO}$. |



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**Table 49. Revision history (continued)**

| Revision | Date | Description of Changes |
|---|---|---|
| 9 | 16 June 2011 | Formatting and minor editorial changes throughout<br>Harmonized oscillator nomenclature<br>Removed all instances of note “All 64 LQFP information is indicative and must be confirmed during silicon validation.”<br><br>Device comparison table: changed temperature value in footnote 2 from 105 °C to 125 °C<br>MPC560xB LQFP 64-pin configuration and MPC560xC LQFP 64-pin configuration: renamed pin 6 from VPP_TEST to VSS_HV<br>Removed “Pin Muxing” section; added sections “Pad configuration during reset phases”, “Voltage supply pins”, “Pad types”, “System pins,” “Functional ports”, and “Nexus 2+ pins”<br>Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN]<br>Added section “NVUSRO[WATCHDOG_EN] field description”<br>Recommended operating conditions (3.3 V) and Recommended operating conditions (5.0 V): updated conditions for ambient and junction temperature characteristics<br>I/O input DC electrical characteristics: updated $I_{LKG}$ characteristics<br>Section “I/O pad current specification”: removed content referencing the $I_{DYNSEG}$ maximum value<br>I/O consumption: replaced instances of “Root medium square” with “Root mean square”<br>I/O weight: replaced instances of bit “SRE” with “SRC”; added pads PH[9] and PH[10]; added supply segments; removed weight values in 64-pin LQFP for pads that do not exist in that package<br>Reset electrical characteristics: updated parameter classification for $\|I_{WPU}\|$<br>Updated Voltage regulator electrical characteristics<br>Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$; replaced “LVD_DIGBKP” with “LVDLVBKP” in note<br>Updated section “Power consumption”<br>Fast external crystal oscillator (4 to 16 MHz) electrical characteristics: updated parameter classification for $V_{FXOSCOP}$<br>Crystal oscillator and resonator connection scheme: added footnote about possibility of adding a series resistor<br>Slow external crystal oscillator (32 kHz) electrical characteristics: updated footnote 1<br>FMPLL electrical characteristics: added short term jitter characteristics; inserted “—” in empty min value cell of $t_{lock}$ row<br>Section “Input impedance and ADC accuracy”: changed “$V_A/V_{A2}$” to “$V_{A2}/V_A$” in Equation 11<br>ADC input leakage current: updated $I_{LKG}$ characteristics<br>ADC conversion characteristics: updated symbols<br>On-chip peripherals current consumption: changed “supply current on “$V_{DD_HV_ADC}$” to “supply current on” $V_{DD_HV}$” in $I_{DD_HV(FLASH)}$ row; updated $I_{DD_HV(PLL)}$ value—was 3 * $f_{periph}$, is 30 * $f_{periph}$; updated footnotes<br>DSPI characteristics: added rows $t_{PCSC}$ and $t_{PASC}$<br>Added DSPI PCS strobe (PCSS) timing diagram |



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**Table 49. Revision history (continued)**

| Revision | Date | Description of Changes |
|---|---|---|
| 10 | 15 Oct 2012 | Table 2 (Bolero 512K device comparison), added footnote for MPC5603BxLH and MPC5604BxLH about FlexCAN availability.<br>Table 2 (MPC5604B/C series block summary), replaced “System watchdog timer” with “Software watchdog timer” and specified AUTOSAR (Automotive Open System Architecture)<br>Table 5 (Functional port pin descriptions):<br>replaced footnote “Available only on MPC560xC versions and MPC5604B 208 MAPBGA devices” with “Available only on MPC560xC versions, MPC5603B 64 LQFP, MPC5604B 64 LQFP and MPC5604B 208 MAPBGA devices”,<br>replaced VDD with VDD_HV<br>Figure 10 (Voltage regulator capacitance connection), updated pin name appearance<br>Renamed Figure 11 ($V_{DD_HV}$ and $V_{DD_BV}$ maximum slope) (was “VDD and VDD_BV maximum slope”)<br>Renamed Figure 12 ($V_{DD_HV}$ and $V_{DD_BV}$ supply constraints during STANDBY mode exit) (was “VDD and VDD_BV supply constraints during STANDBY mode exit”)<br>Table 12 (Recommended operating conditions (3.3 V)), added minimum value of $T_{VDD}$ and footnote about it.<br>Table 13 (Recommended operating conditions (5.0 V)), added minimum value of $T_{VDD}$ and footnote about it.<br>Section 2.17.1, “Voltage regulator electrical characteristics:<br>replaced “slew rate of $V_{DD}/V_{DD_BV}$” with “slew rate of both $V_{DD_HV}$ and $V_{DD_BV}$”<br>replaced “When STANDBY mode is used, further constraints apply to the $V_{DD}/V_{DD_BV}$ in order to guarantee correct regulator functionality during STANDBY exit.” with “When STANDBY mode is used, further constraints are applied to the both $V_{DD_HV}$ and $V_{DD_BV}$ in order to guarantee correct regulator function during STANDBY exit.”<br>Table 27 (Power consumption on VDD_BV and VDD_HV), updated footnotes of $I_{DDMAX}$ and $I_{DDRUN}$ stating that both currents are drawn only from the $V_{DD_BV}$ pin.<br>Table 31 (Flash memory power supply DC electrical characteristics), in the parameter column replaced $V_{DD_BV}$ and $V_{DD_HV}$ respectively with VDD_BV and VDD_HV.<br>Table 45 (On-chip peripherals current consumption), in the parameter column replaced $V_{DD_BV}$, $V_{DD_HV}$ and $V_{DD_HV_ADC}$ respectively with VDD_BV, VDD_HV and VDD_HV_ADC<br>Updated Section 2.26.2, “Input impedance and ADC accuracy<br>Table 46 (DSPI characteristics), modified symbol for $t_{PCSC}$ and $t_{PASC}$ |
| 11 | 14 Nov 2012 | In the cover feature list:<br>added “and ECC” at the end of “Up to 512 KB on-chip code flash supported with the flash controller”<br>added “with ECC” at the end of “Up to 48 KB on-chip SRAM”<br>Table 12 (Recommended operating conditions (3.3 V)), removed minimum value of $T_{VDD}$ and relative footnote.<br>Table 13 (Recommended operating conditions (5.0 V)), removed minimum value of $T_{VDD}$ and relative footnote. |
| 12 | 19 Mar 2014 | Added “K=TSMC Fab” against the Fab and mask indicator in Figure 45 (Commercial product code structure). |



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**Table 49. Revision history (continued)**

| Revision | Date | Description of Changes |
|---|---|---|
| 13 | 19 Jan 2015 | In Table 1 (MPC5604B/C device comparison):<br>• changed the MPC5604BxLH entry for CAN (FlexCAN) from $3^7$ to $2^6$.<br>• updated tablenote 7.<br>In Table 13 (Recommended operating conditions (5.0 V)), updated tablenote 5 to: “1 µF (electrolithic/tantalum) + 47 nF (ceramic) capacitance needs to be provided between $V_{DD_ADC}/V_{SS_ADC}$ pair. Another ceramic cap of 10nF with low inductance package can be added”.<br>In Section 2.17.2, “Low voltage detector electrical characteristics, added a note on LVHVD5 detector.<br>In Section 4, “Ordering information, added a note: “Not all options are available on all devices”. |



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# Appendix A Abbreviations

Table A-1 lists abbreviations used but not defined elsewhere in this document.

**Table A-1. Abbreviations**

| Abbreviation | Meaning |
|---|---|
| CMOS | Complementary metal–oxide–semiconductor |
| CPHA | Clock phase |
| CPOL | Clock polarity |
| CS | Peripheral chip select |
| EVTO | Event out |
| MCKO | Message clock out |
| MDO | Message data out |
| MSEO | Message start/end out |
| MTFE | Modified timing format enable |
| SCK | Serial communications clock |
| SOUT | Serial data out |
| TBD | To be defined |
| TCK | Test clock input |
| TDI | Test data input |
| TDO | Test data output |
| TMS | Test mode select |



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