Revision History

Document No.	Release Date	Change Description
A	7/19/04	Original Sipex Data Sheet.
1.0.0	11/6/08	Generate new Data Sheet using Exar format and change revision to 1.0.0. Remove IEC Air and Contact ESD ratings. Update ordering information to remove EOL part numbers.Update charge pump description to show regulated charge pump design.
1.0.1	6/3/11	Remove SP310ECP-L and SP310EEP-L per PDN 110510-01
1.0.2	3/28/19	Update to MaxLinear format. Update ordering information. Moved ESD ratings to under Absolute Maximum Ratings. Removed obsolete SP310E and SP312E.

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Specifications

Absolute Maximum Ratings

Important: This is a stress rating only and functional operation of the device at these ratings or any other above those indicated in the operation section of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect reliability.

Table 2: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Supply voltage (V_{CC})		6.0	V
V+	V_{CC} - 0.3	11.0	V
V-	-11.0		V
Input Voltages			
T_{IN}	-0.3	V_{CC} +0.3	V
R_{IN}	-15	15	V
Output Voltages			
T_{OUT}	V+, 0.3V	V-, -0.3V	V
R_{OUT}	-0.3	V_{CC} + 0.3	V
Short Circuit Duration			
T_{OUT}		Continuous	
Package Power Dissipation			
Small outline (derate 7mW/°C above 70°C)		375	mW
Storage temperature	-65	150	°C

ESD Ratings

Table 3: ESD Ratings

Parameter	Limit	Units
HBM (Human Body Model)	±15	kV

Electrical Characteristics

V_{CC} = 5V ± 10%, 0.1µF charge pump capacitors, T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are V_{CC} = 5V and T_A = 25°C

Table 4: **Electrical Characteristics**

Parameter	Test Condition	Minimum	Typical	Maximum	Units
TTL Input					
Logic threshold LOW	T_{IN}, $\overline{EN}$, $\overline{SD}$, ON/$\overline{OFF}$			0.8	V
Logic threshold HIGH	T_{IN}, $\overline{EN}$, $\overline{SD}$, ON/$\overline{OFF}$	2.0			V
Logic pull-up current	T_{IN} = 0V		15	200	µA
TTL Output					
Output voltage LOW	I_{OUT} = 3.2mA, V_{CC} = 5V			0.4	V
Output voltage HIGH	I_{OUT} = -1.0mA	3.5			V
RS-232 Output					
Output voltage swing	All transmitter outputs loaded with 3kΩ to GND	±5.0	±6.0		V
Output resistance	V_{CC} = 0V, V_{OUT} = ±2V	300			Ω
Output short circuit current	Infinite duration		±18		mA
Maximum data rate	C_L = 2500pF, R_L = 3kΩ	120	240		kbps
RS-232 Input					
Voltage range		-15		15	V
Voltage threshold LOW	V_{CC} = 5V, T_A = 25°C	0.8	1.2		V
Voltage threshold HIGH	V_{CC} = 5V, T_A = 25°C		1.7	2.8	V
Hysteresis	V_{CC} = 5V, T_A = 25°C	0.2	0.5	1.0	V
Resistance	T_A = 25°C, -15V ≤ V_{IN} ≤ 15V	3	5	7	kΩ
Dynamic Characteristics					
Driver propagation delay	TTL to RS-232; C_L = 50pF		1.5	3.0	µs
Receiver propagation delay	RS-232 to TTL		0.1	1.0	µs
Instantaneous slew rate	C_L = 10pF, R_L = 3-7kΩ, T_A = 25°C			30	V/µs
Transition region slew rate	C_L = 2500pF, R_L = 3kΩ, measured from 3V to -3V or -3V to 3V		10		V/µs
Power Requirements					
V_{CC} power supply current	No load, V_{CC} = 5V, T_A = 25°C		3	5	mA
V_{CC} power supply current, loaded	All transmitters R_L = 3kΩ, T_A = 25°C		15		mA

Performance Curves
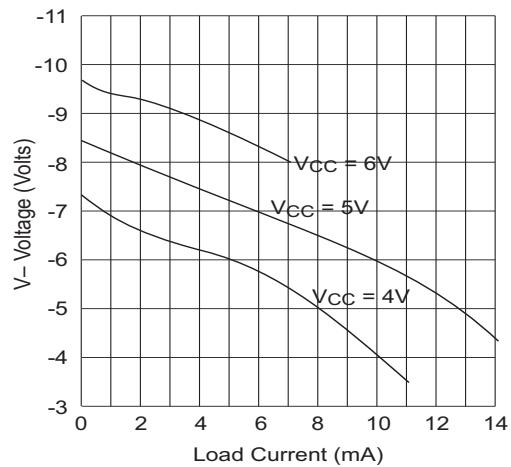
Figure 1: V- Voltage
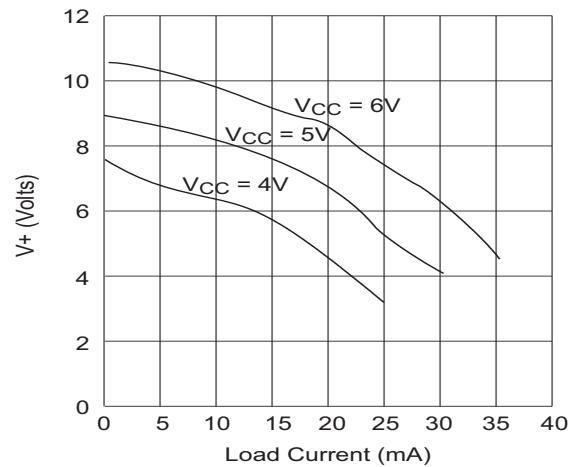
Figure 2: V+ Voltage
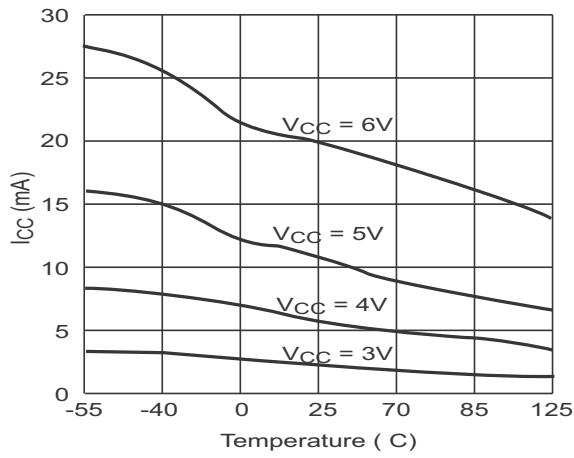
Figure 3: I$_{CC}$ vs. Temperature
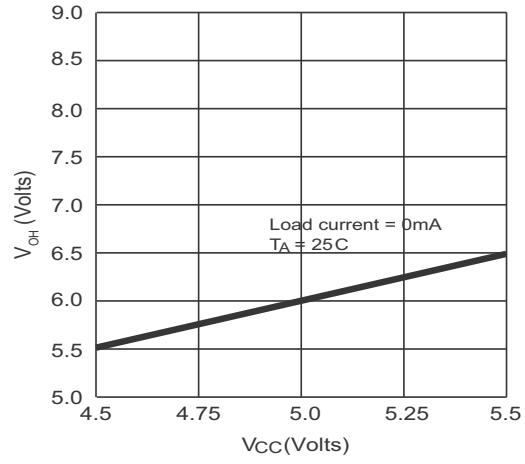
Figure 4: V$_{OH}$ vs. V$_{CC}$

Pin Information

Pin Configurations

```
       C1+  ┌1      16┐ VCC
        V+  ┌2      15┐ GND
        C1- ┌3      14┐ T1OUT
        C2+ ┌4  SP  13┐ R1IN
        C2- ┌5  202 12┐ R1OUT
         V- ┌6  E   11┐ T1IN
      T2OUT ┌7      10┐ T2IN
       R2IN ┌8       9┐ R2OUT
```
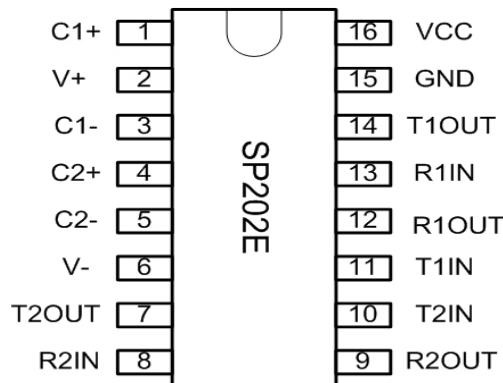
Figure 5: SP202E Pin Configuration

```
       C1+  ┌1      16┐ VCC
        V+  ┌2      15┐ GND
        C1- ┌3      14┐ T1OUT
        C2+ ┌4  SP  13┐ R1IN
        C2- ┌5  232 12┐ R1OUT
         V- ┌6  E   11┐ T1IN
      T2OUT ┌7      10┐ T2IN
       R2IN ┌8       9┐ R2OUT
```
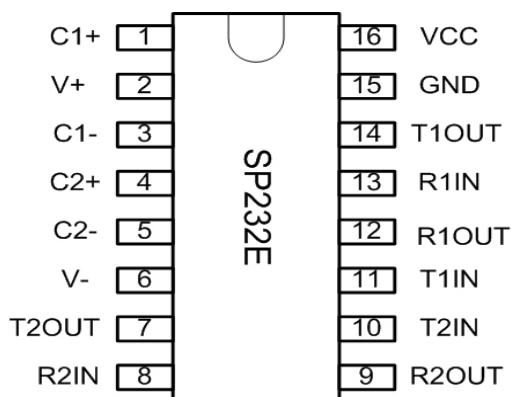
Figure 6: SP232E Pin Configuration

```
       T2IN  ┌1      20┐ R2OUT
       T1IN  ┌2      19┐ R2IN
      R1OUT  ┌3      18┐ T2OUT
       R1IN  ┌4      17┐ V-
      T1OUT  ┌5  SP  16┐ C2-
        GND  ┌6  233 15┐ C2+
        Vcc  ┌7  E   14┐ C1-
         V+  ┌8      13┐ C1+
        GND  ┌9      12┐ C2+
         V-  ┌10     11┐ C2-
```
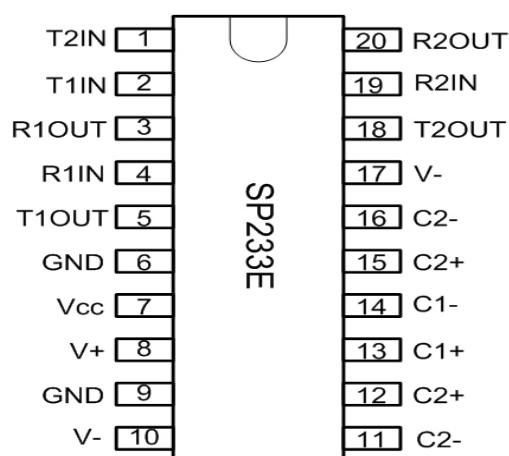
Figure 7: SP233E Pin Configuration

Description

The SP202E, SP232E and SP233E devices are a family of line driver and receiver pairs that meet the EIA / TIA-232 and V-28 serial communications protocols. The ESD tolerance has been improved on these devices to over ±15kV for Human Body Model. These devices are pin-to-pin compatible with MaxLinear's SP232A and SP233A as well as popular industry standards.This family of parts offer a 120kbps data rate, 10V/us slew rate and an on-board charge pump that operates from a single 5V supply using 0.1µF ceramic capacitors.

The SP202E, SP232E and SP233E devices have internal charge pump voltage converters which allow them to operate from a single +5V supply. The charge pumps will operate with polarized or non-polarized capacitors ranging from 0.1 to 10µF and will generate the ±6V needed to generate the RS-232 output levels.

The SP233E design offers internal charge pump capacitors.

Theory Of Operation

The SP202E, SP232E and SP233E devices are made up of three basic circuit blocks: 1. Drivers, 2. Receivers, and 3. charge pump. Each block is described below.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to EIA / TIA-232 levels with an inverted sense relative to the input logic levels. The typical driver output voltage swing is ±6V. Even under worst case loading conditions of 3kΩ and 2500pF, the driver output is guaranteed to be ±5.0V minimum, thus satisfying the RS-232 specification. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability.

The slew rate of the driver output is internally limited to 30V/µs in order to meet the EIA standards (EIA-232F). Additionally, the driver outputs LOW to HIGH transition meets the monotonic output requirements of the standard.

Receivers

The receivers convert EIA / TIA-232 signal levels to inverted TTL or CMOS logic output levels. Since the input is usually from a transmission line, where long cable length

and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines. The input thresholds are 0.8V minimum and 2.8V maximum, again well within the ±3V RS-232 requirements. Should an input be left unconnected, an internal 5kΩ pull-down resistor to ground will commit the output of the receiver to a HIGH state.

In actual system applications, it is quite possible for signals to be applied to receiver inputs before power is applied to the receiver circuitry. This occurs, for example, when a PC user attempts to print, only to realize that the printer wasn't turned on. In this case an RS-232 signal from the PC will appear on the receiver input at the printer. When the printer power is turned on, the receiver will operate normally. All of these devices are fully protected.

Charge pump

The charge pump is an Exar patented design and uses a unique approach compared to older less efficient designs. The charge pump requires 4 external capacitors and uses a four phase voltage shifting technique. The internal power supply consists of a dual charge pump that provides a driver output voltage swing of ±6V. The internal oscillator controls the four phases of the voltage shifting. A description of each phase follows:

Phase 1

V_{SS} charge store and double: The positive terminals of capacitors C1 and C2 are charged from V_{CC} with their negative terminals initially connected to ground. C1+ is then connected to ground and the stored charge from C1- is superimposed onto C2-. Since C2+ is still connected to V_{CC} the voltage potential across C2 is now 2 x V_{CC}.

Phase 2

V_{SS} transfer and invert: Phase two connects the negative terminal of C2 to the V_{SS} storage capacitor and the positive terminal of C2 to ground. This transfers the doubled and inverted (V-) voltage onto C4. Meanwhile, capacitor C1 is charged from V_{CC} to prepare it for its next phase.

Phase 3

V_{DD} charge store and double: Phase three is identical to the first phase. The positive terminals of C1 and C2 are charged from V_{CC} with their negative terminals initially connected to ground. C1+ is then connected to ground and the stored charge from C1- is superimposed onto C2-. Since C2+ is still connected to V_{CC} the voltage potential across capacitor C2 is now 2 x V_{CC}.

Phase 4

V_{DD} transfer: The fourth phase connects the negative terminal of C2 to ground and the positive terminal of C2 to

the V_{DD} storage capacitor. This transfers the doubled (V+) voltage onto C3. Meanwhile, capacitor C1 is charged from V_{CC} to prepare it for its next phase.

The clock rate for the charge pump typically operates at greater than 15kHz allowing the pump to run efficiently with small 0.1µF capacitors. Efficient operation depends on rapid charging and discharging of C1 and C2, therefore capacitors should be mounted as close as possible to the IC and have low ESR (equivalent series resistance). Inexpensive surface mount, ceramic capacitors are ideal for use on the charge pump. If polarized capacitors are used, the positive and negative terminals should be connected as shown in the typical operating circuit. A diagram of the individual phases are shown in Figure 8.
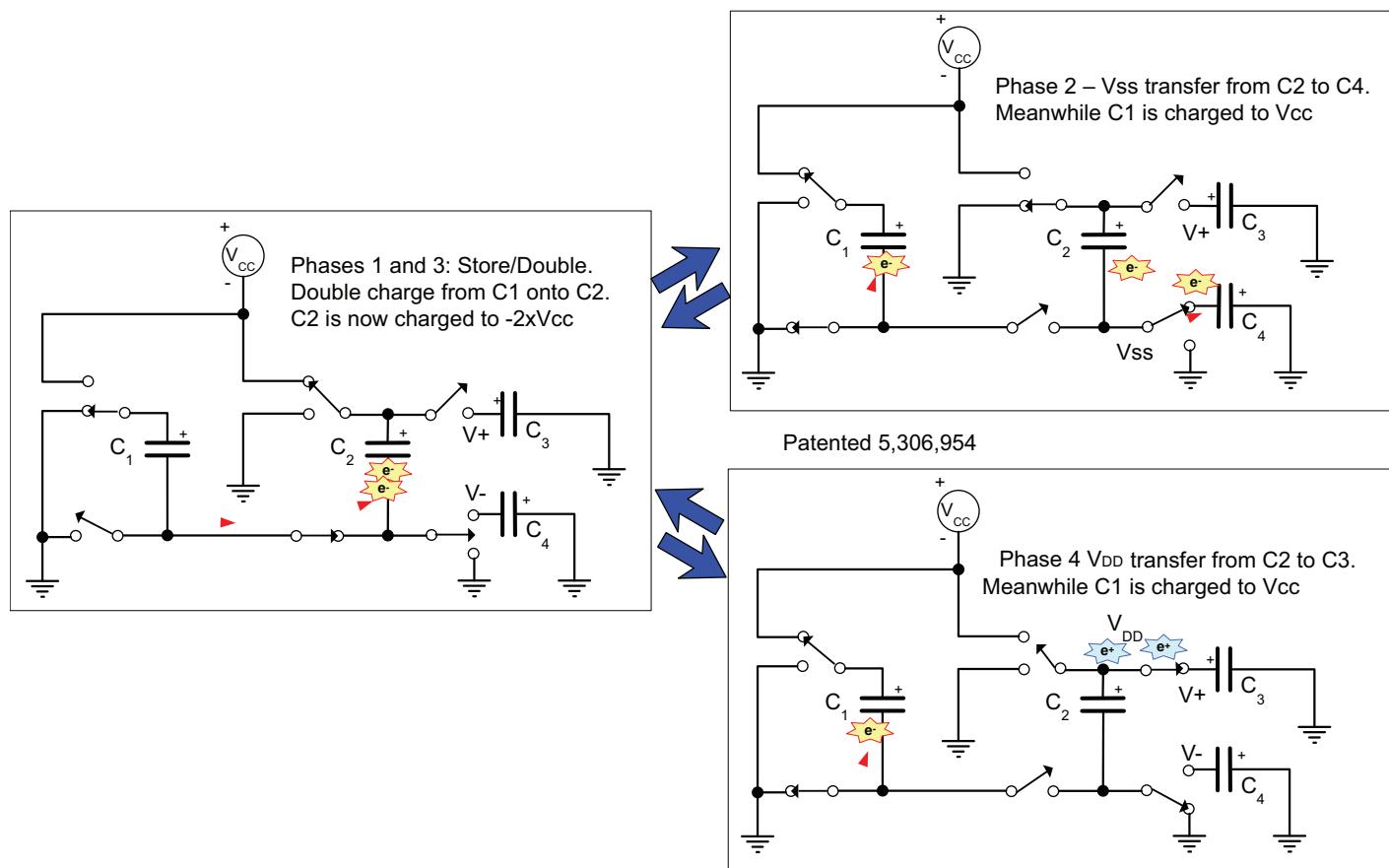
Figure 8: Charge Pump Phases

Pin Strapping for the SP233E

To operate properly, the following pairs of pins must be externally wired together as noted in Table 5:

Table 5: SP233E Pin Strapping

Pins Wired Together	SOICW
Two V- pins	10 & 17
Two C2+ pins	12 & 15
Two C- pins	11 & 16
	Connect pins 6 and 9 to GND

ESD Tolerance

The SP202E, SP232E and SP233E devices incorporate ruggedized ESD cells on all driver outputs and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV Human Body Model without damage nor latch-up.

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing.

The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 9. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the IC's tend to be handled frequently.
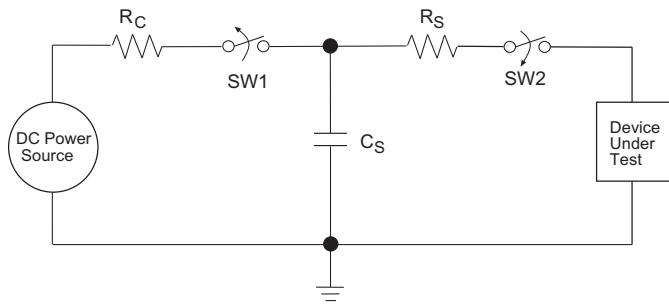
Figure 9: ESD Test Circuit for Human Body Model

Typical Performance Characteristics
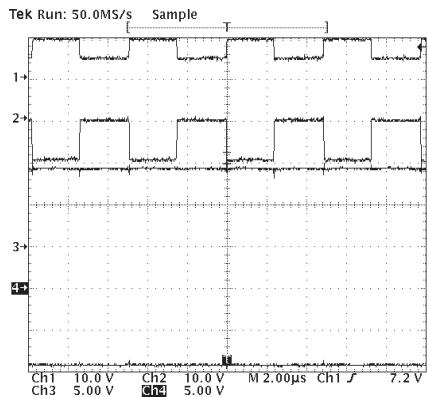
**Figure 10: SP232E Charge Pump Waveforms
No Load
(1 = C1+, 2 = C2+, 3 = V+, 4 = V-)**
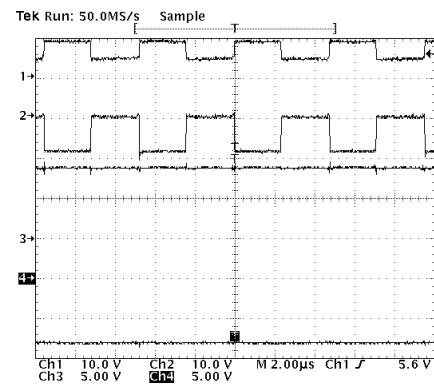
**Figure 11: SP232E Charge Pump Waveforms
When Fully Loaded with 3kΩ
(1 = C1+, 2 = C2+, 3 = V+, 4 = V-)**
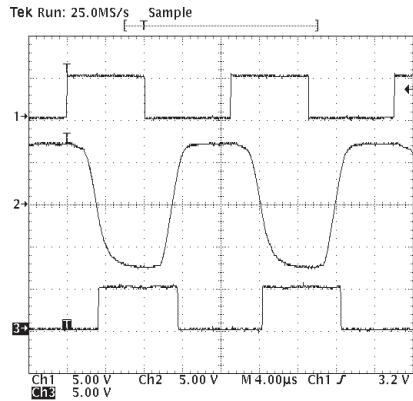
**Figure 12: Loopback Results
at 60kHz and 2500pF load
(1 = TX$_{IN}$, 2 = TX$_{OUT}$/RX$_{IN}$, 3 = RX$_{OUT}$)**
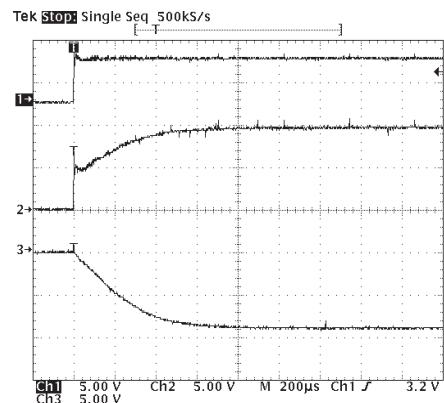
**Figure 13: Charge Pump Outputs
at Start Up
(1 = V$_{CC}$, 2 = V+, 3 = V-)**
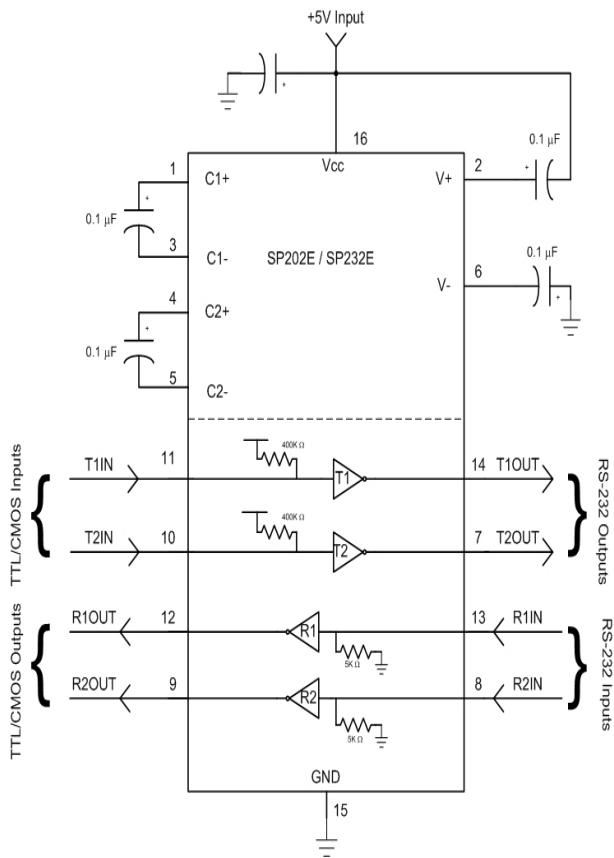
Figure 14: SP202E and SP232E Typical Application Circuit
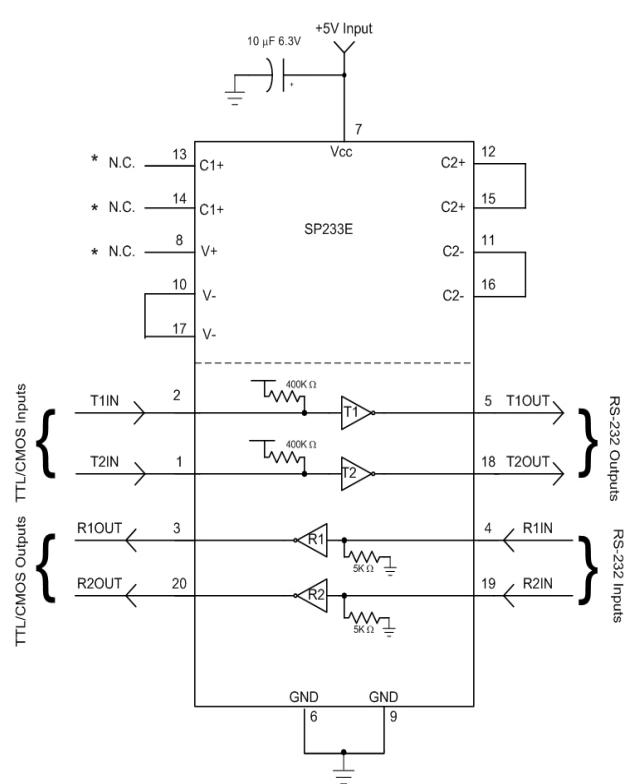
* Do not make connections to these pins

Figure 15: SP233E Typical Application Circuit

Mechanical Dimensions

NSOIC16

Top View

Side View

Front View

| SYMBOLS	COMMON DIMENSIONS IN MM (Control Unit)			COMMON DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
q	0°	—	8°	0°	—	8°
q1	5°	—	15°	5°	—	15°
q2	0°	—	—	0°	—	—
D	9.90 BSC			0.390 BSC		
N	16					

PACKAGE OUTLINE NSOIC .150" BODY
JEDEC MS–012 VARIATION AC

Drawing No: POD-00000114

Revision: A

Figure 16: Mechanical Dimension, NSOIC16

Mechanical Dimensions

WSOIC16

Top View

Side View

Front View

SYMBOLS	COMMON DIMENSIONS IN MM (Control Unit)			COMMON DIMENSIONS IN INCHES (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	—	2.65	0.093	—	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	2.05	—	2.55	0.081	—	0.100
b	0.31	—	0.51	0.012	—	0.020
c	0.20	—	0.33	0.008	—	0.013
E	10.30 BSC			0.406 BSC		
E1	7.50 BSC			0.295 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.75	0.010	—	0.030
L	0.40	—	1.27	0.016	—	0.050
L1	1.40 REF			0.055 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	10.30 BSC			0.405 BSC		
N	16					

PACKAGE OUTLINE SOIC .300" BODY
JEDEC MS-013 VARIATION AA

Drawing No: POD-00000115

Revision: B

Figure 17: **Mechanical Dimensions, WSOIC16**

Mechanical Dimensions

WSOIC20

TOP VIEW

SIDE VIEW 1

SIDE VIEW 2
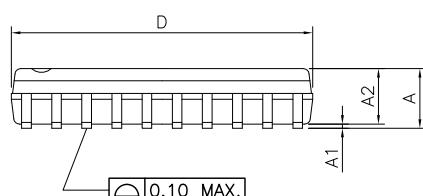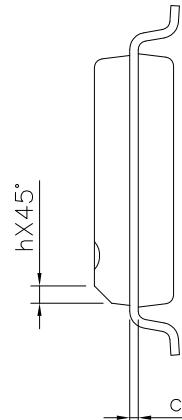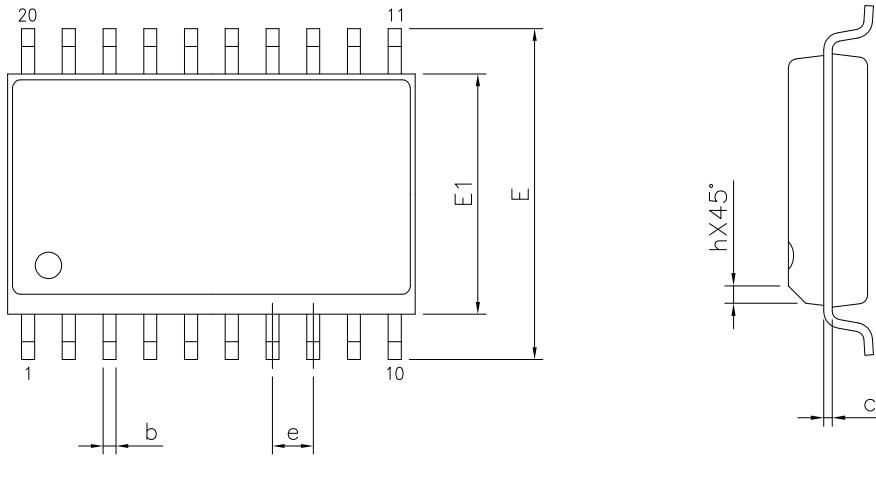
SYMBOLS	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.30
A2	2.05	2.55
b	0.31	0.51
c	0.20	0.33
D	12.80 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.40 REF	
h	0.25	0.75
$\theta°$	0	8

TERMINAL DETAILS
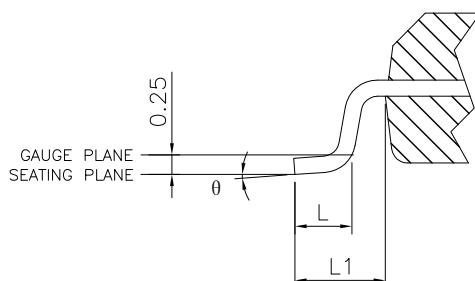
– ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

– DIMENSIONS AND TOLERANCE PER JEDEC MS-013 AC.

Drawing No.: POD-000000 146

Revision: A

Figure 18: Mechanical Dimensions, WSOIC20

Ordering Information

Table 6: Ordering Information

Ordering Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
SP202ECN-L	0°C to 70°C	Yes[2]	NSOIC16	Tube
SP202ECN-L/TR				Reel
SP202ECT-L			WSOIC16	Tube
SP202ECT-L/TR				Reel
SP202EEN-L	-40°C to 85°C		NSOIC16	Tube
SP202EEN-L/TR				Reel
SP202EET-L/TR			WSOIC16	Reel
SP232ECN-L	0°C to 70°C		NSOIC16	Tube
SP232ECN-L/TR				Reel
SP232ECT-L/TR			WSOIC16	Reel
SP232EEN-L	-40°C to 85°C		NSOIC16	Tube
SP232EEN-L/TR				Reel
SP232EET-L/TR			WSOIC16	Reel
SP233EET-L			WSOIC20	Tube

1. Refer to www.maxlinear.com/SP202E, www.maxlinear.com/SP232E, and www.maxlinear.com/SP233E for most up-to-date Ordering Information.
2. Visit www.maxlinear.com for additional information on Environmental Rating.

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