PACKAGE/ORDERING INFORMATION

MODEL	PIN-PACKAGE	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM7227	MSOP10	-40℃ to +85℃	SGM7227YMS10G/TR	SGM7227YMS10	Tape and Reel, 3000
	UTQFN1.8×1.4-10L	-40℃ to +85℃	SGM7227YUWQ10G/TR	7227	Tape and Reel, 3000

ABSOLUTE MAXIMUM RATINGS

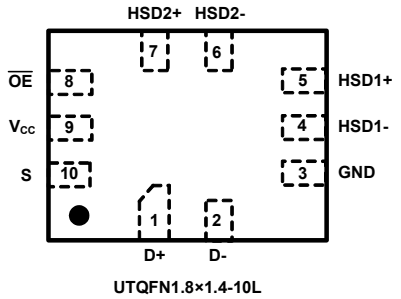
V_{CC} to GND..... 0V to 4.6V
Analog, Digital voltage range .....-0.3V to (V_{CC}) + 0.3V
Continuous Current HSDn or Dn…….....±50mA
Peak Current HSDn or Dn…….....±100mA
Operating Temperature Range.....-40℃ to +85℃
Junction Temperature..... 150℃
Storage Temperature.....-65℃ to +150℃
Lead Temperature (soldering, 10s).....260℃
ESD Susceptibility
HBM (UTQFN1.8×1.4-10L)……4000V
MM (UTQFN1.8×1.4-10L) ……...400V

NOTE:
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

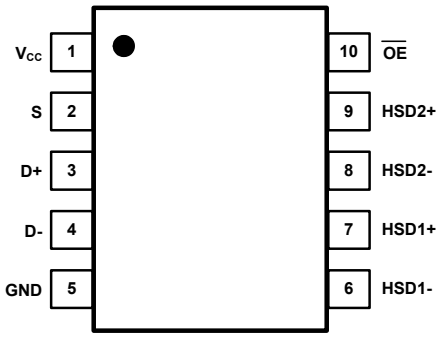
CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS (TOP VIEW)



UTQFN1.8×1.4-10L



MSOP10

PIN DESCRIPTION

PIN		NAME	FUNCTION
UTQFN1.8×1.4-10L	MSOP10		
9	1	V_{CC}	Power Supply
3	5	GND	Ground
10	2	S	Select Input
8	10	$\overline{OE}$	Output Enable
5	7	HSD1+	Multiplexed Source Inputs
4	6	HSD1-	Multiplexed Source Inputs
7	9	HSD2+	Multiplexed Source Inputs
6	8	HSD2-	Multiplexed Source Inputs
1	3	D+	USB Data Bus
2	4	D-	USB Data Bus

FUNCTION TABLE

$\overline{OE}$	S	HSD1+, HSD1-	HSD2+, HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	×	OFF	OFF

Switches Shown For Logic “0” Input

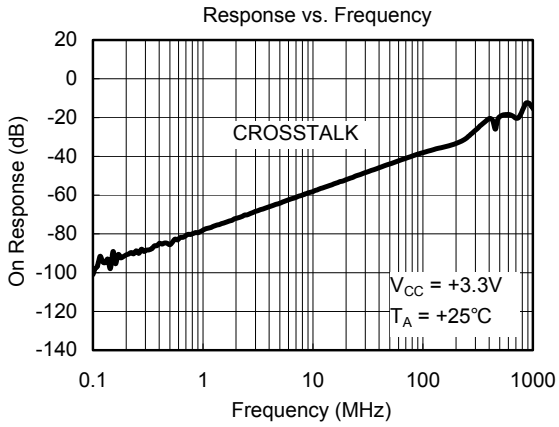
ELECTRICAL CHARACTERISTICS

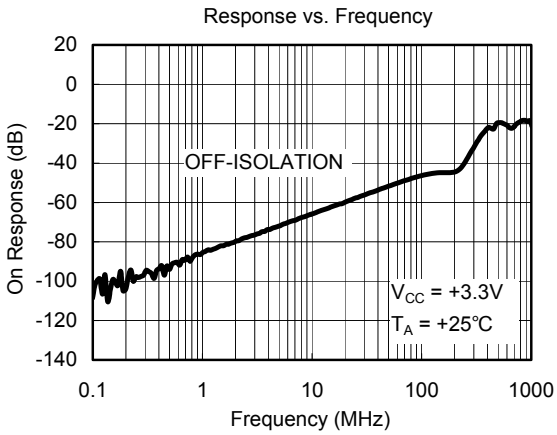
(V_{CC} = +3.3V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SWITCH						
Analog I/O Voltage (HSD1+, HSD1-, HSD2+, HSD2-)	V_{IS}		0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 3.0V, V_{IS} = 0V to 0.4V, I_D = 8mA, Test Circuit 1		5	9	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 3.0V, V_{IS} = 0V to 0.4V, I_D = 8mA, Test Circuit 1		0.3	0.8	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 3.0V, V_{IS} = 0V to 1.0V, I_D = 8mA, Test Circuit 1		1	2	Ω
Power Off Leakage Current (D+, D-)	I_{OFF}	V_{CC} = 0V, V_D = 0V to 3.6V, V_S , $V_{\overline{OE}}$ = 0V or 3.6 V			1	μA
Increase in I_{CC} per Control Voltage	I_{CCT}	V_{CC} = 3.6V, V_S or $V_{\overline{OE}}$ = 2.6V			5	μA
Source Off Leakage Current	$I_{HSD2(OFF)}$, $I_{HSD1(OFF)}$	V_{CC} = 3.6V, V_{IS} = 3.3V/ 0.3V, V_D = 0.3V/ 3.3V			1	μA
Channel On Leakage Current	$I_{HSD2(ON)}$, $I_{HSD1(ON)}$	V_{CC} = 3.6V, V_{IS} = 3.3V/ 0.3V, V_D = 3.3V/ 0.3V or floating			1	μA
DIGITAL INPUTS						
Input High Voltage	V_{IH}		1.6			V
Input Low Voltage	V_{IL}				0.5	V
Input Leakage Current	I_{IN}	V_{CC} = 3.0V, V_S , $V_{\overline{OE}}$ = 0V or V_{CC}			1	μA
DYNAMIC CHARACTERISTICS						
Turn-On Time	t_{ON}	V_{IS} = 0.8V, R_L = 50Ω, C_L = 10pF, Test Circuit 2		15		ns
Turn-Off Time	t_{OFF}			20		ns
Break-Before-Make Time Delay	t_D	V_{IS} = 0.8V, R_L = 50Ω, C_L = 10pF, Test Circuit 3		3.5		ns
Propagation Delay	t_{PD}	R_L = 50Ω, C_L = 10pF		0.5		ns
Off Isolation	O_{ISO}	Signal = 0dBm, R_L = 50Ω, f = 250MHz, Test Circuit 4		-35		dB
Channel-to-Channel Crosstalk	X_{TALK}	Signal = 0dBm, R_L = 50Ω, f = 250MHz, Test Circuit 5		-30		dB
–3dB Bandwidth	BW	Signal = 0dBm, R_L = 50Ω, C_L = 5pF, Test Circuit 6		550		MHz
Channel-to-Channel Skew	t_{SKEW}	R_L = 50Ω, C_L = 10pF		130		ps
Charge Injection Select Input to Common I/O	Q	V_G = GND, C_L = 1.0nF, R_G = 0Ω, Q = C_L x V_{OUT}, Test Circuit 7		10		pC
HSD+, HSD-, D+, D- ON Capacitance	C_{ON}	f = 1MHz		6.5		pF
		f = 250MHz		7		
POWER REQUIREMENTS						
Power Supply Range	V_{CC}		1.8		4.3	V
Power Supply Current	I_{CC}	V_{CC} = 3.0V, V_S , $V_{\overline{OE}}$ = 0V or V_{CC}			1	μA

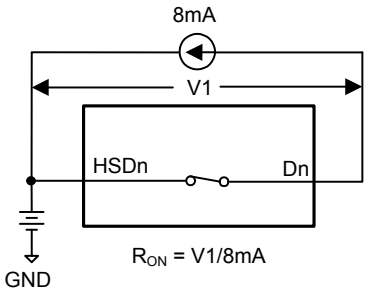
Specifications subject to changes without notice.

TYPICAL PERFORMANCE CHARACTERISTICS

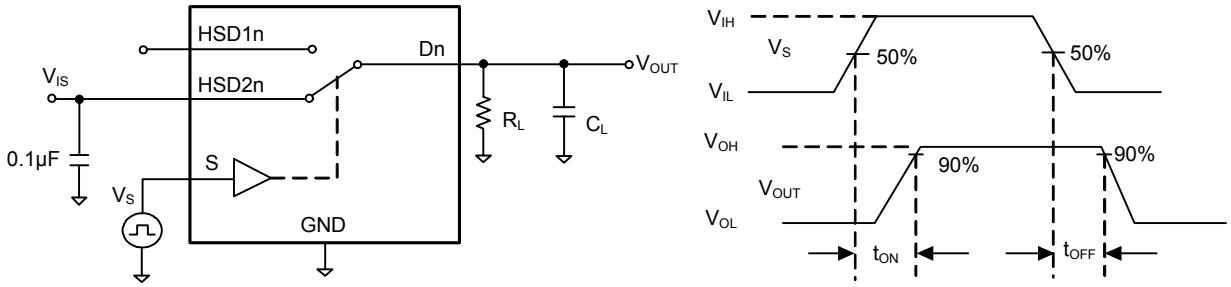




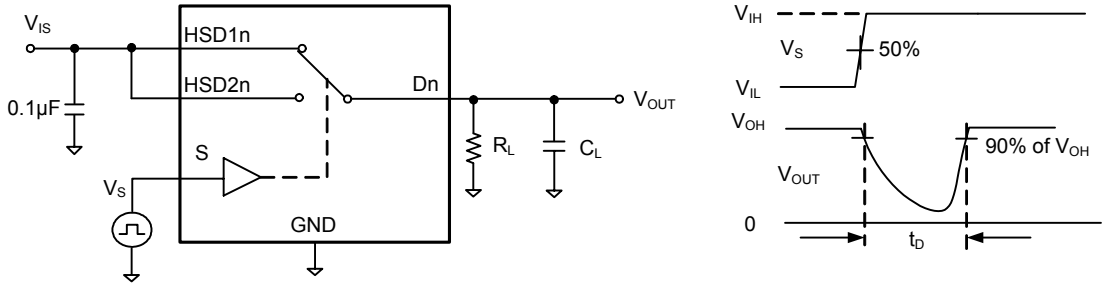
TEST CIRCUITS



Test Circuit 1. On Resistance

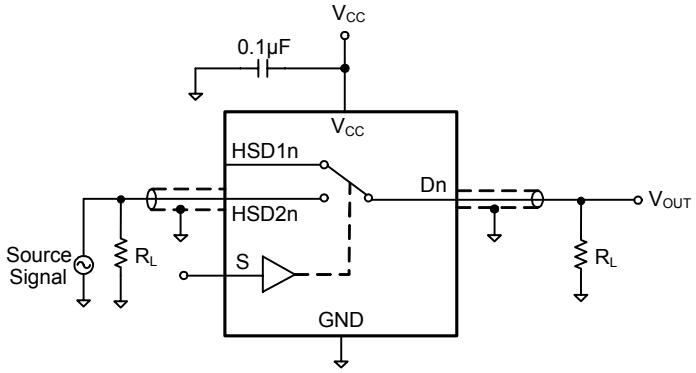


Test Circuit 2. Switching Times (t_{ON}, t_{OFF})

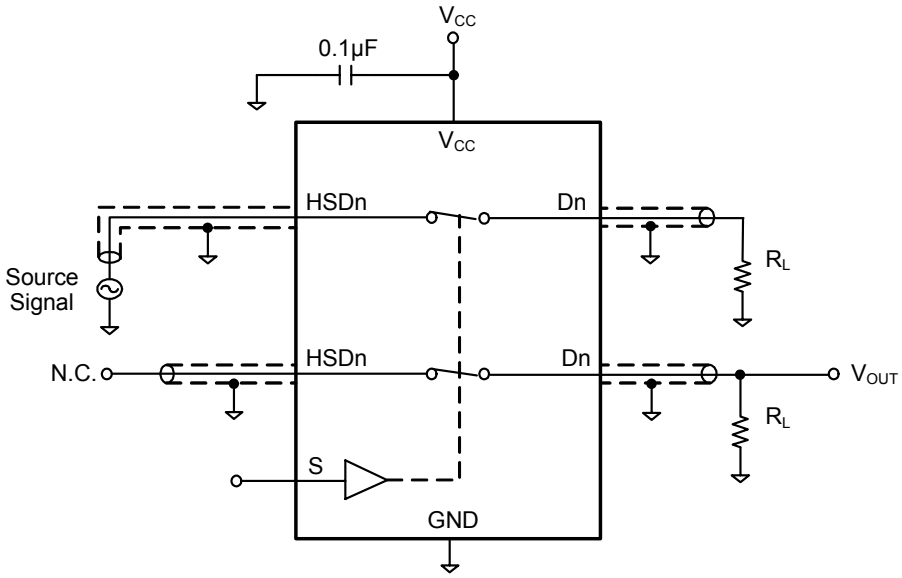


Test Circuit 3. Break-Before-Make Time (t_D)

TEST CIRCUITS (Cont.)



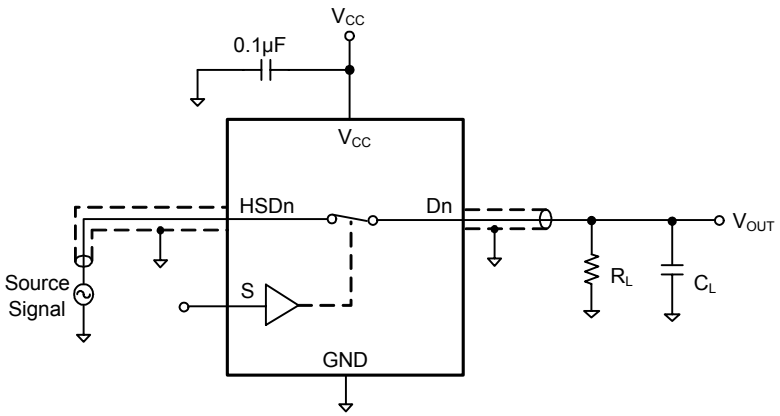
Test Circuit 4. Off Isolation



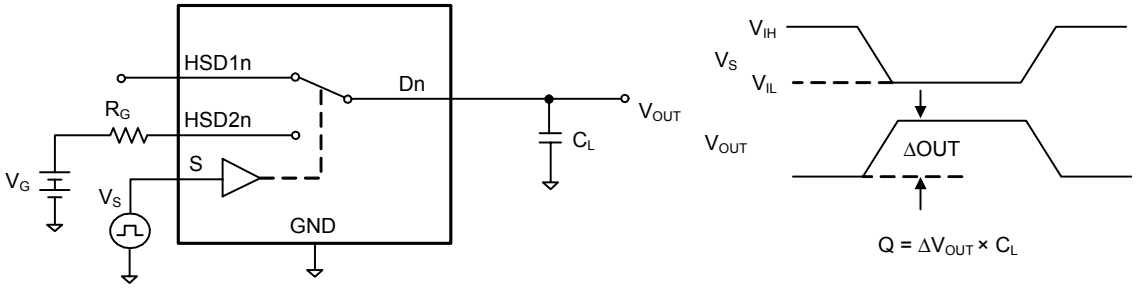
$$\text{Channel To Channel Crosstalk} = -20 \times \log \frac{V_{HSDn}}{V_{OUT}}$$

Test Circuit 5. Channel-to-Channel Crosstalk

TEST CIRCUITS (Cont.)



Test Circuit 6. -3dB Bandwidth



Test Circuit 7. Charge Injection (Q)

APPLICATION NOTES

Meeting USB 2.0 V_{BUS} Short Requirements

Power-Off Protection

For a V_{BUS} short circuit the switch is expected to withstand such a condition for at least 24 hours. The SGM7227 has specially designed circuitry which prevents unintended signal bleed through as well as guaranteed system reliability during a power-down, over-voltage condition. The protection has been added to the common pins (D+, D-).

Power-On Protection

The USB 2.0 specification also notes that the USB device should be capable of withstanding a V_{BUS} short during transmission of data. This modification works by limiting current flow back into the V_{CC} rail during the over-voltage event so current remains within the safe operating range.

SGM7227 USB2.0 Signal Quality Compliance Test Results

Figures 1 and 2 show the test results for USB eye diagram tests.

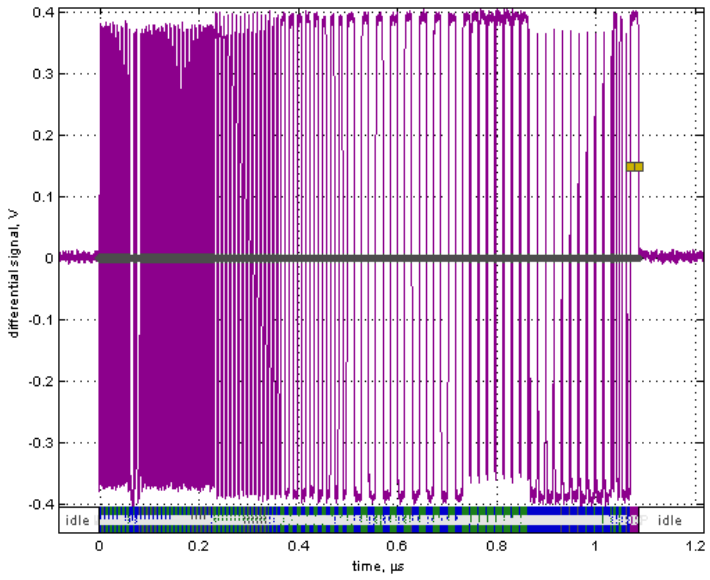


Figure 1. Waveform Plot

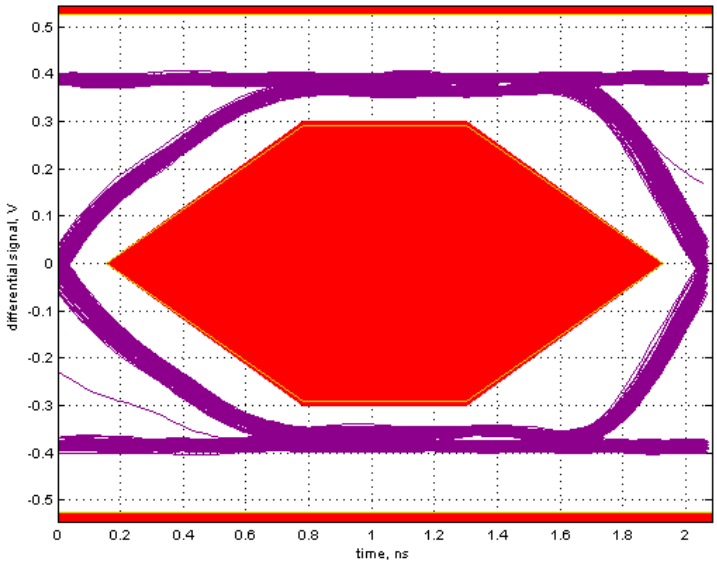


Figure 2. High Speed Signal Quality Eye Diagram Test (V+ = 3.3V)

The following is a summary of the USB test Results. The SGM7227 passes the high speed signal quality, eye diagram and jitter tests.

Required Tests

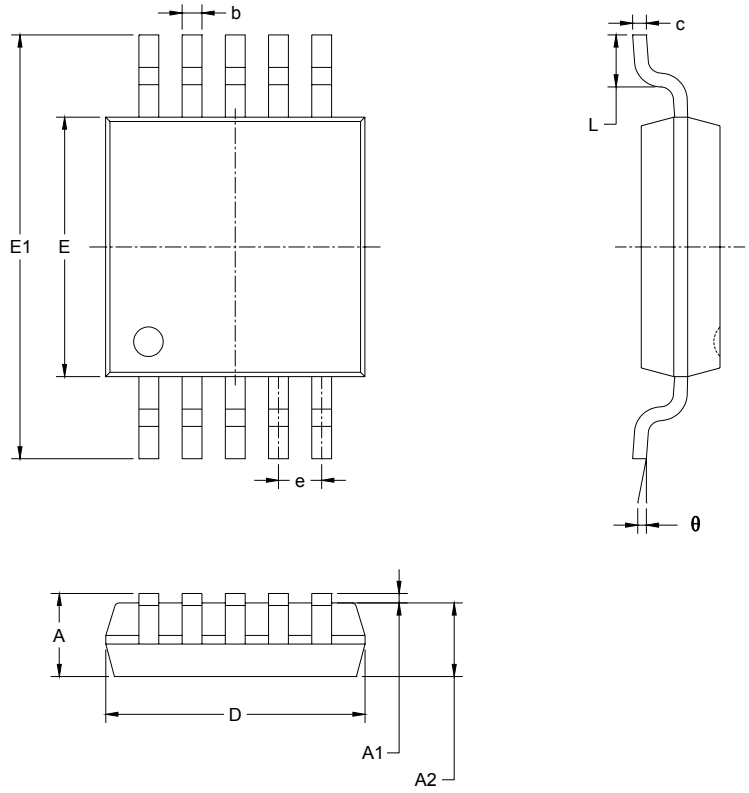
- Overall result:
  Pass!
- Signal eye:
  Eye passes
- EOP width: 7.91 bits
  EOP width passes
- Measured signaling rate: 480.0551 MHz
  Signal rate passes
- Rising Edge Rate: 901.28 V/us (710.10 ps equivalent risetime)
  Passes
- Falling Edge Rate: 889.18 V/us (719.77 ps equivalent risetime)
  Passes

Additional Information

Consecutive jitter range: -61.770 ps to 39.668 ps, RMS jitter 21.900 ps
Paired JK jitter range: -47.800 ps to 42.890 ps, RMS jitter 21.591 ps
Paired KJ jitter range: -50.590 ps to 49.704 ps, RMS jitter 23.281 ps

PACKAGE OUTLINE DIMENSIONS

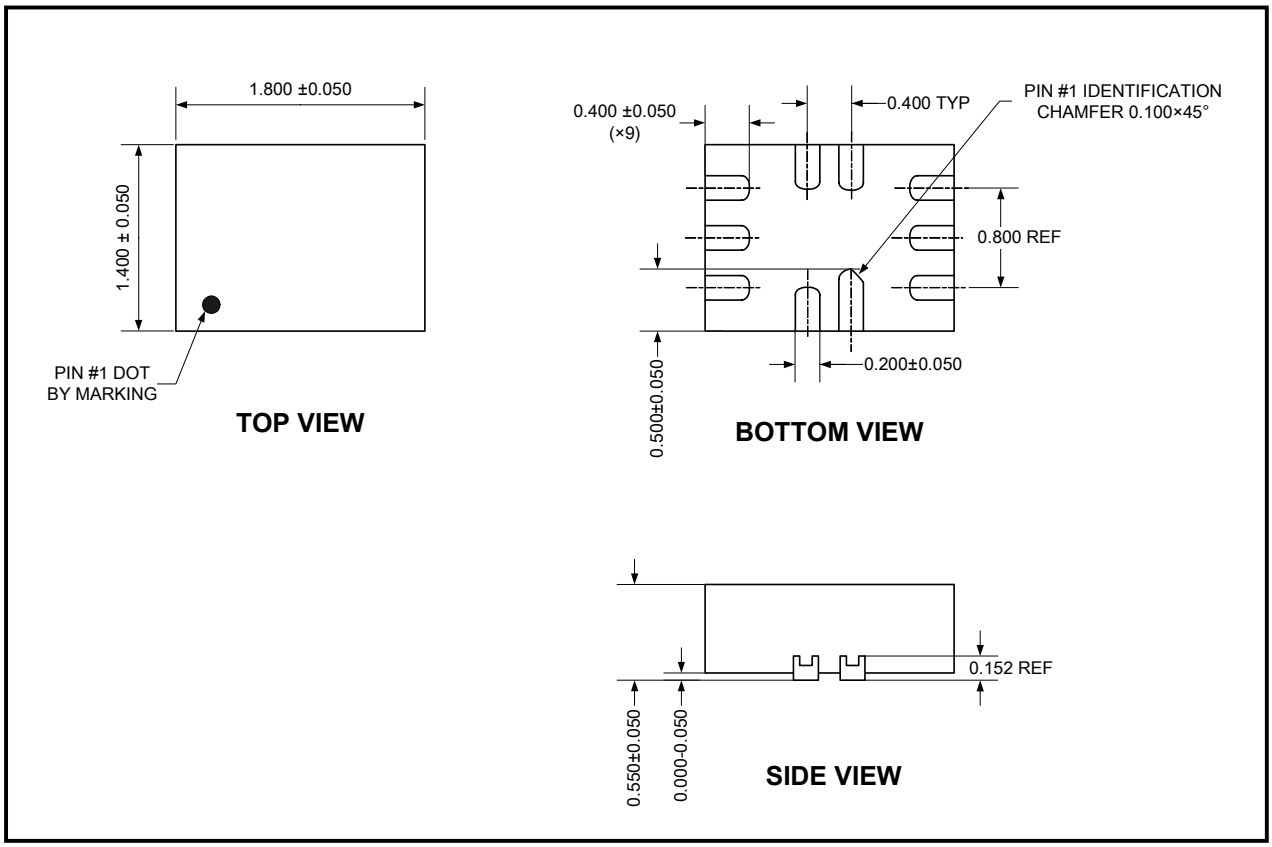
MSOP10



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

PACKAGE OUTLINE DIMENSIONS

UTQFN1.8×1.4-10L



NOTE: All linear dimensions are in millimeters.

REV. A

SGMICRO is dedicated to provide high quality and high performance analog IC products to customers. All SGMICRO products meet the highest industry standards with strict and comprehensive test and quality control systems to achieve world-class consistency and reliability.

For more information regarding SGMICRO Corporation and its products, please visit www.sg-micro.com