Pin Description

Pin #	Pin Name	I/O	Description
3	AI+	I	Positive CML Input Channel A with internal 50Ω pull down
4	AI-	I	Negative CML Input Channel A with internal 50Ω pull down
18	AO+	O	Positive CML Output Channel A with internal 50Ω pull up to VDD during normal operation and 2kΩ when EN=0. Drives to output common mode voltage when input is $<V_{TH-}$.
17	AO-	O	Negative CML Output Channel A with internal 50Ω pull up to VDD during normal operation and 2kΩ when EN=0. Drives to output common mode voltage when input is $<V_{TH-}$.
14	BI+	I	Positive CML Input Channel B with internal 50Ω pull down
13	BI-	I	Negative CML Input Channel B with internal 50Ω pull down
7	BO+	O	Positive CML Output Channel B with internal 50Ω pull up to VDD during normal operation and 2kΩ when EN=0. Drives to output common mode voltage when input is $<V_{TH-}$.
8	BO-	O	Negative CMLOutput Channel B with internal 50Ω pull up to VDD during normal operation and 2kΩ when EN=0. Drives to output common mode voltage when input is $<V_{TH-}$.
20	EN	I	EN is the enable pin. A LVCMOS high provides normal operation. A LVCMOS low selects a low power down mode.
5, 9, 12, 16	GND	PWR	Supply Ground
1	EQA	I	Selection pins for equalizer (see Equalizer Selection Table) w/ 50KΩ internal pull up
10	EQB	I	
2, 6, 11, 15, 19	V_{DD}	PWR	Supply Voltage, 1.5V to 1.8V (±0.1V)

Equalizer Selection

EQx	Compliance Channel
0	[0:2.5dB] @ 1.6 GHz
1	[4.5:6.5dB] @ 1.6 GHz

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +2.5V
DC SIG Voltage	–0.5V to V_{CC} +0.5V
Current Output	-25mA to +25mA
Power Dissipation Continous	500mW
Operating Temperature	0 to +70°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Ps	Supply Power	EN = LVCMOS Low			0.1	W
		EN = LVCMOS High			0.3	
	Latency	From input to output		2.0		ns
CML Receiver Input						
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.200			V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH-SD}	Signal Detect Threshold	EN = High	50		200	
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	Ω
Z_{RX-DC}	DC Input Impedance		40	50	60	
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p
		Deterministic jitter			0.2	
J_{RM}	Random Jitter(1,2)			1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. JItter is measured at 0V at point C of Figure 1.

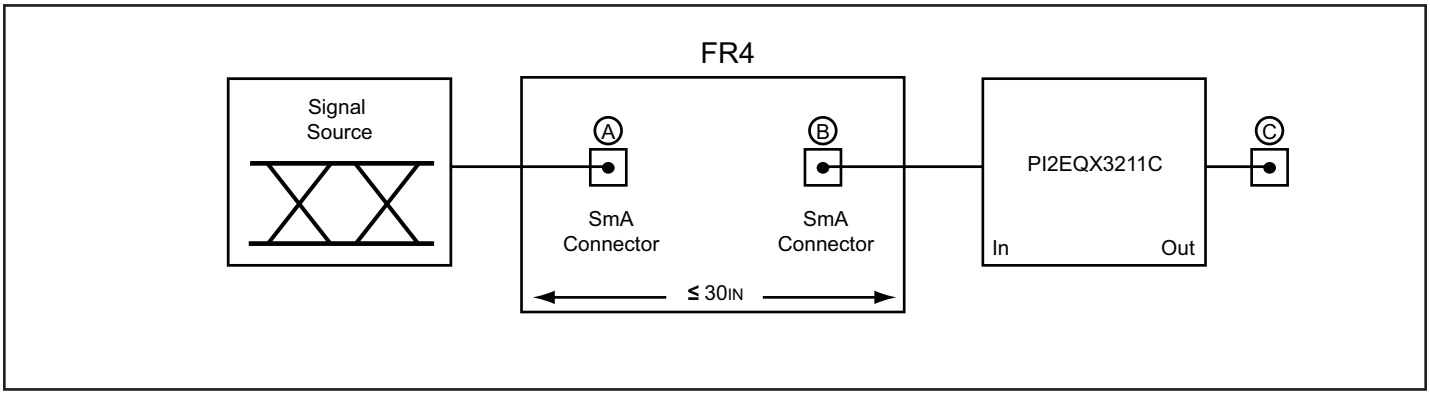


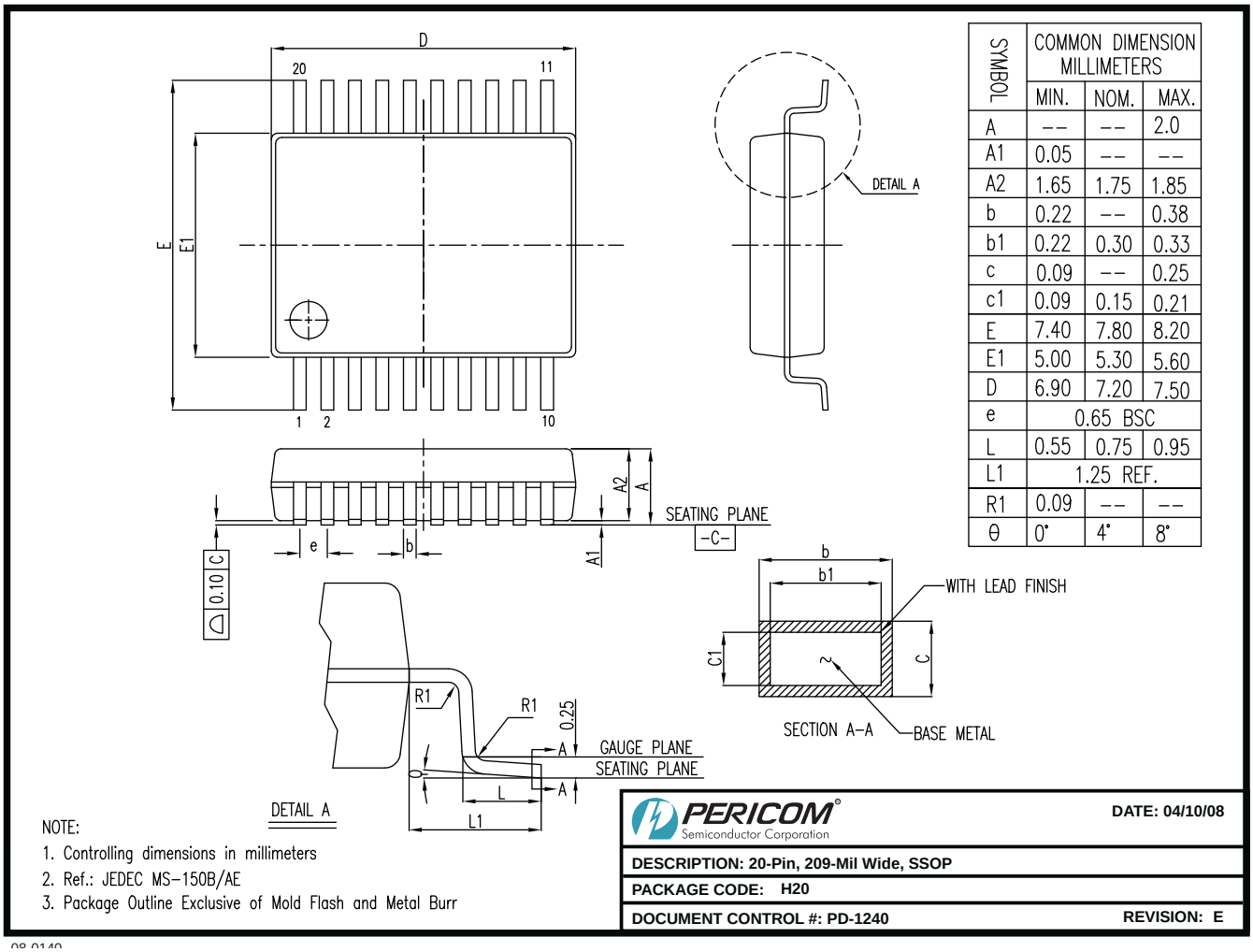
Figure 1. Test Condition Referenced in the Electrical Characteristic Table

AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)						
V_{DIFFP}	Output Voltage Swing	Differential Swing $\lvert V_{TX-D+} - V_{TX-D-} \rvert$	200		375	mVp-p
$V_{TX-DIFFP-P}$	Differential Peak-to-peak Ouput Voltage	$V_{TX-DIFFP-P} = 2 * \lvert V_{TX-D+} - V_{TX-D-} \rvert$	400		750	mV
V_{TX-C} (2)	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert / 2$		V_{DD} - 0.3		V
t_F, t_R	Transition Time	20% to 80% (1)			150	ps
Z_{OUT}	Output resistance	Single ended	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ω
C_{TX}	AC Coupling Capacitor		0.3	4.7	12	nF
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}			V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				250	µA
I_{IL}	Input Low Current				500	

Note:
1. Using K28.7 (0011111000) pattern) .
2. The parameter is determined by device characterization, and is not production tested

Packaging Mechanical: 20-lead SSOP (H20)



SYMBOL	COMMON DIMENSION MILLIMETERS		
	MIN.	NOM.	MAX.
A	--	--	2.0
A1	0.05	--	--
A2	1.65	1.75	1.85
b	0.22	--	0.38
b1	0.22	0.30	0.33
c	0.09	--	0.25
c1	0.09	0.15	0.21
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
D	6.90	7.20	7.50
e	0.65 BSC		
L	0.55	0.75	0.95
L1	1.25 REF.		
R1	0.09	--	--
θ	0°	4°	8°

08-0140

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX3211BHE	H	Pb-Free and Green 20-lead SSOP

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel