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Data sheet status	
Objective product specification	This product specification contains target specifications for product development.
Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Writing conventions

This product specification follows a set of typographic rules that makes the document consistent and easy to read. The following writing conventions are used:

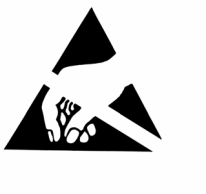
- Commands, bit state conditions, and register names are written in `Courier`.
- Pin names and pin signal conditions are written in **`Courier bold`**.
- Cross references are underlined and highlighted in blue.

Revision history

Date	Version	Description
June 2006	1.4	
April 2008	1.5	• Restructured layout in the new template • Updated package information • Added moisture sensitivity level to the absolute maximum ratings

Attention!

Observe precaution for handling
Electrostatic Sensitive Device.



Datasheet order code: 051005nRF905

Contents

1 Introduction

nRF905 is a single chip radio transceiver for the 433/868/915MHz ISM band. The transceiver consists of a fully integrated frequency synthesizer, receiver chain with demodulator, a power amplifier, a crystal oscillator and, a modulator. The ShockBurst™ feature automatically handles preamble and CRC. You can easily configure the nRF905 through the SPI. Current consumption is very low, in transmit only 9mA at an output power of -10dBm, and in receive mode 12.5mA. Built-in power down modes makes power saving easily realizable.

2 Quick reference data

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum transmit output power	10	dBm
Data rate	50	kbps
Supply current in transmit @ -10dBm output power	9	mA
Supply current in receive mode	12.5	mA
Temperature range	-40 to +85	°C
Typical sensitivity	-100	dBm
Supply current in power down mode	2.5	µA

Table 1. nRF905 quick reference data.

3 Block Diagram

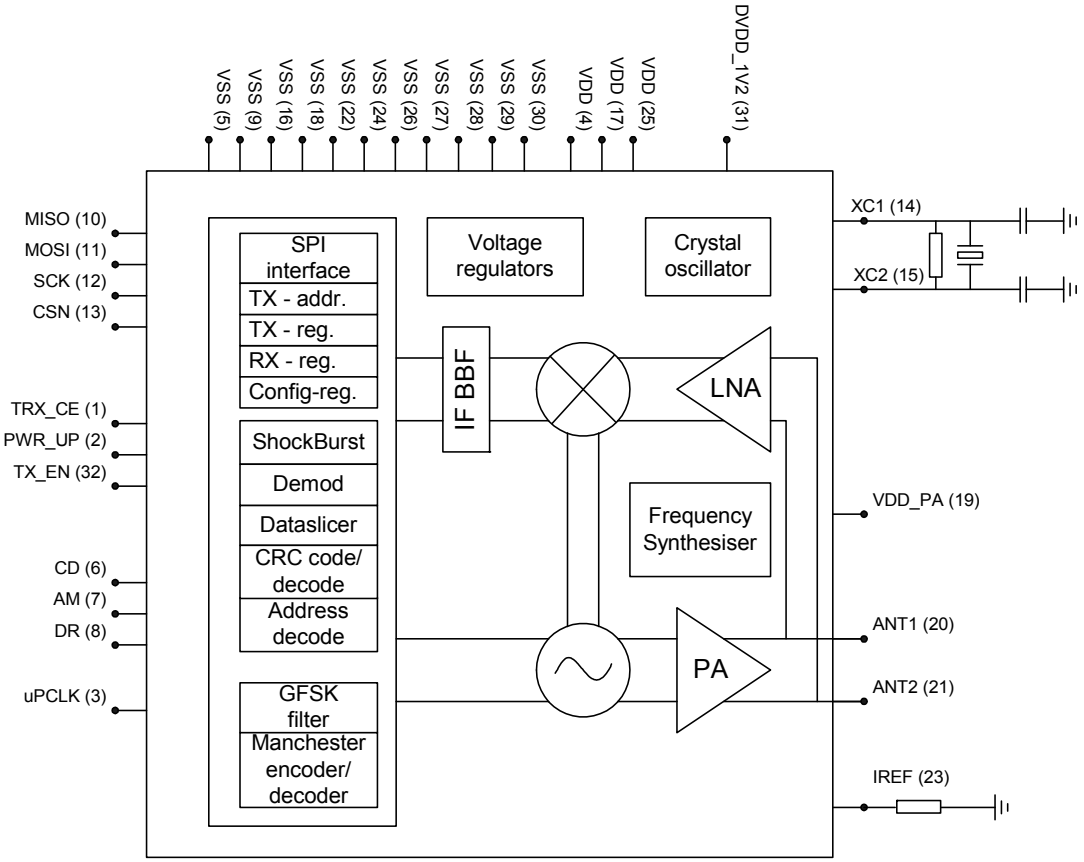


Figure 1. nRF905 with external components.

4 Absolute maximum ratings

Operating conditions	Minimum	Maximum	Units
Supply voltages			
VDD	-0.3	+3.6	V
VSS		0	V
Input voltage			
V_I	-0.3	VDD +0.3	V
Output voltage			
V_O	-0.3	VDD +0.3	V
Total power dissipation			
P_D (T_A=85°C)		200	mW
Temperatures			
Operating temperature	-40	+85	°C
Storage temperature	-40	+125	°C
Moisture sensitivity level			
		260	°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Table 2. Absolute maximum ratings

5 Electrical Specifications

Conditions: VDD = +3V VSS = 0V, TEMP = -40ºC to +85ºC (typical +27ºC)

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage		1.9		3.6	V
TEMP	Operating temperature		-40		85	ºC

Table 3. Operating conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{IH}	HIGH level input voltage		0.7·VDD		VDD	V
V_{IL}	LOW level input voltage		VSS		0.3·VDD	V
Ci	Pin capacitance				5	pF
I_{iL}	Pin leakage current	a			±10	nA
V_{OH}	HIGH level output voltage (I_{OH}=-0.5mA)		VDD-0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.5mA)		VSS		0.3	V

a. Max value determined by design and characterization testing.

Table 4. Digital input/output

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
I_{stby_eclk}	Supply current in standby, uCLK enabled	a		100		µA
I_{stby_dclk}	Supply current in standby, uCLK disabled	b		12.5		µA
I_{PD}	Supply current in power down mode	c		2.5		µA
I_{SPI}	Supply current in SPI programming	d		20		µA

a. Output frequency is 4MHz load of external clock pin is 5pF, Crystal is 4MHz.
b. Crystal is 4MHz.
c. Pin voltages are VSS or VDD.
d. Chip in power down, SPI_SCK frequency is 1MHz.

Table 5. Electrical specifications

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
f_{OP}	Operating frequency	a	430		928	MHz
f_{XTAL}	Crystal frequency	b	4		20	MHz
Δf	Frequency deviation		±42	±50	±58	kHz
BR	Data rate	c		50		kbps
f_{CH433}	Channel spacing for 433MHz band			100		kHz
$f_{CH868/915}$	Channel spacing for 868/ 915MHz band			200		kHz

a. Operates in the 433, 868 and 915MHz ISM band.
b. The crystal frequency may be chosen from 5 different values (4, 8, 12, 16, and 20MHz).
c. Data is Manchester encoded before GFSK modulation.

Table 6. General RF conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
P_{RF10}	Output power 10dBm setting	a	7	10	11	dBm
P_{RF6}	Output power 6dBm setting	a	3	6	9	dBm
P_{RF-2}	Output power –2dBm setting	a	-6	-2	2	dBm
P_{RF-10}	Output power -10dBm setting	a	-14	-10	-6	dBm
P_{BW_-16}	-16dBc bandwidth for modulated carrier	b		173		kHz
P_{BW_-24}	-24dBc bandwidth for modulated carrier	b		222		kHz
P_{BW_-32}	-32dBc bandwidth for modulated carrier	b		238		kHz
P_{BW_-36}	-36dBc bandwidth for modulated carrier	b		313		kHz
P_{RF1}	1st adjacent channel transmit power	c		-27		dBc
P_{RF2}	2nd adjacent channel transmit power	c		-54		dBc
$I_{TX10dBm}$	Supply current @ 10dBm output power			30		mA
$I_{TX-10dBm}$	Supply current @ -10dBm output power			9		mA

a. Optimum load impedance, please see peripheral RF information.
b. Data is Manchester encoded before GFSK modulation.
c. Channel width and channel spacing is 200kHz.

Table 7. Transmitter operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
I_{RX}	Supply current in receive mode			12.5		mA
RX_{SENS}	Sensitivity at 0.1%BER			-100		dBm
RX_{MAX}	Maximum received signal		0			dBm
C/I_{CO}	C/I Co-channel	a		13		dB
C/I_{1ST}	1st adjacent channel selectivity C/I 200kHz	a		-7		dB
C/I_{2ND}	2nd adjacent channel selectivity C/I 400kHz	a		-16		dB
C/I_{+1M}	Blocking at +1MHz	a		-40		dB
C/I_{-1M}	Blocking at -1MHz	a		-50		dB
C/I_{-2M}	Blocking at -2MHz	a		-63		dB

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
C/I_{+5M}	Blocking at +5MHz	a		-70		dB
C/I_{-5M}	Blocking at -5MHz	a		-65		dB
C/I_{+10M}	Blocking at +10MHz	a		-69		dB
C/I_{-10M}	Blocking at -10MHz	a		-67		dB
C/I_{IM}	Image rejection	a		-36		dB

a. Channel Level +3dB over sensitivity, interfering signal a standard CW, image lies 2MHz above wanted.

Table 8. Receiver operation

6 Current Consumption

Mode	Crystal freq. (MHz)	Output clock Freq. (MHz)	Typical current
Power Down	16	OFF	2.5uA
Standby	4	OFF	12uA
Standby	8	OFF	25uA
Standby	12	OFF	27uA
Standby	16	OFF	32uA
Standby	20	OFF	46uA
Standby	4	0.5	110uA
Standby	8	0.5	125uA
Standby	12	0.5	130uA
Standby	16	0.5	135uA
Standby	20	0.5	150uA
Standby	4	1	130uA
Standby	8	1	145uA
Standby	12	1	150uA
Standby	16	1	155uA
Standby	20	1	170uA
Standby	4	2	170uA
Standby	8	2	185uA
Standby	12	2	190uA
Standby	16	2	195uA
Standby	20	2	210uA
Standby	4	4	260uA
Standby	8	4	275uA
Standby	12	4	280uA
Standby	16	4	285uA
Standby	20	4	300uA
Rx @ 433	16	OFF	12.2mA
Rx @ 868/915	16	OFF	12.8mA
Reduced Rx	16	OFF	10.5mA
Tx @ 10dBm	16	OFF	30mA
Tx @ 6dBm	16	OFF	20mA
Tx @ -2dBm	16	OFF	14mA
Tx @ -10dBm	16	OFF	9mA
Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load capacitance of external clock = 13pF, Crystal load capacitance = 12pF			

Table 9. nRF905 current consumption

7 Pin information

7.1 Pin Assignment

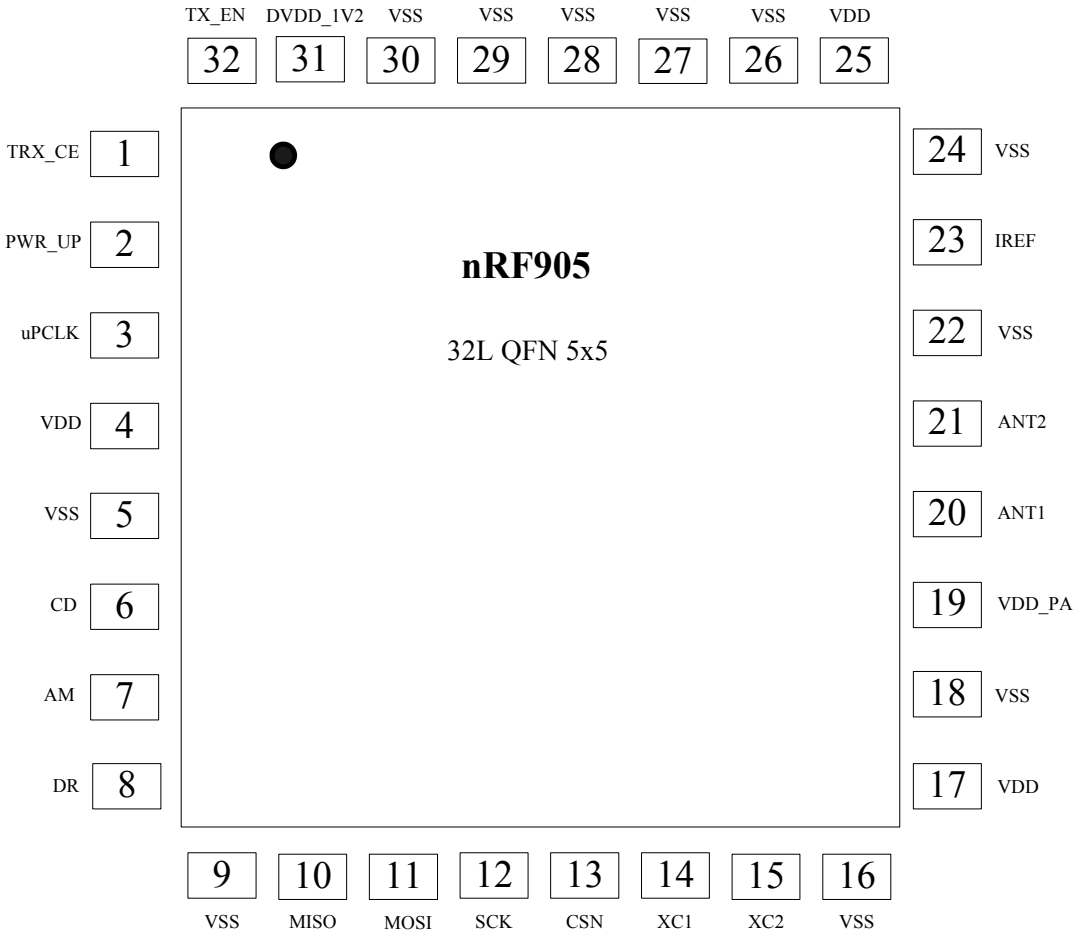


Figure 2. nRF905 pin assignment (top view) for a 32L QFN 5x5 package

7.2 Pin Functions

Pin	Name	Pin function	Description
1	TRX_CE	Digital input	Enables chip for receive and transmit
2	PWR_UP	Digital input	Power up chip
3	uPCLK	Clock output	Output clock, divided crystal oscillator full swing clock
4	VDD	Power	Power supply (+3V DC)
5	VSS	Power	Ground (0V)
6	CD	Digital output	Carrier Detect
7	AM	Digital output	Address Match
8	DR	Digital output	Receive and transmit Data Ready
9	VSS	Power	Ground (0V)
10	MISO	SPI - interface	SPI output
11	MOSI	SPI - interface	SPI input
12	SCK	SPI - Clock	SPI clock
13	CSN	SPI - enable	SPI enable, active low
14	XC1	Analog Input	Crystal pin 1/ External clock reference pin
15	XC2	Analog Output	Crystal pin 2
16	VSS	Power	Ground (0V)
17	VDD	Power	Power supply (+3V DC)
18	VSS	Power	Ground
19	VDD_PA	Power output	Positive supply (1.8V) to nRF905 power amplifier
20	ANT1	RF	Antenna interface 1
21	ANT2	RF	Antenna interface 2
22	VSS	Power	Ground (0V)
23	IREF	Analog Input	Reference current
24	VSS	Power	Ground (0V)
25	VDD	Power	Power supply (+3V DC)
26	VSS	Power	Ground (0V)
27	VSS	Power	Ground (0V)
28	VSS	Power	Ground (0V)
29	VSS	Power	Ground (0V)
30	VSS	Power	Ground (0V)
31	DVDD_1V2	Power	Low voltage positive digital supply output for decoupling
32	TX_EN	Digital input	TX_EN=”1”TX mode, TX_EN=”0”RX mode

Table 10. nRF905 pin function.

8 Modes of Operation

The nRF905 has two active (RX/TX) modes and two power saving modes:

8.1 Active Modes

- ShockBurst™ RX
- ShockBurst™ TX

8.2 Power Saving Modes

- Power down and SPI programming
- Standby and SPI programming

The nRF905 mode is decided by the settings of TRX_CE, TX_EN and PWR_UP.

PWR_UP	TRX_CE	TX_EN	Operating Mode
0	X	X	Power down and SPI programming
1	0	X	Standby and SPI programming
1	X	0	Read data from RX register
1	1	0	Radio Enabled - ShockBurst™ RX
1	1	1	Radio Enabled - ShockBurst™ TX

Table 11. nRF905 operational modes.

8.3 nRF ShockBurst™ Mode

The nRF905 uses the ShockBurst™ feature. ShockBurst™ makes it possible to use the high data rate offered by the nRF905 without the need of a costly, high-speed microcontroller (MCU) for data processing/clock recovery. By placing all high speed signal processing related to RF protocol on-chip, the nRF905 offers the application microcontroller a simple SPI, the data rate is decided by the interface speed the microcontroller sets up. By allowing the digital part of the application to run at low speed, while maximizing the data rate on the RF link, the nRF905 ShockBurst™ mode reduces the average current consumption in applications. In ShockBurst™ RX, Address Match (AM) and Data Ready (DR) notifies the MCU when a valid address and payload is received respectively. In ShockBurst™ TX, the nRF905 automatically generates preamble and CRC. Data Ready (DR) notifies the MCU that the transmission is completed. This means reduced memory demand in the MCU resulting in a low cost MCU, as well as reduced software development time.

8.4 Typical ShockBurst™ TX

1. When the application MCU has data for a remote node, the address of the receiving node (TX-address) and payload data (TX-payload) are clocked into nRF905 through the SPI. The application protocol or MCU sets the speed of the interface.
2. MCU sets TRX_CE and TX_EN high, this activates a nRF905 ShockBurst™ transmission.
3. nRF905 ShockBurst™ does the following:
   - Radio is automatically powered up.
   - Data packet is completed (preamble added, CRC calculated).
   - Data packet is transmitted (50kbps).
   - Data Ready is set high when transmission is completed.

4. If AUTO_RETRAN is set high, the nRF905 continuously retransmits the packet until TRX_CE is set low.
5. When TRX_CE is set low, the nRF905 finishes transmitting the outgoing packet and then sets itself into standby mode.

If TX_EN is set low while TRX_CE is kept high, the nRF905 finishes transmitting the outgoing packet and enters RX mode in the channel already programmed in the RF-CONFIG register.

The ShockBurst™ mode ensures that a transmitted packet that has started always finishes regardless of what TRX_EN and TX_EN are set to during transmission. The new mode is activated when the transmission is completed.

For test purposes such as antenna tuning and measuring output power it is possible to set the transmitter so that a constant carrier is produced. To do this, TRX_CE must be maintained high instead of being pulsed and Auto Retransmit should be switched off. After the burst of data is sent the device continues to send the unmodulated carrier.

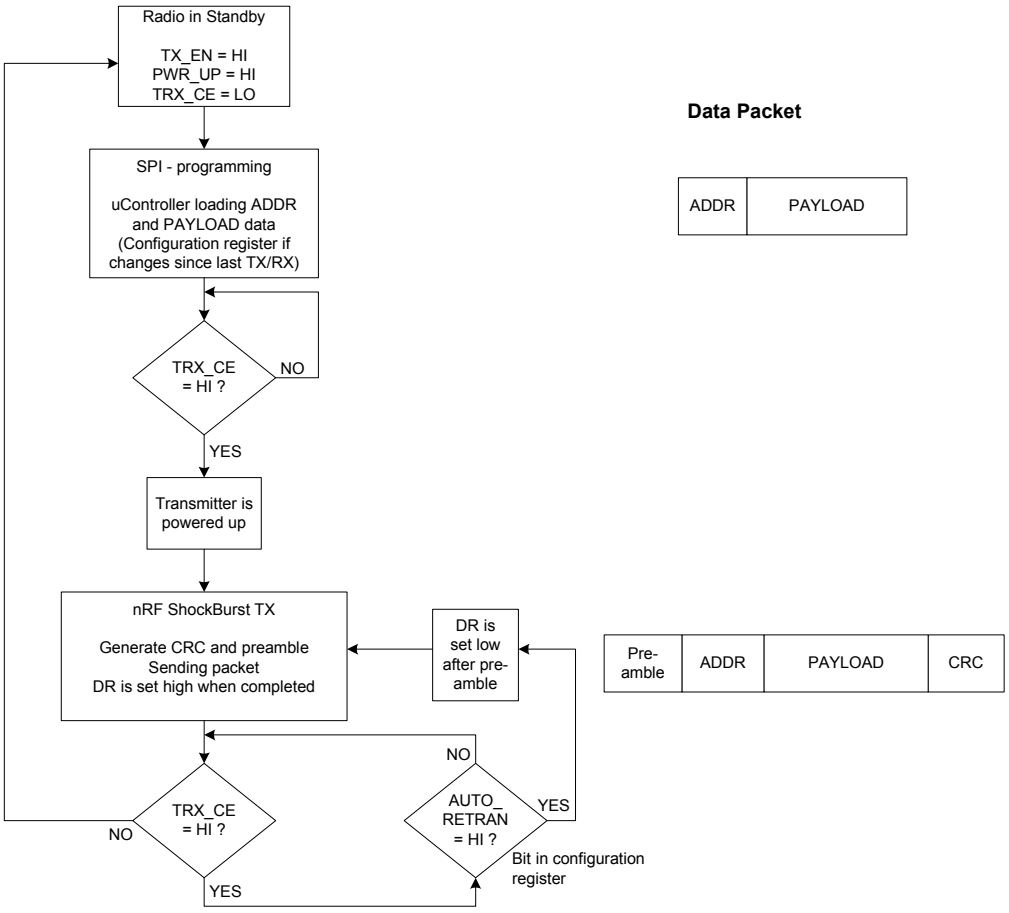


Figure 3. Flowchart ShockBurst™ transmit of nRF905.

Note: When DR is set high it can be set low again under the following conditions:
- If TX_EN is set low
- If PWR_UP is set low

8.5 Typical ShockBurst™ RX

1. ShockBurst™ RX is selected by setting TRX_CE high and TX_EN low.
2. After 650µs nRF905 is monitoring the air for incoming communication.
3. When the nRF905 senses a carrier at the receiving frequency, Carrier Detect (CD) pin is set high.
4. When a valid address is received, Address Match (AM) pin is set high.
5. When a valid packet has been received (correct CRC found), nRF905 removes the preamble, address and CRC bits, and the Data Ready (DR) pin is set high.
6. MCU sets the TRX_CE low to enter standby mode (low current mode).
7. MCU can clock out the payload data at a suitable rate through the SPI.
8. When all payload data is retrieved, nRF905 sets Data Ready (DR) and Address Match (AM) low again.
9. The chip is now ready for entering ShockBurst™ RX, ShockBurst™ TX or, power down mode.

If TX_EN is set high while TRX_CE is kept high, the nRF905 would enter ShockBurst™ TX and start a transmission according to the present contents in the SPI registers.

If TRX_CE or TX_EN is changed during an incoming packet, the nRF905 changes mode immediately and the packet is lost. However, if the MCU is sensing the Address Match (AM) pin, it knows when the chip is receiving an incoming packet and can therefore decide whether to wait for the Data Ready (DR) signal or enter a different mode.

To avoid spurious address matches it is recommended that the address length be 24 bits or higher in length. Small addresses such as 8 or 16 bits can often lead to statistical failures due to the address being repeated as part of the data packet. This can be avoided by using a longer address.

Each byte within the address should be unique. Repeating bytes within the address reduces the effectiveness of the address and increases its susceptibility to noise which increases the packet error rate. The address should also have several level shifts (that is, 10101100) reducing the statistical effect of noise and the packet error rate.

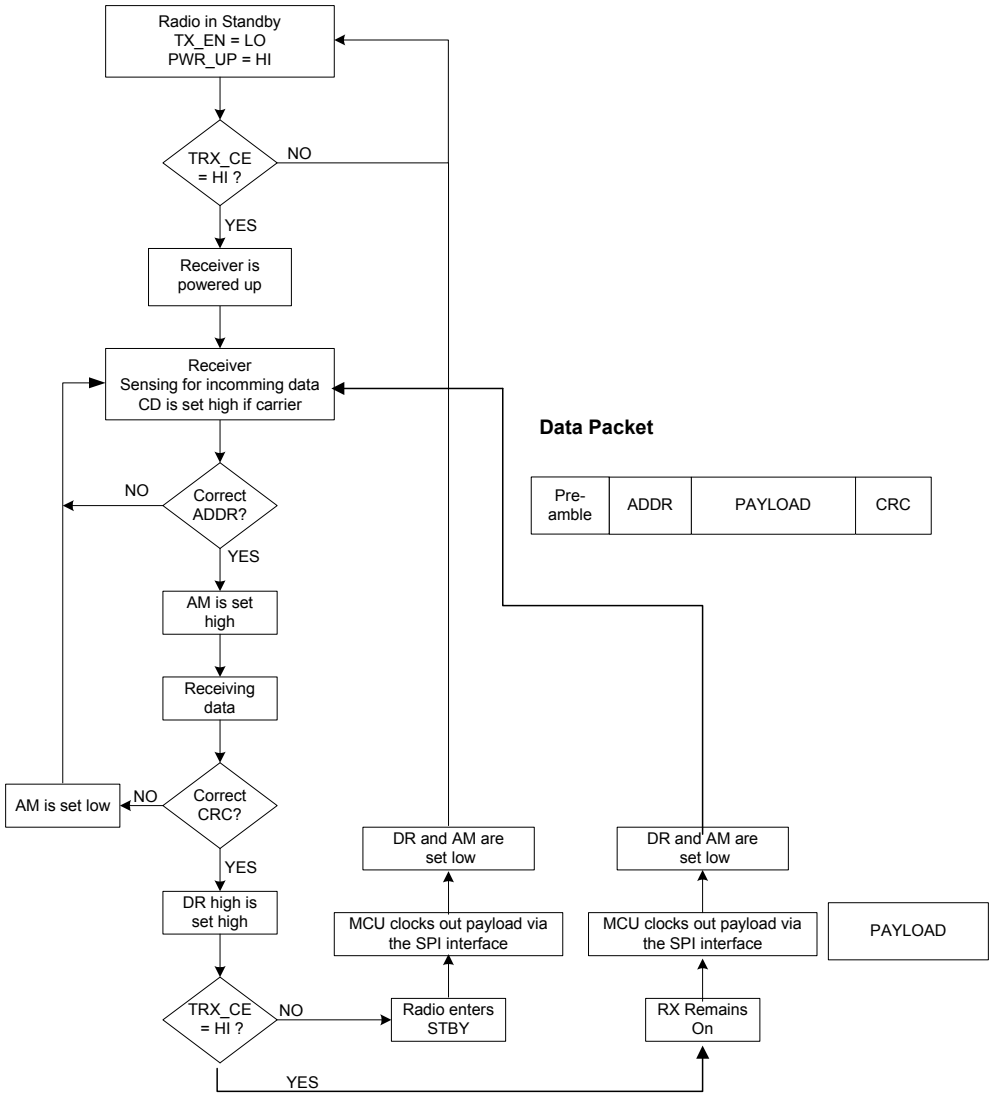


Figure 4. Flowchart ShockBurst™ receive of nRF905.

8.6 Power Down Mode

In power down the nRF905 is disabled with minimal current consumption, typically less than 2.5µA. When the device enters this mode it is not active which minimizes average current consumption and maximizes battery lifetime. The configuration word content is maintained during power down.

8.7 Standby Mode

Standby mode is used to minimize average current consumption while maintaining short start up times to ShockBurst™ RX and ShockBurst™ TX. In this mode part of the crystal oscillator is active. Current consumption is dependent on crystal frequency, Ex: I_{DD}= 12µA @4MHz and I_{DD} =46µA @20MHz. If the uP-clock (pin 3) of nRF905 is enabled, current consumption increases and is dependent on the load capacitance and frequency. The configuration word content is maintained during standby.

9 Device Configuration

All configuration of the nRF905 is through the SPI. The interface consists of five registers. A SPI instruction set is used to decide which operation shall be performed. The SPI can be activated in any mode however, we recommend that the chip is in standby or power down mode.

9.1 SPI Register Configuration

The SPI consists of five internal registers. A register readback mode is implemented to allow verification of the register contents.

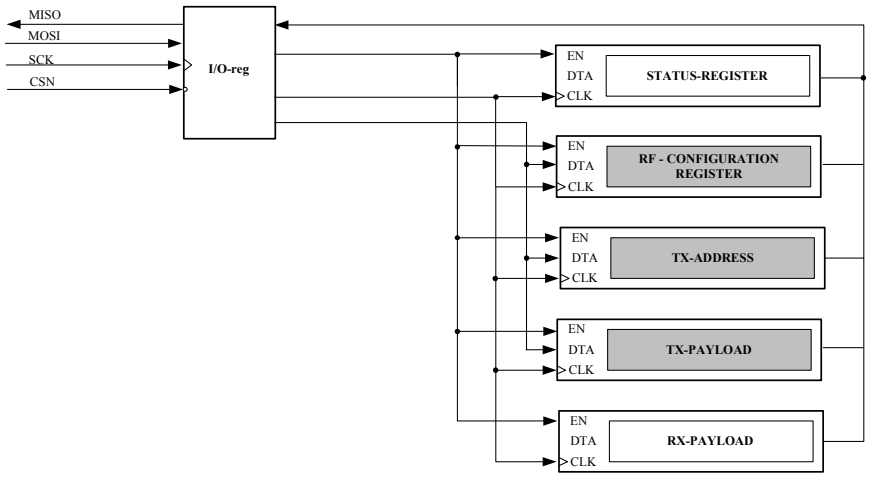


Figure 5. SPI – interface and the five internal registers.

Internal registers	Description
Status – Register	Register contains status of Data Ready (DR), Address Match (AM).
RF – Configuration Register	Register contains transceiver setup information such as frequency and output power ext.
TX – Address	Register contains address of target device. How many bytes used is set in the configuration register.
TX – Payload	Register containing the payload information to be sent in a ShockBurst™ packet. How many bytes used is set in the configuration register.
RX – Payload	Register containing the payload information derived from a received valid ShockBurst ™ packet. How many bytes used is set in the configuration register. Valid data in the RX-Payload register is indicated with a high Date Ready (DR) signal.

Table 12. Internal registers description

9.2 SPI Instruction Set

The available commands used on the SPI are shown below. Whenever CSN is set low the interface expects an instruction. Every new instruction must be started by a high to low transition on CSN.

Instruction set for the nRF905 SPI		
Instruction Name	**Instruction Format**	**Operation**
W_CONFIG (WC)	0000 AAAA	Write Configuration register. AAAA indicates which byte the write operation is to be started from. Number of bytes depends on start address AAAA.
R_CONFIG (RC)	0001 AAAA	Read Configuration register. AAAA indicates which byte the read operation is to be started from. Number of bytes depends on start address AAAA.
W_TX_PAYLOAD (WTP)	0010 0000	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0.
R_TX_PAYLOAD (RTP)	0010 0001	Read TX-payload: 1 – 32 bytes. A read operation always starts at byte 0.
W_TX_ADDRESS (WTA)	0010 0010	Write TX-address: 1 – 4 bytes. A write operation always starts at byte 0.
R_TX_ADDRESS (RTA)	0010 0011	Read TX-address: 1 – 4 bytes. A read operation always starst at byte 0
R_RX_PAYLOAD (RRP)	0010 0100	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0.
CHANNEL_CONFIG (CC)	1000 pphc cccc cccc	Special command for fast setting of CH_NO, HFREQ_PLL and PA_PWR in the CONFIGURATION REGISTER. CH_NO= ccccccccc, HFREQ_PLL = h PA_PWR = pp
STATUS REGISTER	N.A.	The content of the status register (S[7:0]) is always read to MISO after a high to low transition on CSN as shown in Figure 6. and Figure 7.

Table 13. Instruction set for the nRF905 SPI.

A read or a write operation may operate on a single byte or on a set of succeeding bytes from a given start address defined by the instruction. When accessing succeeding bytes, you read or write the MSB of the byte with the smallest byte number first.

9.3 SPI Timing

The interface supports SPI mode 0. SPI operation and timing is given in Figure 6. to Figure 8. and in Table 14.. The device must be in one of the power saving modes for you to read or write to the configuration registers.

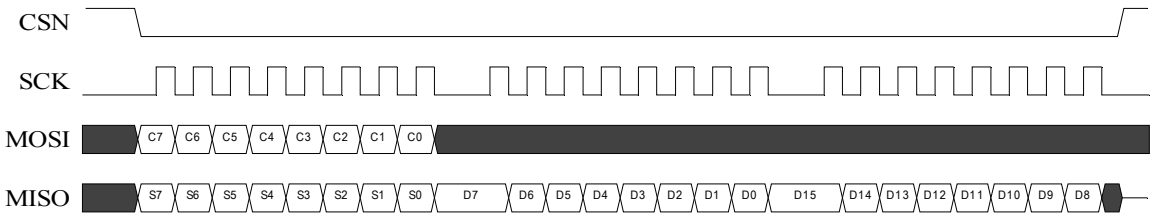


Figure 6. SPI read operation.

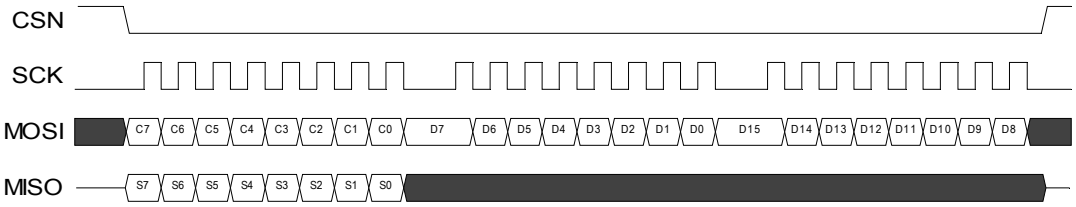


Figure 7. SPI write operation.

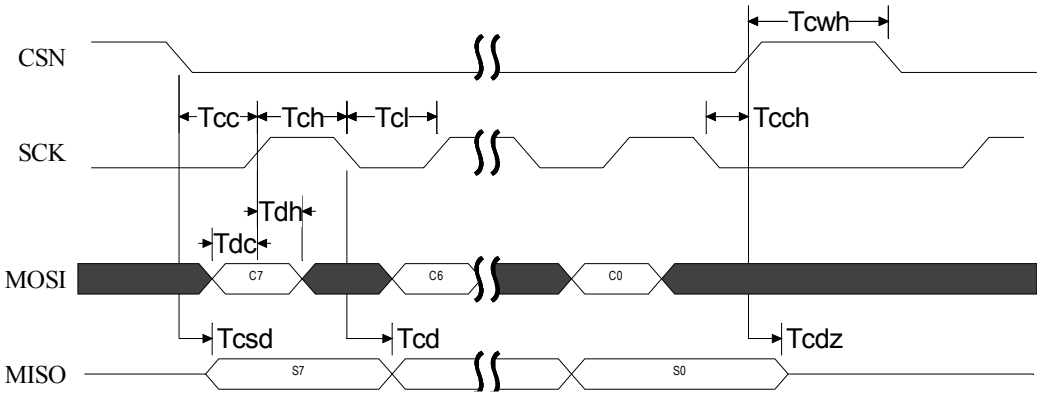


Figure 8. SPI NOP timing diagram.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Data to SCK Setup	Tdc	5		ns
SCK to Data Hold	Tdh	5		ns
CSN to Data Valid	Tcsd		45	ns
SCK to Data Valid	Tcd		45	ns
SCK Low Time	Tcl	40		ns
SCK High Time	Tch	40		ns
SCK Frequency	Tsck	DC	10	MHz
SCK Rise and Fall	Tr,Tf		100	ns
CSN to SCK Setup	Tcc	5		ns
SCK to CSN Hold	Tcch	5		ns
CSN Inactive time	Tcwh	500		ns
CSN to Output High Z	Tcdz		45	ns

Table 14. SPI timing parameters (C_{load} = 10pF)

9.4 RF – Configuration Register Description

Parameter	Bitwidth	Description
CH_NO	9	Sets center frequency together with HFREQ_PLL (default = $001101100_b = 108_d$). f_{RF} = (422.4 + CH_NO_d /10)*(1+$HFREQ\_PLL_d$) MHz
HFREQ_PLL	1	Sets PLL in 433 or 868/915MHz mode (default = 0). '0' – Chip operating in 433MHz band '1' – Chip operating in 868 or 915 MHz band
PA_PWR	2	Output power (default = 00). '00' -10dBm '01' -2dBm '10' +6dBm '11' +10dBm
RX_RED_PWR	1	Reduces current in RX mode by 1.6mA. Sensitivity is reduced (default = 0). '0' – Normal operation '1' – Reduced power
AUTO_RETRAN	1	Retransmit contents in TX register if TRX_CE and TXEN are high (default = 0). '0' – No retransmission '1' – Retransmission of data packet
RX_AFW	3	RX-address width (default = 100). '001' – 1 byte RX address field width '100' – 4 byte RX address field width
TX_AFW	3	TX-address width (default = 100). '001' – 1 byte TX address field width '100' – 4 byte TX address field width
RX_PW	6	RX-payload width (default = 100000). '000001' – 1 byte RX payload field width '000010' – 2 byte RX payload field width . '100000' – 32 byte RX payload field width
TX_PW	6	TX-payload width (default = 100000). '000001' – 1 byte TX payload field width '000010' – 2 byte TX payload field width . '100000' – 32 byte TX payload field width
RX_ADDRESS	32	RX address identity. Used bytes depend on RX_AFW (default = $E7E7E7E7_h$).
UP_CLK_FREQ	2	Output clock frequency (default = 11). '00' – 4MHz '01' – 2MHz '10' – 1MHz '11' – 500kHz
UP_CLK_EN	1	Output clock enable (default = 1). '0' – No external clock signal available '1' – External clock signal enabled

Parameter	Bitwidth	Description
XOF	3	Crystal oscillator frequency. Must be set according to external crystal resonant frequency (default = 100). '000' – 4MHz '001' – 8MHz '010' – 12MHz '011' – 16MHz '100' – 20MHz
CRC_EN	1	CRC – check enable (default = 1). '0' – Disable '1' – Enable
CRC_ MODE	1	CRC – mode (default = 1). '0' – 8 CRC check bit '1' – 16 CRC check bit

Table 15. Configuration register description

9.5 Register Contents

RF-CONFIG_REGISTER (R/W)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	CH_NO[7:0]	0110_1100
1	bit[7:6] not used, AUTO_RETRAN, RX_RED_PWR, PA_PWR[1:0], HFREQ_PLL, CH_NO[8]	0000_0000
2	bit[7] not used, TX_AFW[2:0] , bit[3] not used, RX_AFW[2:0]	0100_0100
3	bit[7:6] not used, RX_PW[5:0]	0010_0000
4	bit[7:6] not used, TX_PW[5:0]	0010_0000
5	RX_ADDRESS (device identity) byte 0	E7
6	RX_ADDRESS (device identity) byte 1	E7
7	RX_ADDRESS (device identity) byte 2	E7
8	RX_ADDRESS (device identity) byte 3	E7
9	CRC_MODE,CRC_EN, XOF[2:0], UP_CLK_EN, UP_CLK_FREQ[1:0]	1110_0111

Table 16. RF config register

TX_PAYLOAD (R/W)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	TX_PAYLOAD[7:0]	X
1	TX_PAYLOAD[15:8]	X
-	-	X
-	-	X
30	TX_PAYLOAD[247:240]	X
31	TX_PAYLOAD[255:248]	X

Table 17. TX payload register

TX_ADDRESS (R/W)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	TX_ADDRESS[7:0]	E7
1	TX_ADDRESS[15:8]	E7
2	TX_ADDRESS[23:16]	E7
3	TX_ADDRESS[31:24]	E7

Table 18.TX address register

RX_PAYLOAD (R)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	RX_PAYLOAD[7:0]	X
1	RX_PAYLOAD[15:8]	X
	-	X
	-	X
30	RX_PAYLOAD[247:240]	X
31	RX_PAYLOAD[255:248]	X

Table 19. RX payload register

STATUS_REGISTER (R)		
Byte #	**Content bit[7:0], MSB = bit[7]**	**Init value**
0	AM, bit [6] not used, DR, bit [0:4] not used	X

Table 20. Status register

The length of all registers is fixed. However, the bytes in TX_PAYLOAD, RX_PAYLOAD, TX_ADDRESS and RX_ADDRESS used in ShockBurst™ RX/TX are set in the configuration register. Register content is not lost when the device enters one of the power saving modes.

10 Important Timing Data

The following timing must be obeyed during nRF905 operation.

10.1 Device Switching Times

nRF905 timing	Max.
PWR_DWN ➔ ST_BY mode	3 ms
STBY ➔ TX ShockBurst™	650 µs
STBY ➔ RX ShockBurst™	650 µs
RX ShockBurst™ ➔ TX ShockBurst™	550 µs[a]
TX ShockBurst™ ➔ RX ShockBurst™	550 µs

a. RX to TX or TX to RX switching is available without re-programming the RF configuration register. The same frequency channel is maintained.

Table 21. Switching times for nRF905.

10.2 ShockBurst™ TX timing

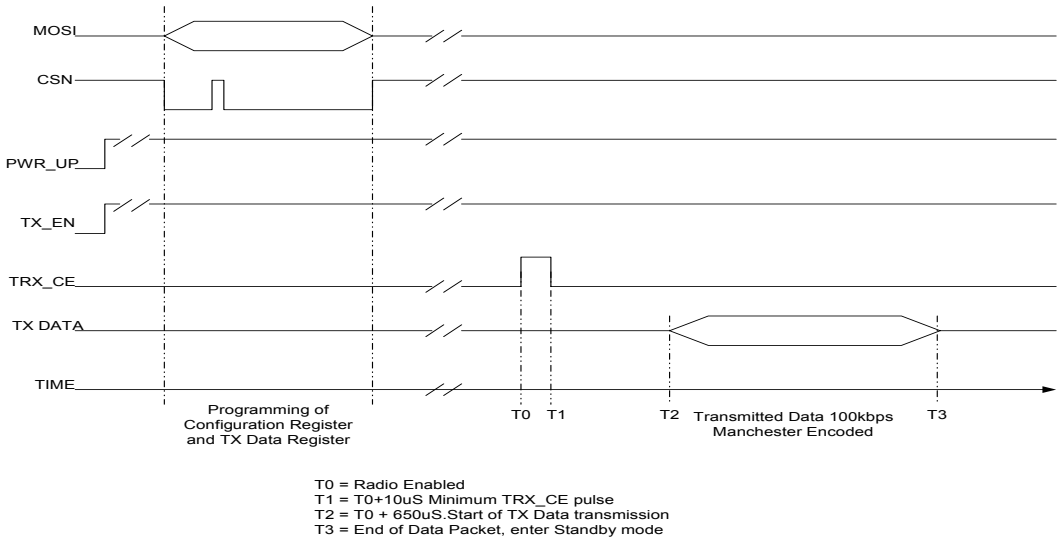


Figure 9. Timing diagram for standby to transmit

After a data packet has finished transmitting, the device automatically enters Standby mode and waits for the next pulse of TRX_CE. If the auto retransmit function is enabled the data packet continues resending the same data packet until TRX_CE is set low.

10.3 ShockBurst™ RX timing

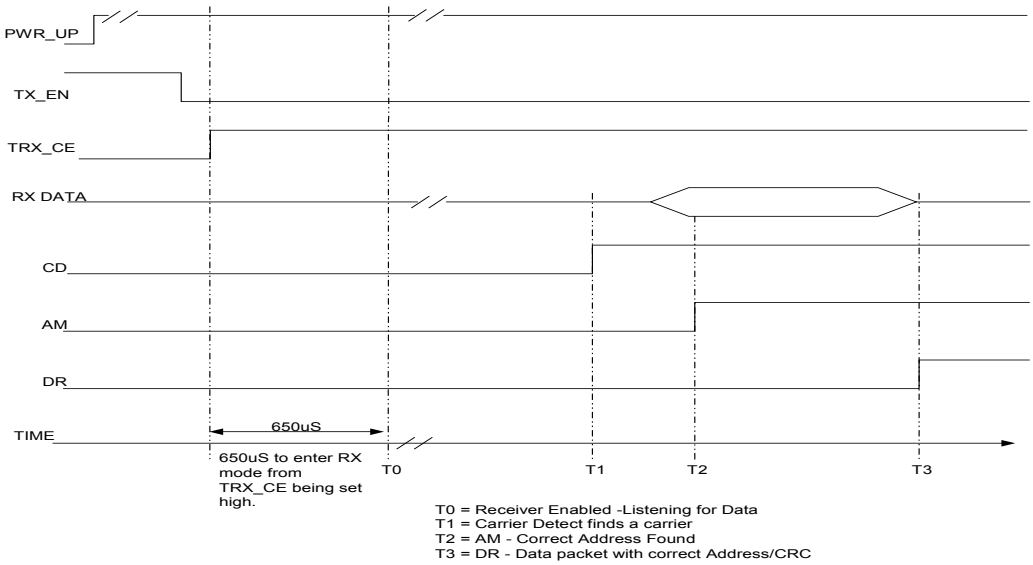


Figure 10. Timing diagram for standby to receiving

After the Data Ready (DR) has been set high a valid data packet is available in the RX data register. This may be clocked out in RX mode or standby mode. After the data has been clocked out through the SPI the Data Ready (DR) and Address Match (AM) pins are reset to low.

The RX register is reset if the PWR_UP pin is taken low or if the device is switched into TX mode, that is, TXEN is taken high. This also results in the Data Ready (DR) and Address Match (AM) pins being reset to low.

10.4 Preamble

In each data packet transmitted by the nRF905 a preamble is added automatically. The preamble is a pre-defined bit sequence used to adjust the receiver for optimal performance. A ten bit sequence is used as preamble in nRF905. The length of the preamble, $t_{preamble}$, is then 200µs.

10.5 Time On Air

The time on air is the sum of the radio start up time and the data packet length. The length of the preamble, address field, payload and CRC checksum give the data packet length while the radio start up time is given in Table 11. While preamble length and start up time are fixed the user sets the other parameters in the RF configuration register. The below equation shows how to calculate TOA:

$$TOA = t_{startup} + t_{preamble} + \frac{N_{address} + N_{payload} + N_{CRC}}{BR}$$

$t_{startup}$ and $t_{preamble}$ are RF start up time and preamble time respectively. $N_{address}$, $N_{payload}$ and N_{CRC} are numbers of bits in the address, payload and CRC checksum while BR is the bitrate, which is equal to 50kbps.

11 Peripheral RF Information

11.1 Crystal Specification

Tolerance includes initial accuracy and tolerance over temperature and aging.

Frequency	C_L	ESR	C_{0max}	Tolerance @ 868/915 MHz	Tolerance @ 433 MHz
4MHz	8pF – 16pF	150Ω	7.0pF	±30ppm	±60ppm
8MHz	8pF – 16pF	100Ω	7.0pF	±30ppm	±60ppm
12MHz	8pF – 16pF	100Ω	7.0pF	±30ppm	±60ppm
16MHz	8pF – 16pF	100Ω	7.0pF	±30ppm	±60ppm
20MHz	8pF – 16pF	100Ω	7.0pF	±30ppm	±60ppm

Table 22. Crystal specification of nRF905

To achieve a crystal oscillator solution with low power consumption and fast start up time, it is recommended to specify the crystal with a low value of crystal load capacitance. Specifying a lower value of crystal parallel equivalent capacitance, Co=1.5pF is also good, but this can increase the price of the crystal itself. Typically Co=1.5pF at a crystal specified for Co_max=7.0pF.

The crystal load capacitance, C_L, is given by:

$$C_L = \frac{C_1' \cdot C_2'}{C_1' + C_2'}, \quad where\ C_1' = C_1 + C_{PCB1} + C_{I1}\ and\ C_2' = C_2 + C_{PCB2} + C_{I2}$$

C_1 and C_2 are 0603 SMD capacitors as shown in the application schematics. C_{PCB1} and C_{PCB2} are the layout parasitic on the circuit board. C_{I1} and C_{I2} are the capacitance seen into the XC1 and XC2 pin respectively; the value is typical 1pF.

11.2 External Clock Reference

An external reference clock, such as an MCU clock, may be used instead of a crystal. The clock signal should be applied directly to the XC1 pin, the XC2 pin can be left high impedance. When operating with an external clock instead of a crystal the clock must be applied in standby mode to achieve low current consumption. If the device is set into standby mode with no external clock or crystal then the current consumption increases up to a maximum of 1mA.

11.3 Microprocessor Output Clock

By default a microprocessor clock output is provided. Providing an output clock increases the current consumption in standby mode. The current consumption in standby depends on frequency and load of external crystal, frequency of output clock and capacitive load of the provided output clock. Typical current consumption values are found in Table 9. on page 13.

11.4 Antenna Output

The ANT1 and ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD_PA, either through a RF choke or through the center point in a dipole antenna. The load impedance seen between the ANT1/ANT2 outputs should be in the range 200-700W. The optimum differential load impedance at the antenna ports is given as:

900MHz225Ω+j210

430MHz300Ω+j100

A low load impedance (for instance 50Ω) can be obtained by fitting a simple matching network or a RF transformer (balun). Further information regarding balun structures and matching networks may be found in chapter 15 on page 35.

11.5 Output Power Adjustment

The power amplifier in nRF905 can be programmed to four different output power settings by the configuration register. By reducing output power, the total TX current is reduced.

Power setting	RF output power	DC current consumption
00	-10 dBm	9.0 mA
01	-2 dBm	14.0 mA
10	6 dBm	20.0 mA
11	10 dBm	30.0 mA
Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load impedance = 400 Ω.		

Table 23. RF output power setting for the nRF905

11.6 Modulation

The modulation of nRF905 is Gaussian Frequency Shift Keying (GFSK) with a data rate of 100kbps. Deviation is ±50kHz. GFSK modulation results in a more bandwidth effective transmission link compared with ordinary FSK modulation.

The data is internally Manchester encoded (TX) and Manchester decoded (RX). That is, the effective symbol rate of the link is 50kbps. By using internally Manchester encoding, no scrambling in the microcontroller is needed.

11.7 Output Frequency

The operating RF frequency of nRF905 is set in the configuration register by CH_NO and HFREQ_PLL. The operating frequency is given by:

$$f_{OP} = (422.4 + (CH\_NO/10)) \cdot (1 + HFREQ\_PLL)\ MHz$$

When HFREQ_PLL is ‘0’ the frequency resolution is 100kHz and when it is ‘1’ the resolution is 200kHz.

The application operating frequency must be chosen to apply with the Short Range Device regulation in the area of operation.

Operating frequency	HFREQ_PLL	CH_NO
430.0 MHz	[0]	[001001100]
433.1 MHz	[0]	[001101011]
433.2 MHz	[0]	[001101100]
434.7 MHz	[0]	[001111011]
862.0 MHz	[1]	[001010110]
868.2 MHz	[1]	[001110101]
868.4 MHz	[1]	[001110110]
869.8 MHz	[1]	[001111101]
902.2 MHz	[1]	[100011111]
902.4 MHz	[1]	[100100000]
927.8 MHz	[1]	[110011111]

Table 24. Examples of real operating frequencies

11.8 PCB Layout and Decoupling Guidelines

nRF905 is an extremely robust RF device due to internal voltage regulators and requires the minimum of RF layout protocols. However, the following design rules should still be incorporated into the layout design.

A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. It is preferable to mount a large surface mount capacitor (for example, 4.7µF tantalum) in parallel with the smaller value capacitors. The supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to place via holes as close as possible to the VSS pins. A minimum of one via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the crystal or the power supply lines.

A fully qualified RF layout for the nRF905 and its surrounding components, including antennas and matching networks, can be downloaded from www.nordicsemi.no.

12 nRF905 features

12.1 Carrier Detect

When the nRF905 is in ShockBurst™ RX, the Carrier Detect (CD) pin is set high if a RF carrier is present at the channel the device is programmed to. This feature is very effective to avoid collision of packets from different transmitters operating at the same frequency. Whenever a device is ready to transmit it could first be set into receive mode and sense whether or not the wanted channel is available for outgoing data. This forms a very simple listen before transmit protocol. Operating Carrier Detect (CD) with Reduced RX Power mode is an extremely power efficient RF system. Typical Carrier Detect level (CD) is typically 5dB lower than sensitivity, that is, if sensitivity is –100dBm then the Carrier Detect function senses a carrier wave as low as –105dBm. Below –105dBm the Carrier Detect signal is low, that is, 0V. Above –95dBm the Carrier Detect signal is high, that is, Vdd. Between approximately -95 to -105 the Carrier Detect Signal toggles.

12.2 Address Match

When the nRF905 is in ShockBurst™ RX mode, the Address Match (AM) pin is set high as soon as an incoming packet with an address that is identical with the device's own identity is received. With the Address Match pin the controller is alerted that the nRF905 is receiving data actually before the Data Ready (DR) signal is set high. If the Data Ready (DR) pin is not set high, that is, the CRC is incorrect then the Address Match (AM) pin is reset to low at the end of the received data packet. This function can be very useful for an MCU. If Address Match (AM) is high then the MCU can make a decision to wait and see if Data Ready (DR) is set high indicating a valid data packet has been received or ignore that a possible packet is being received and switch modes.

12.3 Data Ready

The Data Ready (DR) signal makes it possible to largely reduce the complexity of the MCU software program.

In ShockBurst™ TX, the Data Ready (DR) signal is set high when a complete packet is transmitted, telling the MCU that the nRF905 is ready for new actions. It is reset to low at the start of a new packet transmission or when switched to a different mode, that is, receive mode or standby mode.

In ShockBurst™ TX Auto Retransmit the Data Ready (DR) signal is set high at the beginning of the preamble and is set low at the end of the preamble. The Data Ready (DR) signal therefore pulses at the beginning of each transmitted data packet.

In ShockBurst™ RX, the signal is set high when nRF905 has received a valid packet, that is, a valid address, packet length and correct CRC. The MCU can then retrieve the payload through the SPI. The Data Ready (DR) pin is reset to low once the data has been clocked out of the data buffer or the device is switched to transmit mode.

12.4 Auto Retransmit

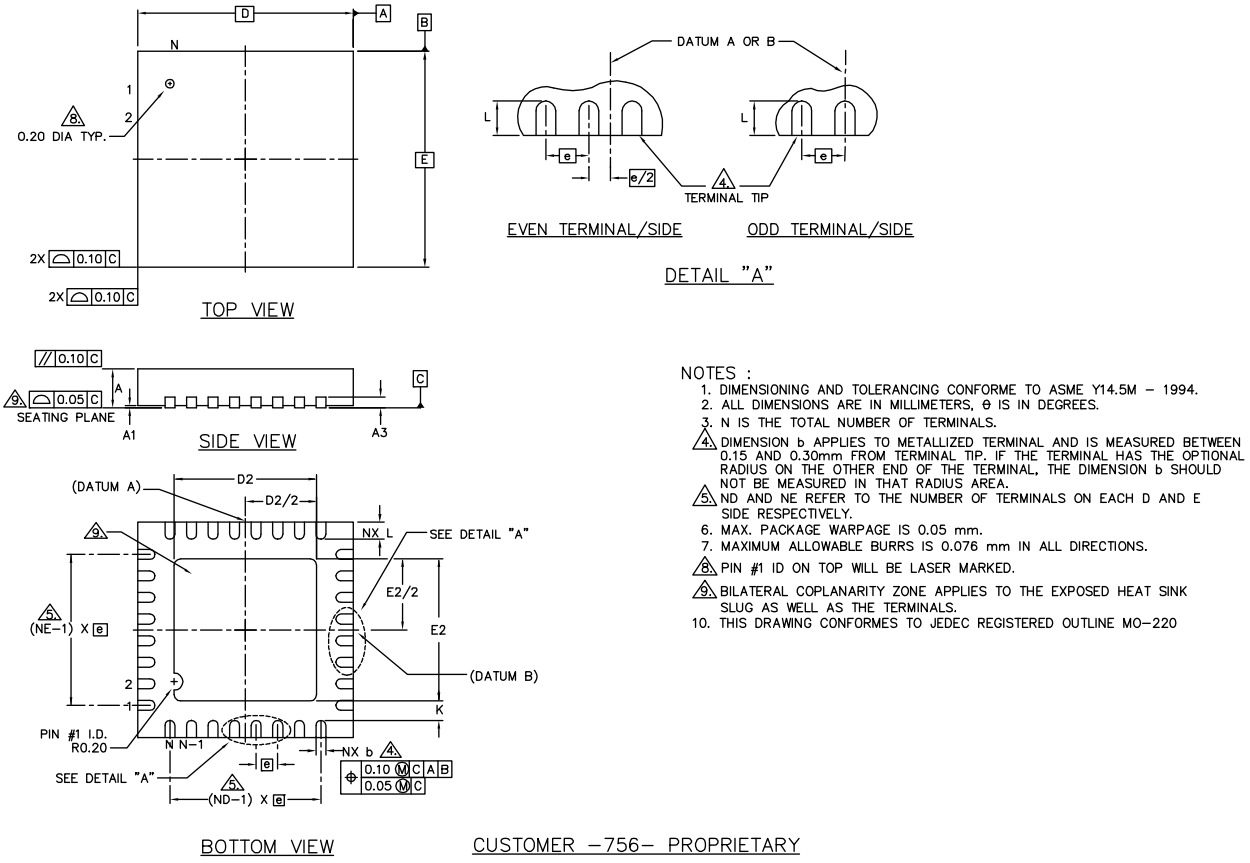
One way to increase system reliability in a noisy environment or in a system without collision control is to transmit a packet several times. This is easily accomplished with the Auto Retransmit feature in nRF905. By setting the AUTO_RETRAN bit to "1" in the configuration register, the circuit keeps sending the same data packet as long as TRX_CE and TX_EN is high. As soon as TRX_CE is set low the device finishes sending the packet it is currently transmitting and then returns to standby mode.

12.5 RX Reduced Power Mode

To maximize battery lifetime in application where the nRF905 high sensitivity is not necessary; nRF905 offers a built in reduced power mode. In this mode, the receive current consumption reduces from 12.5mA to only 10.5mA. The sensitivity is reduced to typical –85dBm, ±10dB. Some degradation of the nRF905 blocking performance should be expected in this mode. The reduced power mode is an excellent option when using Carrier Detect to sense if the wanted channel is available for outgoing data.

13 Mechanical specifications

nRF905 uses the QFN 32L 5x5 green package with a mat tin finish. Dimensions are in mm. Recommended soldering reflow profile can be found in application note nAN400-08, QFN soldering reflow guidelines, www.nordicsemi.no.



NOTES :
1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO–220

Package		A	A1	A3	b	D	E	e	J	K	L	N	ND	NE	θ
QFN32	Min.	0.8	0.0		0.18				3.2	0.2	0.35				0
(5x5 mm)	Typ.	0.85	0.02	0.2	0.23	5 BSC	5 BSC	0.5 BSC	3.3		0.4	32	8	8	
	Max.	0.9	0.05		0.3				3.4		0.45				12

Figure 11. nRF905 package outline

14 Ordering information

14.1 Package marking

n	R	F		B	X
9	0	5			
Y	Y	W	W	L	L

14.1.1 Abbreviations

Abbreviation	Definition
905	Product number
B	Build Code, that is, unique code for production sites, package type and, test platform.
X	"X" grade, that is, Engineering Samples (optional).
YY	Two digit Year number
WW	Two digit week number
LL	Two letter wafer lot number code

Table 25. Abbreviations

14.2 Product options

14.2.1 RF silicon

Ordering code	Package	Container	MOQ[a]
nRF905	5x5mm 32-pin QFN, lead free (green)	Tray	490
nRF905-REEL	5x5mm 32-pin QFN, lead free (green)	13” reel	2500

a. Minimum Order Quantity

Table 26. nRF905 RF silicon options

14.2.2 Development tools

Type Number	Description	Version
nRF905-EVKIT 433	nRF905 Development kit 433MHz	1.0
nRF905-EVKIT 868/915	nRF905 Development kit 868/915MHz	1.0

Table 27. nRF905 solution options

15 Application Examples

15.1 Differential Connection to a Loop Antenna

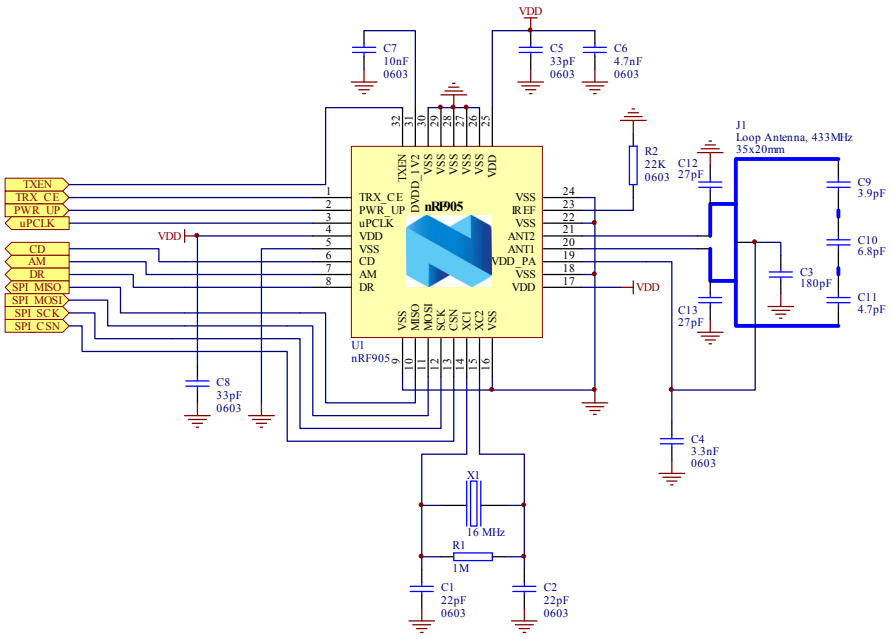


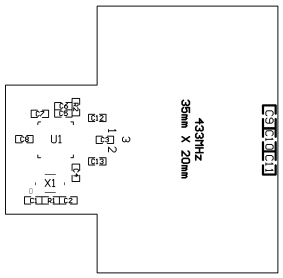
Figure 12. nRF905 Application schematic, differential connection to a loop antenna (433MHz)

Component	Description	Size	Value	Tol.	Units
C1	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C2	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C3	NP0 ceramic chip capacitor, (PA supply decoupling)	0603	180	±5%	pF
C4	X7R ceramic chip capacitor, (PA supply decoupling)	0603	3.3	±10%	nF
C5	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C7	X7R ceramic chip capacitor, (Supply decoupling)	0603	10	±10%	nF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C9	NP0 ceramic chip capacitor, (Antenna tuning)	0603	3.9	±0.1	pF
C10	NP0 ceramic chip capacitor, (Antenna tuning)	0603	6.8	±0.1	pF
C11	NP0 ceramic chip capacitor, (Antenna tuning)	0603	4.7	±0.1	pF
C12	NP0 ceramic chip capacitor, (Antenna tuning)	0603	27	±5%	pF
C13	NP0 ceramic chip capacitor, (Antenna tuning)	0603	27	±5%	pF
R1	0.1W chip resistor, (Crystal oscillator bias)	0603	1	±5%	MΩ
R2	0.1W chip resistor, (Reference bias)	0603	22	±1%	kΩ
U1	nRF905 Transceiver	QFN32L/5x5			
X1	Crystal, C_L = 12pF	LxWxH = 4.0x2.5x0.8	16	±60ppm	MHz

Table 28. Recommended external components, differential connection to a loop antenna (433MHz)

15.2 PCB Layout Example; Differential Connection to a Loop Antenna

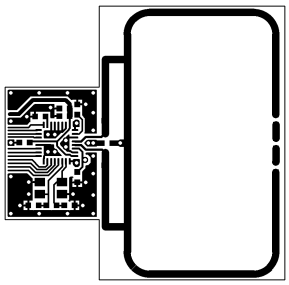
Figure 13. shows a PCB layout example for the application schematic in Figure 12. A double sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane. There is no ground plane beneath the antenna.



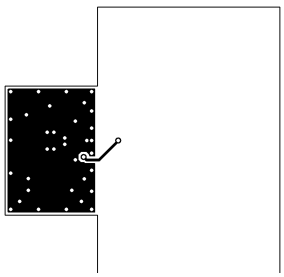
a) Top silk screen

No components in bottom layer

b) Bottom silk screen



c) Top view



d) Bottom view

Figure 13. PCB layout example for nRF905, differential connection to a loop antenna

A fully qualified RF layout for the nRF905 and its surrounding components, including antennas and matching networks, can be downloaded from www.nordicsemi.no.

15.3 Single ended connection to 50Ω antenna

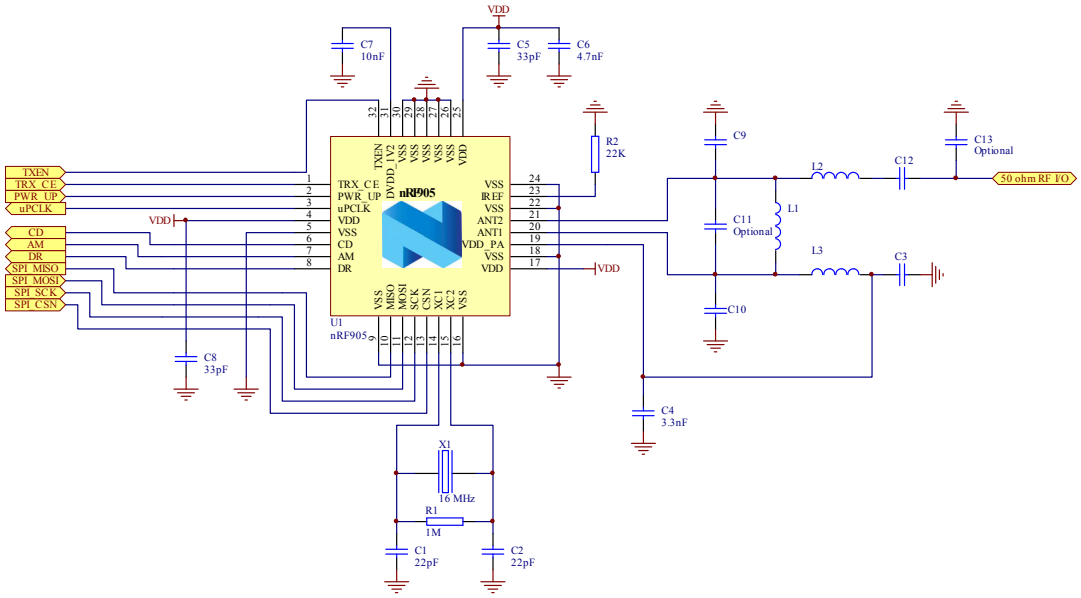


Figure 14. 433 MHz operating nRF905 application schematic, single ended connection to 50Ω antenna by using a differential to single ended matching network

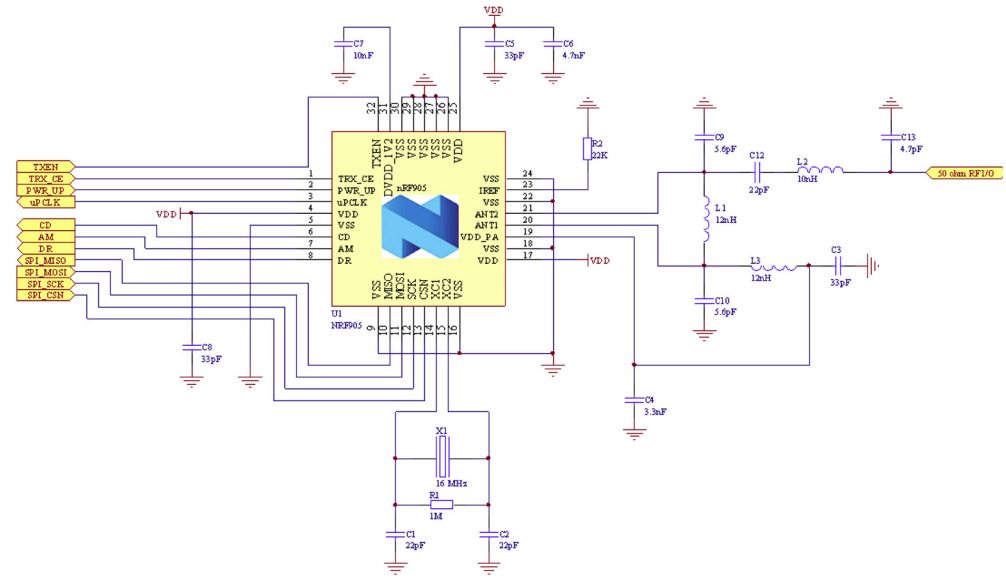


Figure 15. 868-915 MHz operating nRF905 application schematic, single ended connection to 50Ω antenna by using a differntial to single ended matching network

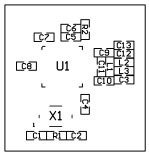
Component	Description	Size	Value	Tol.	Units
C1	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C2	NP0 ceramic chip capacitor, (Crystal oscillator)	0603	22	±5%	pF
C3	NP0 ceramic chip capacitor, (PA supply decoupling) @ 433MHz @ 868MHz @ 915MHz	0603	 180 33 33	±5%	pF
C4	X7R ceramic chip capacitor, (PA supply decoupling)	0603	3.3	±10%	nF
C5	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C7	X7R ceramic chip capacitor, (Supply decoupling)	0603	10	±10%	nF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C9	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868MHz @ 915MHz	0603	 18 5.6 5.6	 ±5% <±0.25pF <±0.25pF	pF
C10	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868MHz @ 915MHz	0603	 18 5.6 5.6	 ±5% <±0.25pF <±0.25pF	pF
C11	NP0 ceramic chip capacitor, (Impedance matching)	0603	Not fitted		pF
C12	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868MHz @ 915MHz	0603	 6.8 22 22	 ±5% ±5% ±5%	pF
C13	NP0 ceramic chip capacitor, (Impedance matching) @ 433MHz @ 868MHz @ 915MHz	0603	 Not fitted 4.7 4.7		pF
L1	Chip inductor, (Impedance matching) @ 433MHz: SRF> 433MHz @ 868MHz: SRF> 868MHz @ 915MHz: SRF> 915MHz	0603	 12 12 12	±5%	nH
L2	Chip inductor, (Impedance matching) @ 433MHz: SRF> 433MHz @ 868MHz: SRF> 868MHz @ 915MHz: SRF> 915MHz	0603	 39 10 10	 ±5% ±5% ±5%	nH

Component	Description	Size	Value	Tol.	Units
L3	Chip inductor, (Impedance matching) @ 433MHz: SRF> 433MHz @ 868MHz: SRF> 868MHz @ 915MHz: SRF> 915MHz	0603	 39 12 12	 ±5% ±5% ±5%	nH
R1	0.1W chip resistor, (Crystal oscillator bias)	0603	1	±5%	MΩ
R2	0.1W chip resistor, (Reference bias)	0603	22	±1%	kΩ
U1	nRF905 Transceiver	QFN32L/5x5			
X1	Crystal, C_L = 12pF @ 433MHz @ 868MHz @ 915MHz	LxWxH = 4.0x2.5x0.8	16	 ±60ppm ±30ppm ±30ppm	MHz

Table 29. Recommended external components, single ended connection to 50Ω antenna

15.4 PCB Layout Example; Single Ended Connection to 50Ω Antenna

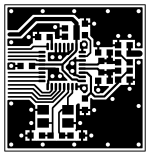
Figure 16. shows a PCB layout example for the application schematic in Figure 14. and Figure 17. shows a PCB layout example for the application schematic in Figure 15. A double sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.

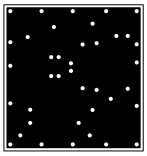


No components in bottom layer

a) Top silk screen

b) Bottom silk screen

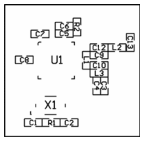




c) Top view

d) Bottom view

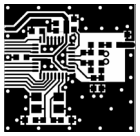
Figure 16. PCB layout example for 433 MHz operation on nRF905, single ended connection to 50Ω antenna by using a differential to single ended matching network

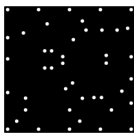


No components in bottom layer

b) Bottom silk screen

a) Top silk screen





c) Top view

d) Bottom view

Figure 17. PCB layout example for 868-915 MHz operation on nRF905, single ended connection to 50Ω antenna by using a differential to single ended matching network

A fully qualified RF layout for the nRF905 and its surrounding components, including antennas and matching networks, can be downloaded from www.nordicsemi.no

16 Glossary of terms

Term	Description
ADC	Analog to Digital Converter
AM	Address Match
CD	Carrier Detect
CLK	Clock
CRC	Cyclic Redundancy Check
DR	Data Ready
GFSK	Gaussian Frequency Shift Keying
ISM	Industrial-Scientific-Medical
kSPS	kilo Samples per Second
MCU	Micro Controller Unit
PWR_DWN	Power Down
PWR_UP	Power Up
RX	Receive
SPI	Serial Programmable Interface
CSN	SPI Chip Select Not
MISO	SPI Master In Slave Out
MOSI	SPI Master Out Slave In
SCK	SPI Serial Clock
SPS	Samples per Second
STBY	Standby
TRX_EN	Transmit/Receive Enable
TX	Transmit
TX_EN	Transmit Enable

Table 30. Glossary of terms.