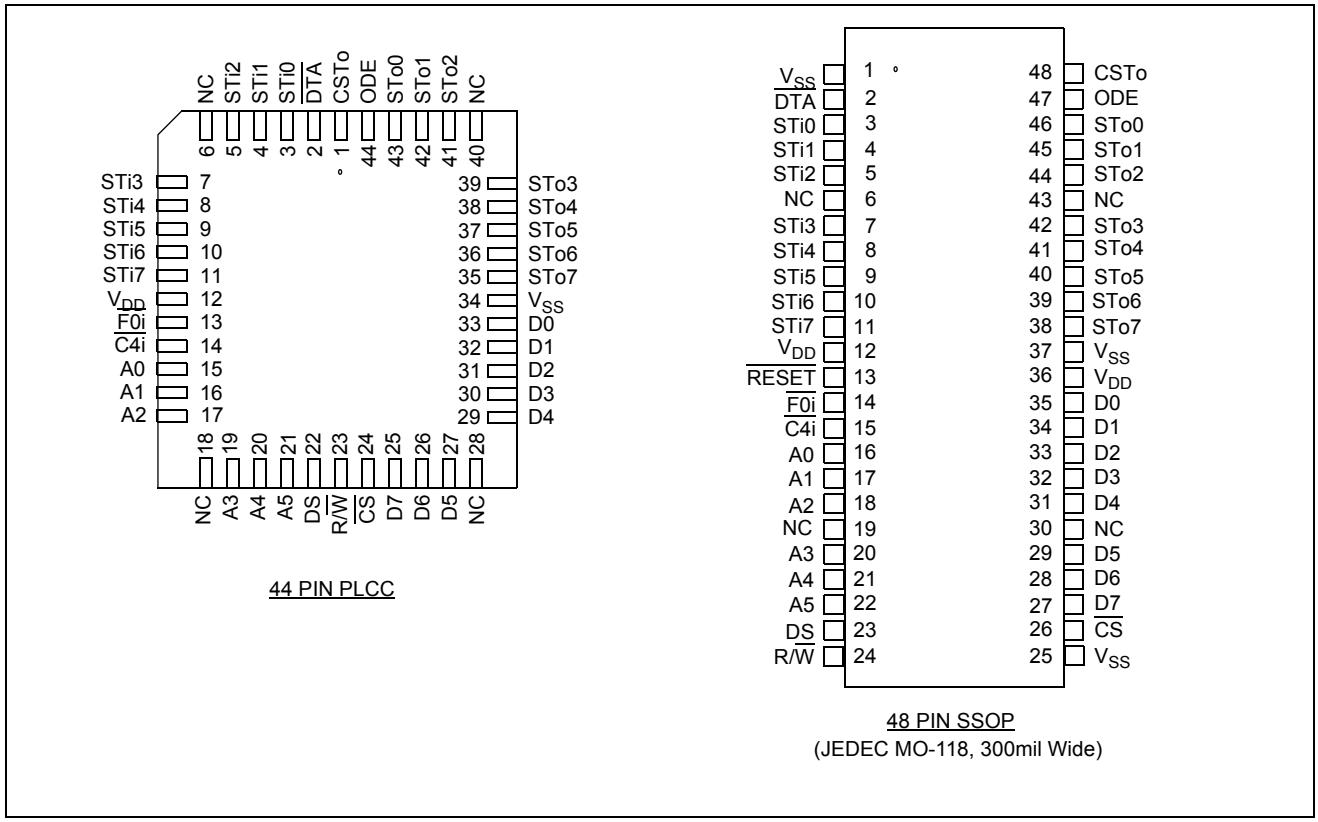


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
44 PLCC	**48 SSOP**		
2	2	**$\overline{\text{DTA}}$**	**Data Acknowledgment** (5 V Tolerant Three-state Output)**.** This active low output indicates that a data bus transfer is complete. A pull-up resistor is required at this output.
3-5	3-5	**STi0-2**	**ST-BUS Inputs 0 to 2** (5 V-tolerant Inputs). Serial data input streams. These streams have data rates of 2.048 Mbit/s with 32 channels.
7-11	7-11	**STi3-7**	**ST-BUS Inputs 3 to 7** (5 V-tolerant Inputs). Serial data input streams. These streams may have data rates of 2.048 Mbit/s with 32channels.
12	12,36	**V_{DD}**	**+3.3 Volt Power Supply**.
	13	**$\overline{\text{RESET}}$**	**Device Reset** (5 V-tolerant input). This pin is only available for the 48-pin SSOP package.This active low input puts the device in its reset state. It clears the internal counters and registers. All ST-BUS outputs are set to the high impedance state. In normal operation. The $\overline{\text{RESET}}$ pin must be held low for a minimum of 100nsec to reset the device. Internal pull-up.
13	14	**$\overline{\text{F0i}}$**	**Frame Pulse** (5 V-tolerant Input). This is the input for the frame synchronization pulse for the 2048 kbit/s ST-BUS streams. A $\overline{\text{low}}$ on this input causes the internal counter to reset on the next negative transition of $\overline{\text{C4i}}$.

Pin Description (continued)

Pin #		Name	Description
44 PLCC	48 SSOP		
14	15	$\overline{\text{C4i}}$	**4.096 MHz Clock** (5 V-tolerant Input). ST-BUS bit cell boundaries lie on the alternate falling edges of this clock.
15-17	16-18	**A0-2**	**Address 0-2 / Input Streams 8-10** (5 V-tolerant Input). These are the inputs for the address lines on the microprocessor interface.
19-21	20-22	**A3-5**	**Address 3-5 / Input Streams 11-13** (5 V-tolerant Input). These are the inputs for the address lines on the microprocessor interface.
22	23	**DS**	**Data Strobe** (5 V-tolerant Input). This is the input for the active high data strobe on the microprocessor interface.
23	24	**R/$\overline{\text{W}}$**	**Read/Write** (5 V-tolerant Input). This is the input for the read/write signal on the microprocessor interface - high for read, low for write.
24	26	$\overline{\text{CS}}$	**Chip Select** (5 V-tolerant Input). This is the input for the active low chip select on the microprocessor interface
25-27	27-29	**D7-D5**	**Data Bus** (5 V-tolerant I/O): These are the bidirectional data pins on the microprocessor interface.
29-33	31-35	**D4-D0**	**Data Bus** (5 V-tolerant I/O): These are the bidirectional data pins on the microprocessor interface.
34	1, 25,37	$\mathbf{V_{SS}}$	**Ground**.
35-39	38-42	**STo7-3**	**ST-BUS Outputs 7 to 3** (5 V-Tolerant Three-state Outputs). These are the pins for the eight 2048 kbit/s ST-BUS output streams.
41-43	44-46	**STo2-0**	**ST-BUS Outputs 2to 0** (5 V-Tolerant Three-state Outputs). These are the pins for the eight 2048kbit/s ST-BUS output streams.
44	47	**ODE**	**Output Drive Enable** (5 V-tolerant Input). If this input is held high, the STo0-STo7 output drivers function normally. If this input is low, the STo0-STo7 output drivers go into their high impedance state. **NB:** Even when ODE is high, channels on the STo0-STo7 outputs can go high impedance under software control.
1	48	**CSTo**	**Control ST-BUS Output** (5 V-Tolerant Output). Each frame of 256 bits on this ST-BUS output contains the values of bit 1 in the 256 locations of the Connection Memory High.
6, 18, 28, 40	6, 19, 30, 43	**NC**	**No Connection**.

Functional Description

In recent years, there has been a trend in telephony towards digital switching, particularly in association with software control. Simultaneously, there has been a trend in system architectures towards distributed processing or multi-processor systems.

In accordance with these trends, Zarlink has devised the ST-BUS (Serial Telecom Bus). This bus architecture can be used both in software-controlled digital voice and data switching, and for interprocessor communications. The uses in switching and in interprocessor communications are completely integrated to allow for a simple general purpose architecture appropriate for the systems of the future.

The serial streams of the ST-BUS operate continuously at 2048 kbit/s and are arranged in 125 μs wide frames which contain 32 8-bit channels. Zarlink manufactures a number of devices which interface to the ST-BUS; a key device being the MT89L80 chip.

The MT89L80 can switch data from channels on ST-BUS inputs to channels on ST-BUS outputs, and simultaneously allows its controlling microprocessor to read channels on ST-BUS inputs or write to channels on ST-BUS outputs (Message Mode). To the microprocessor, the MT89L80 looks like a memory peripheral. The microprocessor can write to the MT89L80 to establish switched connections between input ST-BUS channels and output ST-BUS channels, or to transmit messages on output ST-BUS channels. By reading from the MT89L80, the microprocessor can receive messages from ST-BUS input channels or check which switched connections have already been established.

By integrating both switching and interprocessor communications, the MT89L80 allows systems to use distributed processing and to switch voice or data in an ST-BUS architecture.

Hardware Description

Serial data at 2048 kbit/s is received at the eight ST-BUS inputs (STi0 to STi7), and serial data is transmitted at the eight ST-BUS outputs (STo0 to STo7). Each serial input accepts 32 channels of digital data, each channel containing an 8-bit word which may represent a PCM-encoded analog/voice sample as provided by a codec (e.g., Zarlink's MT8964).

This serial input word is converted into parallel data and stored in the 256 X 8 Data Memory. Locations in the Data Memory are associated with particular channels on particular ST-BUS input streams. These locations can be read by the microprocessor which controls the chip.

Locations in the Connection Memory, which is split into high and low parts, are associated with particular ST-BUS output streams. When a channel is due to be transmitted on an ST-BUS output, the data for the channel can either be switched from an ST-BUS input or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory. This Data Memory address corresponds to the channel on the input ST-BUS stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory data is received, via the Control Interface, at D7 to D0. The Control Interface also receives address information at A5 to A0 and handles the microprocessor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. There are two parts to any address in the Data Memory or Connection Memory. The higher order bits come from the Control Register, which may be written to or read from via the Control Interface. The lower order bits come from the address lines directly.

The Control Register also allows the chip to broadcast messages on all ST-BUS outputs (i.e., to put every channel into Message Mode), or to split the memory so that reads are from the Data Memory and writes are to the Connection Memory Low. The Connection Memory High determines whether individual output channels are in Message Mode, and allows individual output channels to go into a high-impedance state, which enables arrays of MT89L80s to be constructed. It also controls the CSTo pin.

All ST-BUS timing is derived from the two signals $\overline{C4i}$ and $\overline{F0i}$.

A5	A4	A3	A2	A1	A0	Hex Address	Location
0	0	0	0	0	0	00 - 1F	Control Register *
1	0	0	0	0	0	20	Channel 0†
1	0	0	0	0	1	21	Channel 1†
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	3F	Channel 31†

* Writing to the Control Register is the only fast transaction.
† Memory and stream are specified by the contents of the Control Register.

Figure 3 - Address Memory Map

Software Control

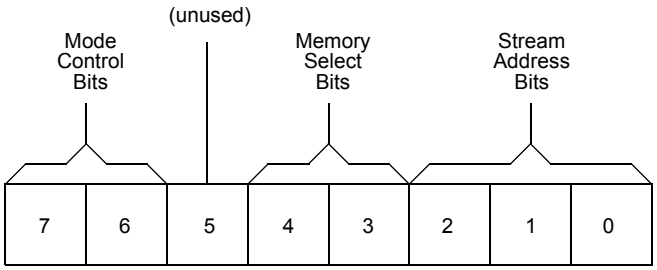
The address lines on the Control Interface give access to the Control Register directly or, depending on the contents of the Control Register, to the High or Low sections of the Connection Memory or to the Data Memory.

If address line A5 is low, then the Control Register is addressed regardless of the other address lines (see Fig. 3). If A5 is high, then the address lines A4-A0 select the memory location corresponding to channel 0-31 for the memory and stream selected in the Control Register.

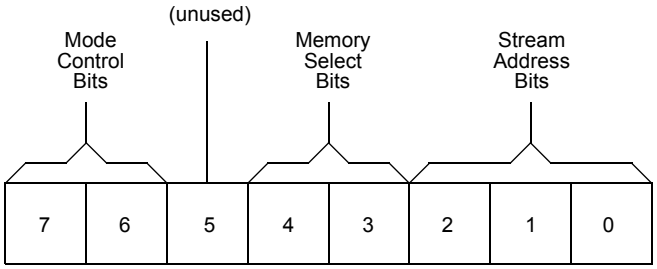
The data in the Control Register consists of mode control bits, memory select bits, and stream address bits (see Fig. 4). The memory select bits allow the Connection Memory High or Low or the Data Memory to be chosen, and the stream address bits define one of the ST-BUS input or output streams.

Bit 7 of the Control Register allows split memory operation - reads are from the Data Memory and writes are to the Connection Memory Low.

The other mode control bit, bit 6, puts every output channel on every output stream into active Message Mode; i.e., the contents of the Connection Memory Low are output on the ST-BUS output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

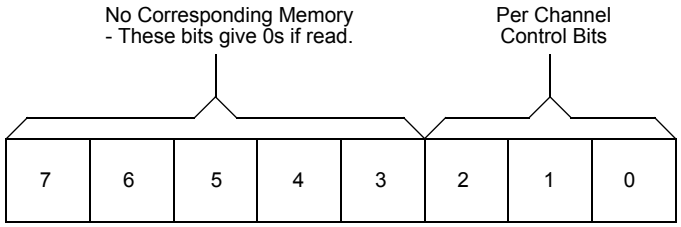


Bit	Name	Description
7	Split Memory	When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory Low, except when the Control Register is accessed again. When 0, the Memory Select bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.



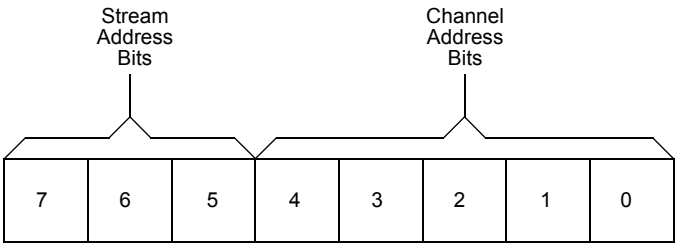
Bit	Name	Description
6	Message Mode	When 1, the contents of the Connection Memory Low are output on the Serial Output streams except when the ODE pin is low. When 0, the Connection Memory bits for each channel determine what is output.
5	(unused)	
4-3	Memory Select Bits	0-0 - Not to be used 0-1 - Data Memory (read only from the microprocessor port) 1-0 - Connection Memory Low 1-1 - Connection Memory High
2-0	Stream Address Bits	The number expressed in binary notation on these bits refers to the input or output ST-BUS stream which corresponds to the subsection of memory made accessible for subsequent operations.

Figure 4 - Control Register Bits



Bit	Name	Description
2	Message Channel	When 1, the contents of the corresponding location in Connection Memory Low are output on the location's channel and stream. When 0, the contents of the corresponding location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location's channel and stream.
1	CSTo Bit	This bit is output on the CSTo pin one channel early. The CSTo bit for stream 0 is output first.
0	Output Enable	If the ODE pin is high and bit 6 of the Control Register is 0, then this bit enables the output driver for the location's channel and stream. This allows individual channels on individual streams to be made high-impedance, allowing switching matrices to be constructed. A 1 enables the driver and a 0 disables it.

Figure 5 - Connection Memory High Bits



Bit	Name	Description
7-5*	Stream Address Bits*	The number expressed in binary notation on these 3 bits is the number of the ST-BUS stream for the source of the connection. Bit 7 is the most significant bit. e.g., if bit 7 is 1, bit 6 is 0 and bit 5 is 0, then the source of the connection is a channel on STi4.
4-0*	Channel Address Bits*	The number expressed in binary notation on these 5 bits is the number of the channel which is the source of the connection (The ST-BUS stream where the channel lies is defined by bits 7, 6 and 5.). Bit 4 is the most significant bit. e.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 1 and bit 0 is 1, then the source of the connection is channel 19.
*If bit 2 of the corresponding Connection High location is 1 or if bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwise, the bits are used as indicated to define the source of the connection which is output on the channel and stream associated with this location.		

Figure 6 - Connection Memory Low Bits

If bit 6 of the Control Register is 0, then bits 2 and 0 of each Connection Memory High location function normally (see Fig. 5). If bit 2 is 1, the associated ST-BUS output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, one of the bytes received on the serial inputs is transmitted and the contents of the Connection Memory Low define the ST-BUS input stream and channel where the byte is to be found (see Fig. 6).

If the ODE pin is low, then all serial outputs are high-impedance. If it is high and bit 6 in the Control Register is 1, then all outputs are active. If the ODE pin is high and bit 6 in the Control Register is 0, then the bit 0 in the Connection Memory High location enables the output drivers for the corresponding individual ST-BUS output stream and channel. Bit 0=1 enables the driver and bit 0=0 disables it (see Fig. 5).

Bit 1 of each Connection Memory High location (see Fig. 5) is output on the CSTo pin once every frame. To allow for delay in any external control circuitry the bit is output one channel before the corresponding channel on the ST-BUS streams, and the bit for stream 0 is output first in the channel; e.g., bit 1's for channel 9 of streams 0-7 are output synchronously with ST-BUS channel 8 bits 7-0.

Applications

Use in a Simple Digital Switching System

Figs. 7 and 8 show how MT89L80s can be used with MT8964s to form a simple digital switching system. Fig. 7 shows the interface between the MT89L80s and the filter/codecs. Fig. 8 shows the position of these components in an example architecture.

The MT8964 filter/codec in Fig. 7 receives and transmits digitized voice signals on the ST-BUS input D_R, and ST-BUS output D_X, respectively. These signals are routed to the ST-BUS inputs and outputs on the top MT89L80, which is used as a digital speech switch.

The MT8964 is controlled by the ST-BUS input D_C originating from the bottom MT89L80, which generates the appropriate signals from an output channel in Message Mode. This architecture optimizes the messaging capability

of the line circuit by building signalling logic, e.g., for on-off hook detection, which communicates on an ST-BUS output. This signalling ST-BUS output is monitored by a microprocessor (not shown) through an ST-BUS input on the bottom MT89L80.

Fig. 8 shows how a simple digital switching system may be designed using the ST-BUS architecture. This is a private telephone network with 256 extensions which uses a single MT89L80 as a speech switch and a second MT89L80 for communication with the line interface circuits.

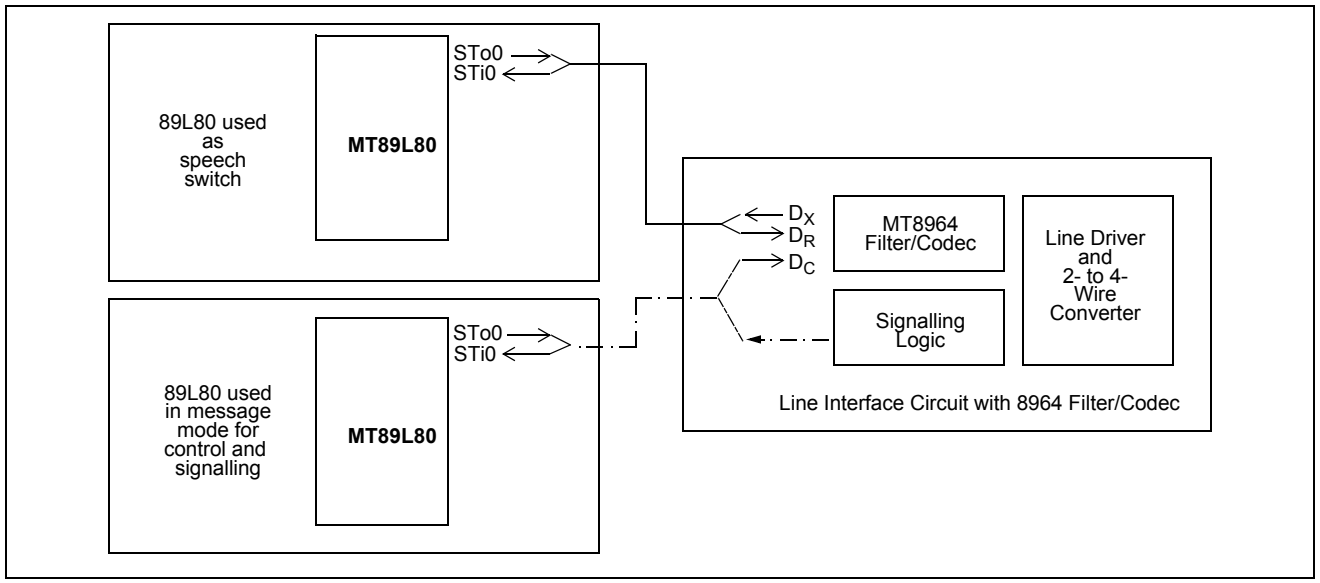


Figure 7 - Example of Typical Interface between 89L80s and 8964s for Simple Digital Switching System

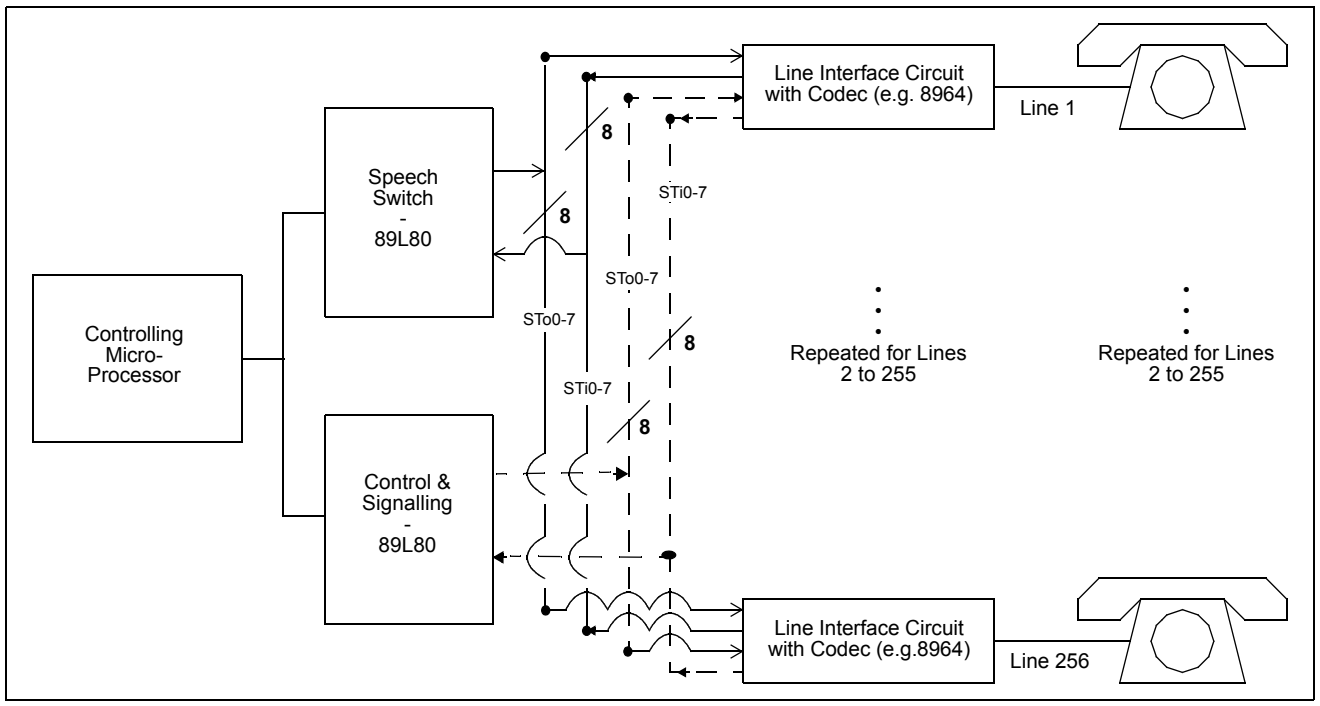


Figure 8 - Example Architecture of a Simple Digital Switching System

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage		-0.3	5.0	V
2	Voltage on any I/O pin (except supply pins)	V_O	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at Digital Outputs	I_O		20	mA
4	Storage Temperature	T_S	-55	+125	°C
5	Package Power Dissipation	P_D		1	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		+85	°C	
2	Positive Supply	V_{DD}	3.0		3.6	V	
3	Input High Voltage	V_{IH}	$0.7V_{DD}$		V_{DD}	V	
4	Input High Voltage on 5 V Tolerant Inputs	V_{IH}			5.5	V	
5	Input Low Voltage	V_{IL}	V_{SS}		$0.3V_{DD}$	V	

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	INPUTS	Supply Current	I_{DD}		4	7	mA	Outputs unloaded
2		Input High Voltage	V_{IH}	$0.7V_{DD}$			V	
3		Input Low Voltage	V_{IL}			$0.3V_{DD}$	V	
4		Input Leakage	I_{IL}			5	µA	V_I between V_{SS} and V_{DD}
5		Input Pin Capacitance	C_I			10	pF	
6	OUTPUTS	Output High Voltage	V_{OH}	$0.8V_{DD}$			V	I_{OH} = 10 mA
7		Output High Current	I_{OH}	10			mA	Sourcing. V_{OH}=2.4V
8		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
9		Output Low Current	I_{OL}	5			mA	Sinking. V_{OL} = 0.4V
10		High Impedance Leakage	I_{OZ}			5	µA	V_O between V_{SS} and V_{DD}
11		Output Pin Capacitance	C_O			10	pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics –Timing Parameter Measurement Voltage Levels

	Characteristics	Sym	Level	Units	Test Conditions
1	CMOS Threshold Voltage	V_{TT}	$0.5V_{DD}$	V	
2	CMOS Rise/Fall Threshold Voltage high	V_{HM}	$0.7V_{DD}$	V	
3	CMOS Rise/Fall Threshold Voltage low	V_{LM}	$0.3V_{DD}$	V	

AC Electrical Characteristics† - Clock Timing (Figures 9 and 10)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	INPUTS	Clock Period*	t_{CLK}	220	244	300	ns	
2		Clock Width High	t_{CH}	85	122	150	ns	
3		Clock Width Low	t_{CL}	85	122	150	ns	
4		Clock Transition Time	t_{CTT}			10	ns	
5		Frame Pulse Setup Time	t_{FPS}	10		190	ns	
6		Frame Pulse Hold Time	t_{FPH}	10		190	ns	
7		Frame Pulse Width	t_{FPW}		244		ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Contents of Connection Memory are not lost if the clock stops, however, ST-BUS outputs go into the high impedance state.
NB: Frame Pulse is repeated every 512 cycles of C4i.

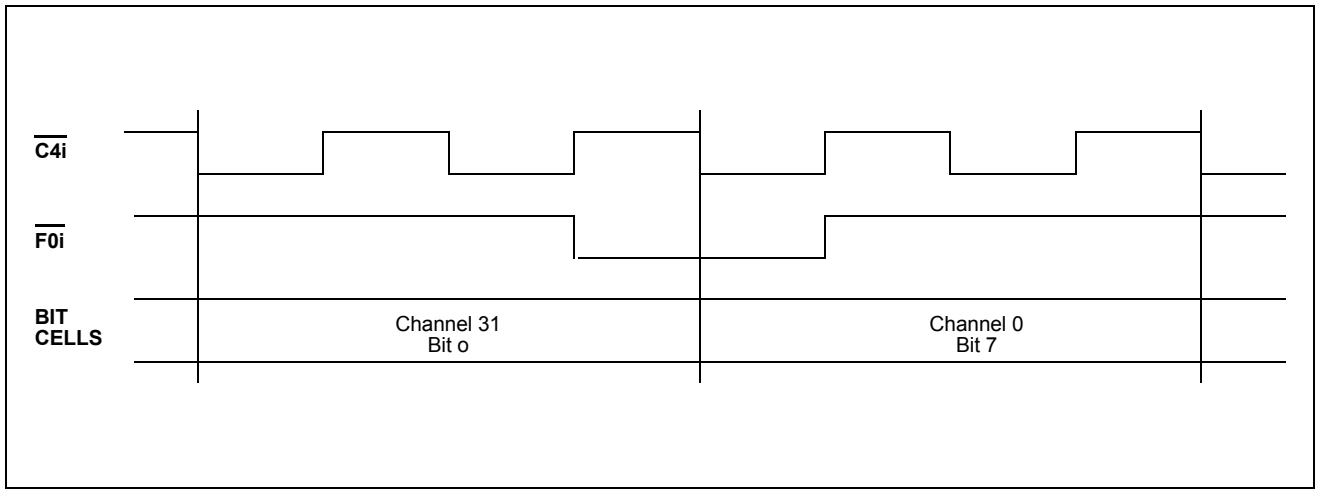


Figure 9 - Frame Alignment

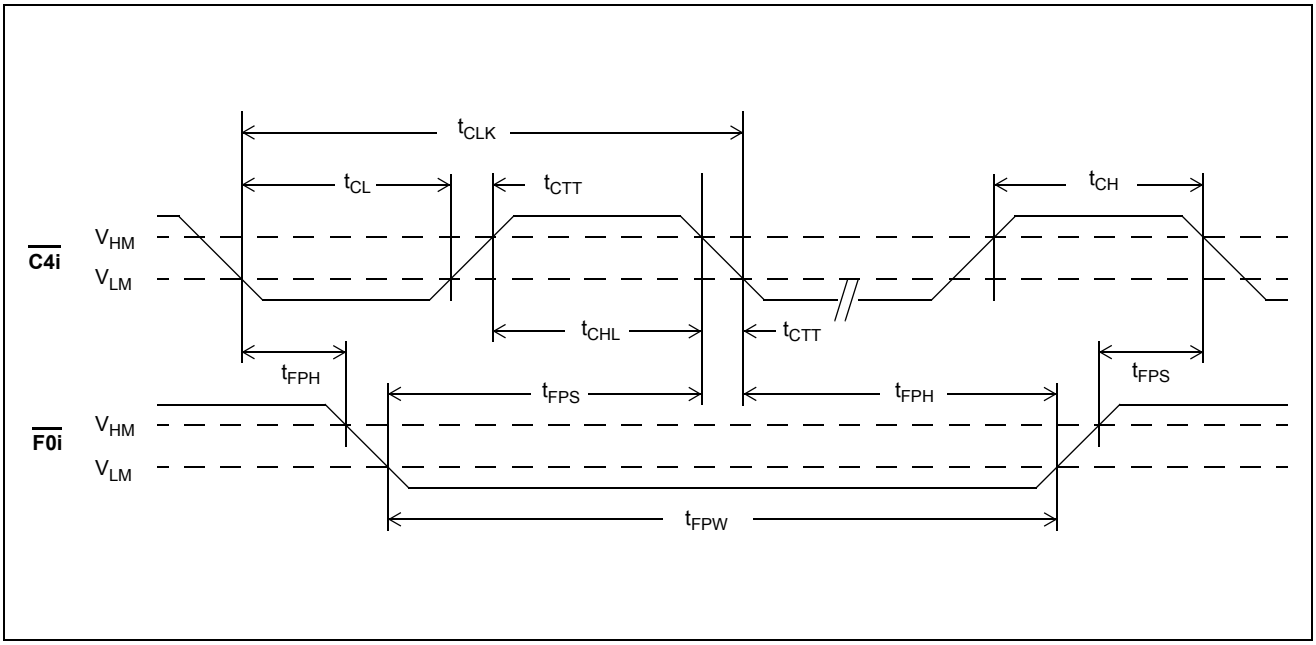


Figure 10 - Clock Timing

AC Electrical Characteristics† - Serial Streams (Figures 11, 12 and 13)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	OUTPUTS	STo0/7 Delay - Active to High Z	t_{SAZ}	5		55	ns	R_L=1 KΩ*, C_L=150 pF
2		STo0/7 Delay - High Z to Active	t_{SZA}	5		55	ns	C_L=150 pF
3		STo0/7 Delay - Active to Active	t_{SAA}	5		55	ns	C_L=150 pF
4		Output Driver Enable Delay	t_{OED}			50	ns	R_L=1 KΩ*, C_L=150 pF
5		External Control Delay	t_{XCD}			55	ns	C_L=150 pF
6	IN	Serial Input Setup Time	t_{SIS}	20			ns	
7		Serial Input Hold Time	t_{SIH}	20			ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

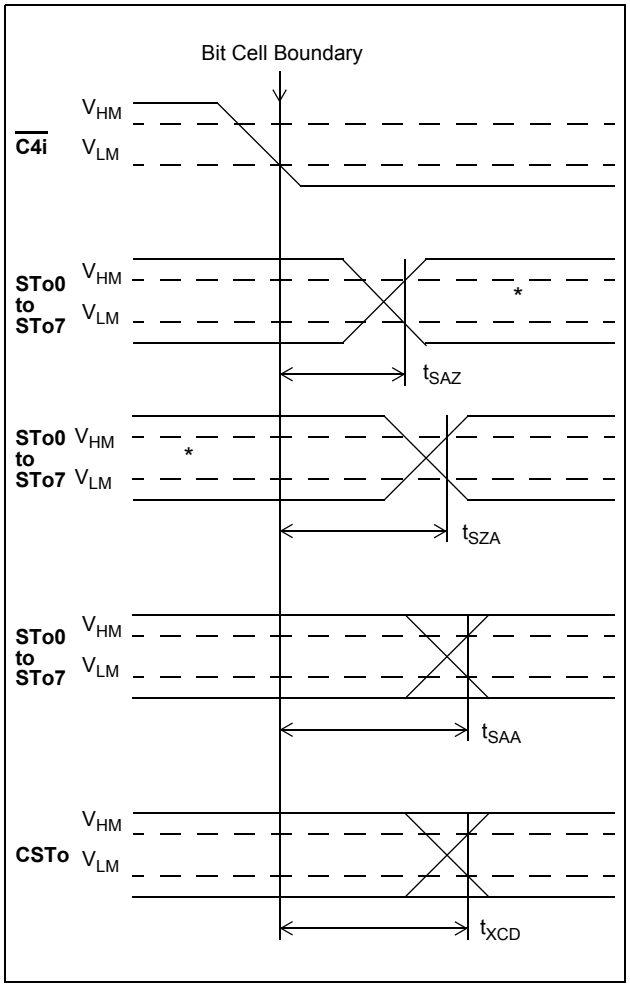


Figure 11 - Serial Outputs and External Control

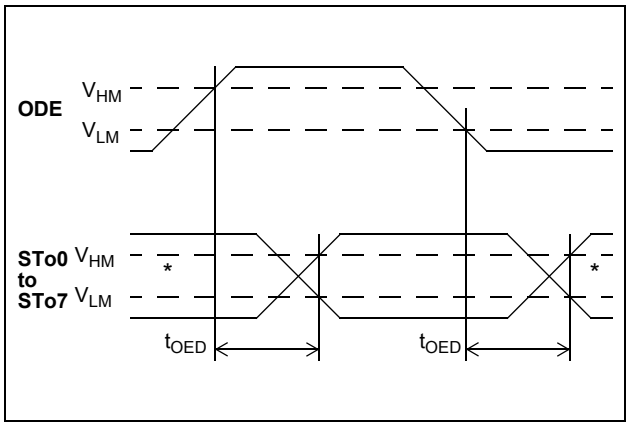


Figure 12 - Output Driver Enable

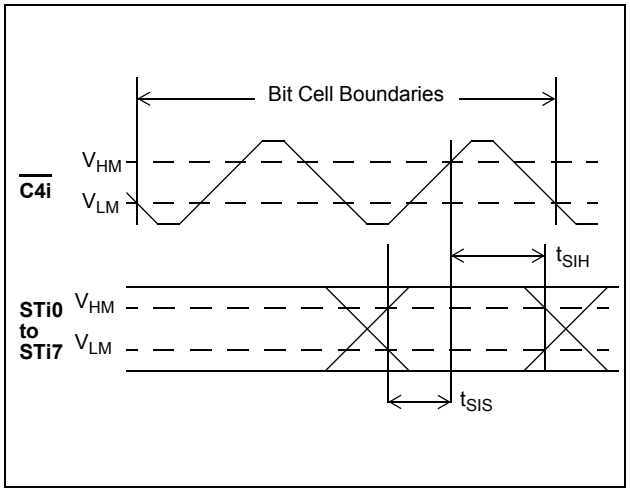


Figure 13 - Serial Inputs

AC Electrical Characteristics† - Processor Bus (Figures 14)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Chip Select Setup Time	t_{CSS}	0			ns	
2	Read/Write Setup Time	t_{RWS}	5			ns	
3	Address Setup Time	t_{ADS}	5			ns	
4	Acknowledgment Delay Control Register Read	t_{AKD}		52	120	ns	C_L=150 pF
	Control Register Write	t_{AKD}		25	65	ns	C_L=150 pF
	Connection Memory Read	t_{AKD}		62	120	ns	C_L=150 pF
	Connection Memory Write	t_{AKD}		30	53	ns	C_L=150 pF
	Data Memory Read	t_{AKD}		560	1220	ns	C_L=150 pF
5	Fast Write Data Setup Time	t_{FWS}	0			ns	
6	Slow Write Data Delay	t_{SWD}			122	ns	
7	Read Data Setup Time	t_{RDS}	0			ns	C_L= 150 pF
8	Data Hold Time Read	t_{DHT}	10		90	ns	R_L=1 KΩ*, C_L=150 pF
	Write	t_{DHT}	5	10		ns	
9	Read Data To High Impedance	t_{RDZ}	15	50	90	ns	R_L=1 KΩ*, C_L=150 pF
10	Chip Select Hold Time	t_{CSH}	0			ns	
11	Read/Write Hold Time	t_{RWH}	0			ns	
12	Address Hold Time	t_{ADH}	8			ns	
13	Acknowledgment Hold Time	t_{AKH}		50	80	ns	R_L=1 KΩ*, C_L=150 pF

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

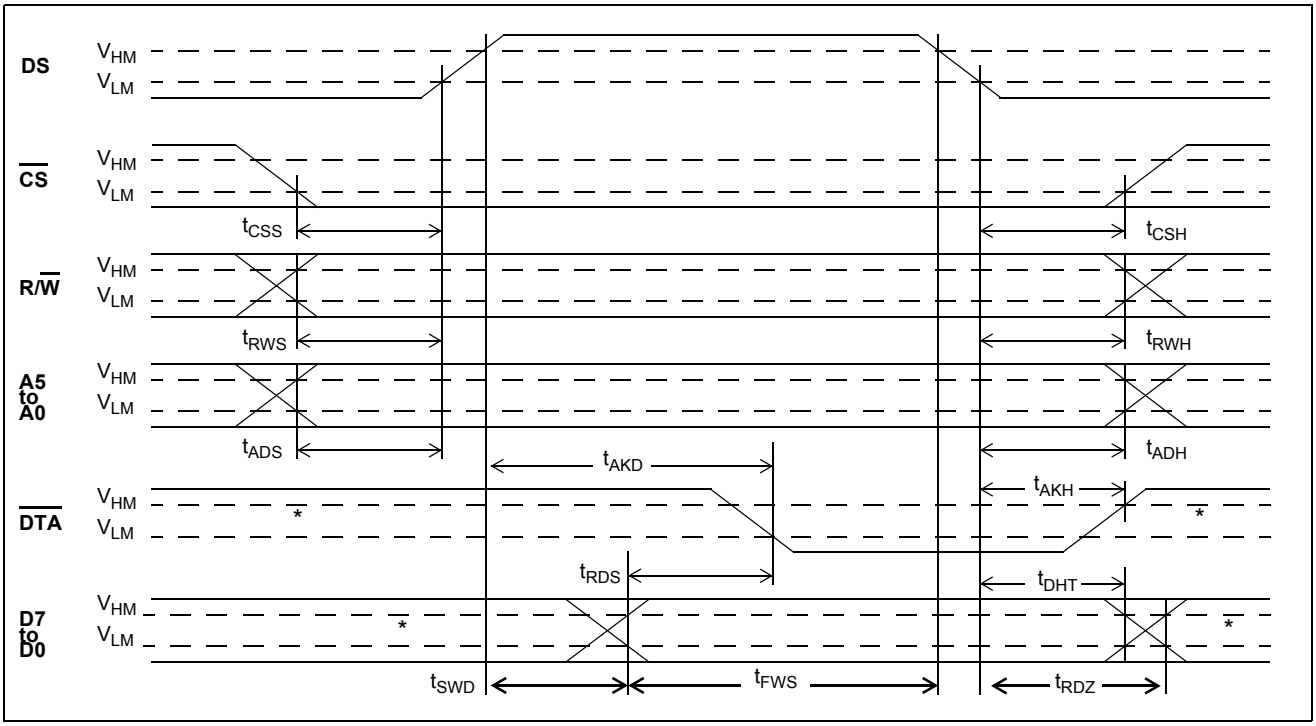
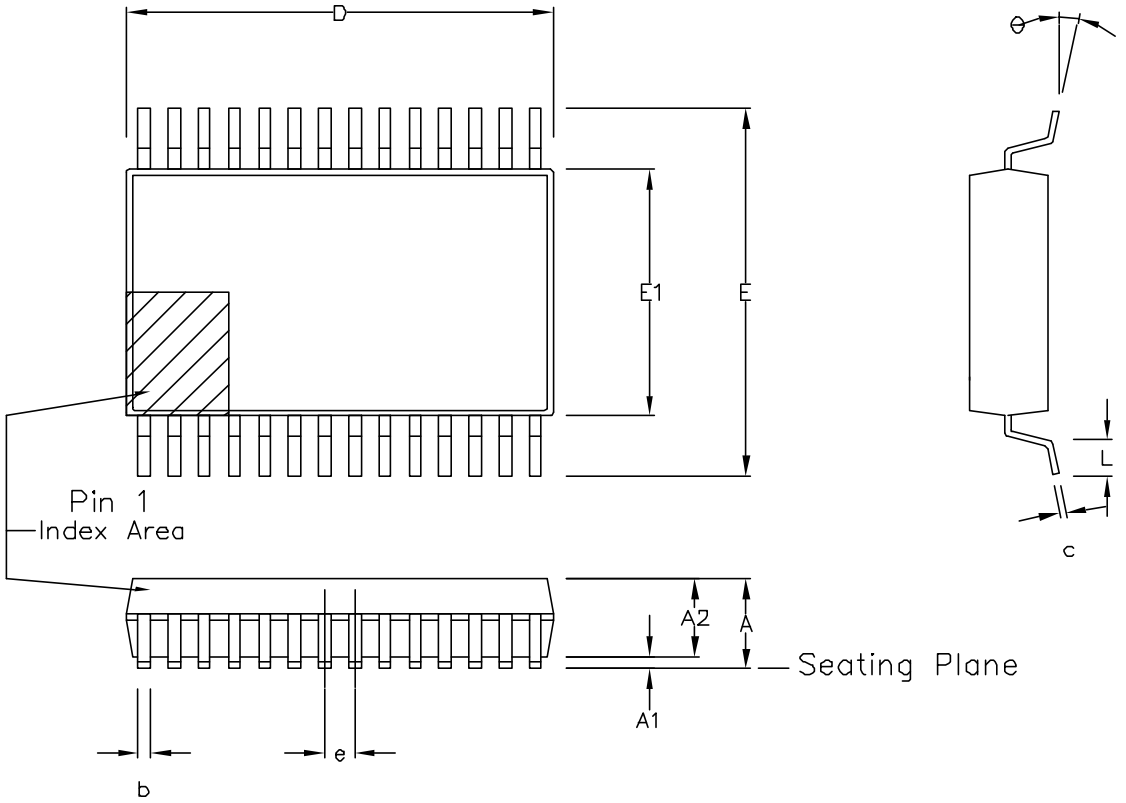


Figure 14 - Processor Bus



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.41	2.59	2.79		0.095	0.102	0.110
A1	0.20	0.30	0.40		0.008	0.012	0.016
A2	2.26	2.39	2.52		0.089	0.094	0.099
D	15.75	15.88	16.00		0.620	0.625	0.630
E	10.03	10.31	10.67		0.395	0.406	0.420
E1	7.39	7.49	7.59		0.291	0.295	0.299
L	0.51	0.76	1.02		0.020	0.030	0.040
e	0.64 BSC.				0.025 BSC.		
b	0.20	0.25	0.34		0.008	0.010	0.0135
c	0.13	0.20	0.25		0.005	0.008	0.010
θ	0°		8°		0°		8°
	Pin features						
N	48						
Conforms to JEDEC MO-118 AA Iss. A							

tes:
A visual index feature, e.g. a dot, must be located within the cross-hatched area.
Controlling dimension are in millimeters.
Dimensions D and E1 do not include mould flash or protrusion. Mould flash or protrusion shall not exceed 0.15 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.

	1			
	213915			
	13-01-03			

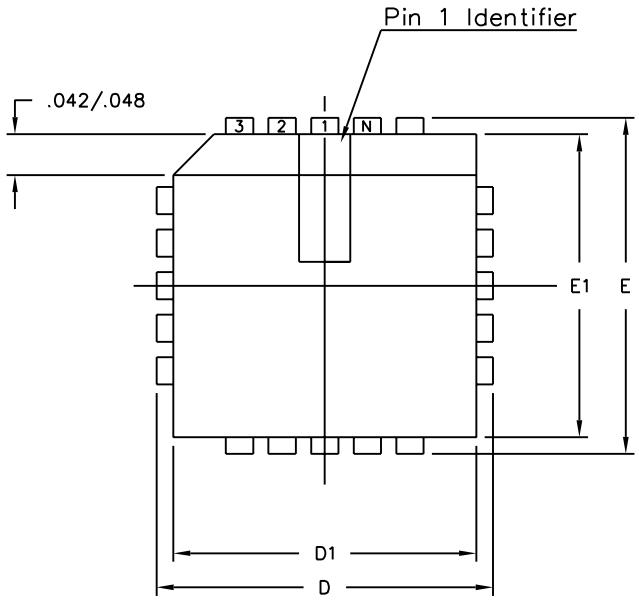
ZARLINK SEMICONDUCTOR

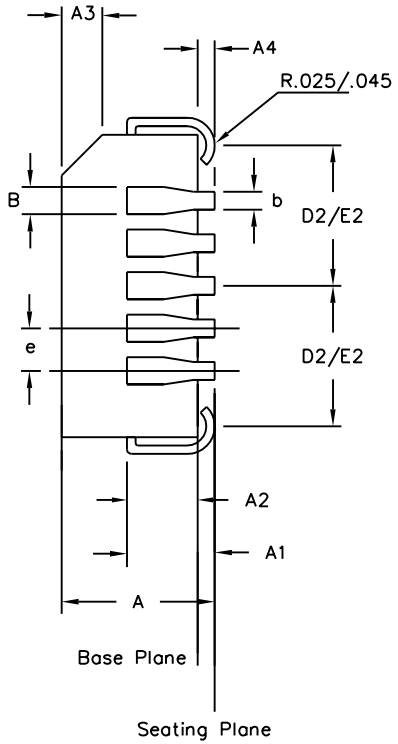
Previous package codes
NP / N

Package Code DD

Package Outline for 48 lead SSOP (300 mil Body Width)

GPD00816





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207470	213094	
DATE	15Aug94	10Sep99	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

HP / P

Package Code QA

Package Outline for 44 lead PLCC

GPD00003

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