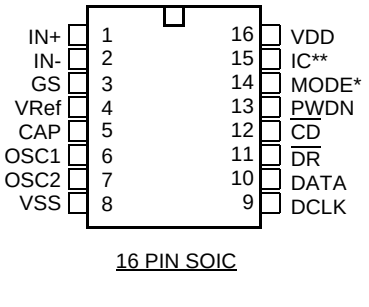


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	IN+	**Non-inverting Op-Amp (Input).**
2	IN-	**Inverting Op-Amp (Input).**
3	GS	**Gain Select (Output).** Gives access to op-amp output for connection of feedback resistor.
4	V_{Ref}	**Voltage Reference (Output).** Nominally $V_{DD}/2$. This is used to bias the op-amp inputs.
5	CAP	**Capacitor.** Connect a 0.1 μF capacitor to V_{SS}.
6	OSC1	**Oscillator (Input).** Crystal connection. This pin can be driven directly from an external clocking source.
7	OSC2	**Oscillator (Output).** Crystal connection. When OSC1 is driven by an external clock, this pin should be left open.
8	V_{SS}	Power supply ground.
9	DCLK	**3-wire FSK Interface: Data Clock (CMOS Output/Schmitt Input).** In mode 0 (MT88E41 compatible mode - when the MODE pin is logic low) this is a CMOS output which denotes the nominal mid-point of a FSK data bit. In mode 1 (when the MODE pin is logic high) this is a Schmitt trigger input used to shift the FSK data byte out to the DATA pin.
10	DATA	**3-wire FSK Interface: Data (CMOS Output).** In mode 0 (MT88E41 compatible mode - when the MODE pin is logic low) the FSK serial bit stream is output to DATA as demodulated. Mark frequency corresponds to logical 1. Space frequency corresponds to logical 0. In mode 1 (when the MODE pin is logic high) the start and stop bits are stripped off and only the data byte is stored in a 1 byte buffer. At the end of each word signalled by the $\overline{DR}$ pin, the microcontroller should shift the byte out to DATA pin by applying 8 read pulses at the DCLK pin.
11	$\overline{DR}$	**3-wire FSK Interface: Data Ready (Open Drain/CMOS Output).** Active low. In mode 0 (MT88E41 compatible mode - when the MODE pin is logic low) this is an open drain output. In mode 1 (when the MODE pin is logic high) this is a CMOS output. This pin denotes the end of a word. Typically, $\overline{DR}$ is used to interrupt the microcontroller. It is normally hi-Z or high (modes 0 and 1 respectively) and goes low for half a bit time at the end of a word. But in mode 1 if DCLK begins during $\overline{DR}$ low, the first rising edge of the DCLK input will return $\overline{DR}$ to high. This feature allows an interrupt requested by $\overline{DR}$ to be cleared upon reading the first DATA bit.

Pin Description

Pin #	Name	Description
12	$\overline{CD}$	**Carrier Detect (Open Drain/CMOS Output).** Active low. In mode 0 (MT88E41 compatible mode - when the MODE pin is logic low) this is an open drain output. In mode 1 (when the MODE pin is logic high) this is a CMOS output. A logic low indicates that a carrier has been present for a specified time on the line. A time hysteresis is provided to allow for momentary discontinuity of carrier. The demodulated FSK data is inhibited until the carrier has been detected.
13	PWDN	**Power Down (Schmitt Input).** Active high. Powers down the device including the input op-amp and the oscillator. Must be low for operation.
14	MODE	**Mode select (Input).** This pin selects the 3-wire FSK interface mode. To select mode 0 (MT88E41 compatible mode) this pin should be logic low. To select mode 1 this pin should be logic high. Because this pin is already connected to Vss in 'E41 applications, the MT88E39 can replace the 'E41 without any circuit or software change.
15	IC	**Internal Connection.** Internal connection. Leave open circuit. In MT88E41, this was IC2 which was also left open in the application circuit.
16	V_{DD}	Positive power supply voltage.

Functional Description

The MT88E39 is a FSK demodulator compatible with FSK based Caller ID services around the world, such as in North America, France, Germany, and Japan. Caller ID is the generic term for a group of services offered by telephone operating companies whereby information about the calling party is delivered to the subscriber. In the FSK based methods, the information is modulated in either Bell 202 (in North America) or CCITT V.23 (in Europe) FSK format and transmitted at 1200 baud from the serving end office to the subscriber's terminal.

In North America, Caller ID uses the voiceband data transmission interface defined in the Bellcore document GR-30-CORE. The terminal or CPE (Customer Premises Equipment) requirements are defined in Bellcore document SR-TSV-002476. Typical services are CND (Calling Number Delivery), CNAM (Calling Name Delivery), VMWI (Visual Message Waiting Indicator) and CIDCW (Calling Identity Delivery on Call Waiting).

In on-hook Caller ID, such as CND and CNAM, the information is typically transmitted from the end office before the subscriber picks up the phone. There are various methods such as between the first and second rings (North America), between an abbreviated ring and the first true ring (Japan, France and Germany). On-hook Caller ID can also occur without ringing for services such as VMWI. The MT88E39 is suitable for these forms of alerting.

In off-hook Caller ID, such as CIDCW, information about a new calling party is sent to the subscriber who is already engaged in a call. Bellcore's method uses a special dual tone known as CAS (CPE Alerting Signal) which should be detected by the CPE. After the CPE has acknowledged with a DTMF digit, the end office will send the FSK data. The MT88E39 is suitable for receiving the FSK data but a separate CAS detector is required.

The MT88E39 provides an interface to the Caller ID physical layer. It bandpass filters and demodulates the 1200 baud FSK signal. It also provides a convenient interface to extract the demodulated FSK data. Although the main application of the MT88E39 is Caller ID, it can also be used wherever 1200 baud Bell 202 and/or CCITT V.23 FSK reception is required.

3 to 5V operation

The MT88E39 can operate from 5.5 V down to 2.7 V, but the FSK reject level will change with Vdd. In a battery powered CPE, the FSK accept level will become lower as the batteries are run down. If the CPE is designed for 4.5 V, the accept level will be lowered when the batteries drain to 3 V. In North America there is a requirement for rejecting FSK signals which are below 3 mVrms when data is not preceded by ringing, such as VMWI (Visual

Message Waiting Indicator) applications. When the batteries are drained, the CPE will not meet the reject level. For on-hook Caller ID, there is no reject level and the CPE will meet all requirements.

Input Configuration

The input arrangement of the MT88E39 provides an operational amplifier, as well as a bias source (V_{Ref}) which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

Figure 3 shows the necessary connections for a differential input configuration. In a single-ended configuration, the input pins are connected as shown in Figure 4.

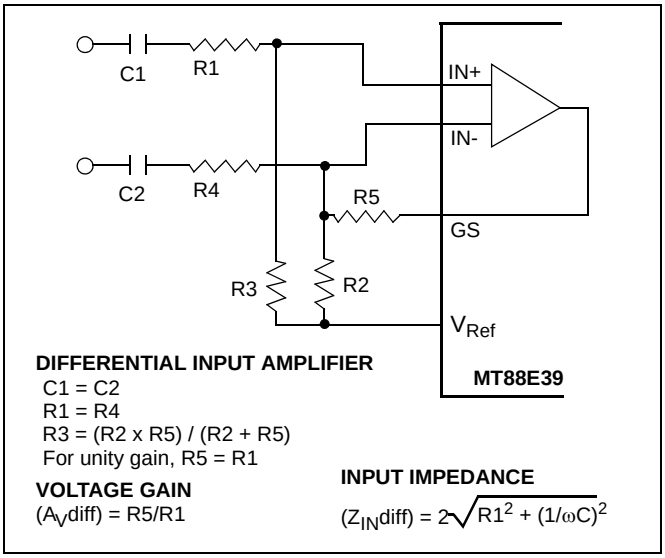


Figure 3 - Differential Input Configuration

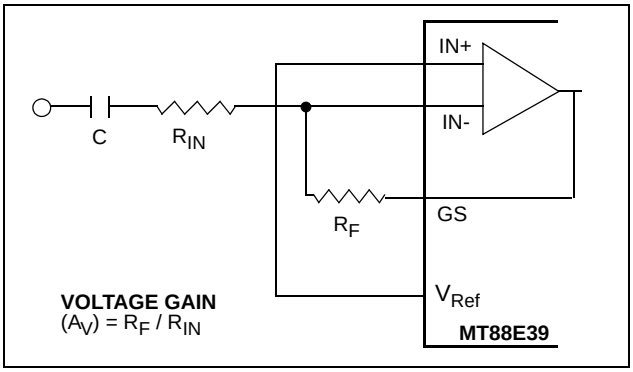


Figure 4 - Single-Ended Input Configuration

3-wire FSK Data Interface

The MT88E39 provides a powerful dual mode 3-wire interface so that the 8-bit data words in the demodulated FSK bit stream can be extracted without the need either for an external UART or for the microcontroller to perform the UART function in software. The interface is specifically designed for the 1200 baud rate and is comprised of the DATA, DCLK (data clock) and $\overline{DR}$ (data ready) pins. Two modes (0 and 1) are selectable via control of the device's MODE pin. In mode 0 the FSK bit stream is output as demodulated. In mode 1 the FSK data byte is store in a 1 byte buffer. Note that in mode 0 $\overline{DR}$ and $\overline{CD}$ are open drain outputs; in mode 1 they are CMOS outputs. DCLK is an output in mode 0, an input in mode 1.

Mode 0

This mode is selected when the MODE pin is low. It is the MT88E41 compatible mode where the FSK data stream is output as demodulated. Since the MODE pin was IC1 in MT88E41 and connected to Vss, the MT88E39 will work in mode 0 when placed in a MT88E41 socket.

In this mode, the MT88E39 receives the FSK signal, demodulates it, and outputs the data directly to the DATA pin (see Figure 11). For each received stop and start bit sequence, the MT88E39 outputs a fixed frequency clock string of 8 pulses at the DCLK pin. Each DCLK rising edge occurs in the nominal centre of a data bit. DCLK is not generated for the stop and start bits. Consequently, DCLK will clock only valid data into a peripheral device such as a serial to parallel shift register or a microcontroller. The MT88E39 also outputs an end of word pulse (Data Ready) on the $\overline{DR}$ pin, which indicates the reception of every 10-bit word (counting the start and stop bits) sent from the end office. $\overline{DR}$ can be used to interrupt a microcontroller or cause a serial to parallel converter to parallel load its data into a microcontroller. The mode 0 DATA pin can also be connected to a personal computer's serial communication port after converting from CMOS to RS-232 voltage levels.

Mode 1

This mode is selected when the MODE pin is high. In this mode, the microcontroller supplies read pulses at the DCLK pin (which is now an input) to shift the 8-bit data words out of the MT88E39, onto the DATA pin. The MT88E39 asserts $\overline{DR}$ to denote the word boundary and indicate to the microprocessor that a new word has become available (see Figure 12).

Internal to the MT88E39, the demodulated data bits are sampled and stored. The start and stop bits are stripped off. After the 8th bit, the data byte is parallel loaded into an 8 bit shift register and $\overline{DR}$ goes low. The shift register's contents are shifted out to the DATA pin on the supplied DCLK's rising edge in the order they were received.

If DCLK begins while $\overline{DR}$ is low, $\overline{DR}$ will return to high upon the first DCLK. This feature allows the associated interrupt to be cleared by the first read pulse. Otherwise $\overline{DR}$ is low for half a nominal bit time (1/2400 sec). After the last bit has been read, additional DCLKs are ignored.

Note that in both modes, the 3-pin interface may also output data generated by speech or other voiceband signals. The user may choose to ignore these outputs when FSK data is not expected, or force the MT88E39 into its power down mode.

Power Down Mode

For applications requiring reduced power consumption, the MT88E39 can be forced into power down when it is not needed. This is done by pulling the PWDN pin high. In power down mode, the oscillator, op-amp and internal circuitry are all disabled and the MT88E39 will not react to the input signal. $\overline{DR}$ and $\overline{CD}$ are at high impedance or at logic high (modes 0 and 1 respectively). In mode 0, DATA and DCLK are at logic high. The MT88E39 can be awakened for reception of the FSK signal by pulling the PWDN pin low.

Carrier Detect

The carrier detector provides an indication of the presence of a signal in the FSK frequency band. It detects the presence of a signal of sufficient amplitude at the output of the FSK bandpass filter. The signal is qualified by a digital algorithm before the $\overline{CD}$ output is set low to indicate carrier detection. A 10ms hysteresis is provided to allow for momentary signal drop out once $\overline{CD}$ has been activated. $\overline{CD}$ is released when there is no activity at the FSK bandpass filter output for 10 ms.

When $\overline{CD}$ is inactive (high), the raw output of the demodulator is ignored by the data timing recovery circuit (see Figure 1). In mode 0, the DATA pin is forced high. No DCLK or $\overline{DR}$ signal is generated. In mode 1, the internal shift register is not updated and no $\overline{DR}$ is generated. If DCLK is clocked (in mode 1), DATA is undefined.

Note that signals such as CAS, speech and DTMF tones also lie in the FSK frequency band and the carrier detector may be activated by these signals. They will be demodulated and presented as data. To avoid false data, the PWDN pin should be used to disable the FSK demodulator when no FSK signal is expected.

Ringing, on the other hand, does not pose a problem as it is ignored by the carrier detector.

Crystal Oscillator

The MT88E39 uses either a 3.579545 MHz ceramic resonator or crystal oscillator as the master timing source.

The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency tolerance:	±0.2%(-40°C+85°C)
Resonance mode:	Parallel
Load capacitance:	18 pF
Maximum series resistance:	150 ohms
Maximum drive level (mW):	2 mW

e.g., CTS MP036S

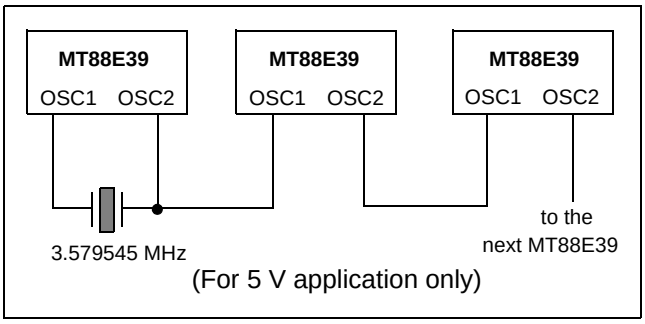


Figure 5 - Common Crystal Connection

For 5 V applications any number of MT88E39 devices can be connected as shown in Figure 5 such that only one crystal is required. The connection between OSC2 and OSC1 can be DC coupled as shown, or the OSC1 input on all devices can be driven from a CMOS buffer (dc coupled) with the OSC2 outputs left unconnected.

V_{Ref} and CAP Inputs

V_{Ref} is the output of a low impedance voltage source equal to $V_{DD}/2$ and is used to bias the input op-amp. A 0.1 µF capacitor is required between CAP and V_{SS} to suppress noise on $V_{Ref.}$

Applications

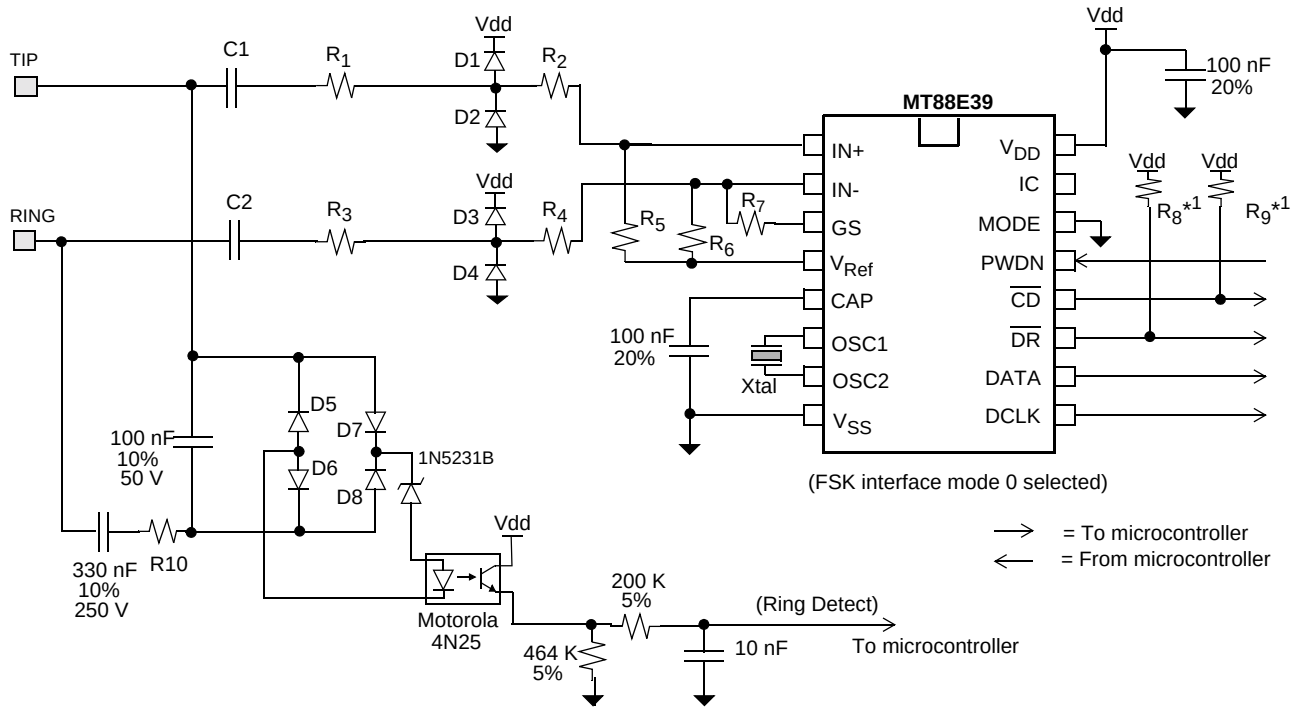
Table 1 shows the Bellcore and ETSI FSK signal characteristics. The application circuit in Figure 6 will meet these requirements.

For 5 V designs the input op-amp should be set to unity gain to meet the Bellcore requirements and -2.5 dB gain for ETSI requirements.

As supply voltage (V_{DD}) is decreased, the FSK detect threshold will be lowered. Therefore for designs operating at other than 5 V nominal voltage, to meet the FSK reject level requirement the gain of the op-amp should be reduced accordingly.

For 3 V designs the gain settings for Bellcore and ETSI should be -3 dB and -5.5 dB respectively.

For applications requiring detection of lower FSK signal level, the input op-amp may be configured to provide adequate gain. However, too much gain will cause noise tolerance to fail the TIA requirements because the FSK signal will be clipped at GS when the single tone noise is added.



Note:
*1 R8 and R9 not required when FSK interface mode 1 is selected.

Unless stated otherwise, resistors are 1%, 0.1 Watt; capacitors are 5%, 6.3 V
D1, D2, D3, D4 = diodes, 1N4003 or 1N4148 or equivalent
D5, D6, D7, D8 = bridge rectifier diodes, 1N914
Xtal = 3.579545 MHz, +/-0.2%
R8 = R9 = 100 K, 20%
R10 = 12K1, 1W5, 5%, Fusible resistor

R2 = R4 = 34 K

For 1000 Vrms, 60 Hz isolation from Tip to Earth and Ring to Earth:
R1 = R3 = 430 K, 0.5 W, 5%, 475 V minimum. e.g., IRC Type GS-3
C1 = C2 = 2 n2, 1332 V minimum

If the 1000Vrms is met by other means, then this circuit has to meet FCC part 68 Type B Ringing:
R1 = R3 = 432 K, 0.1 W, 1%, 56 V minimum
C1 = C2 = 2n2, 212V minimum

Example of component values for Vdd = 5 V +/- 10%

For Bellcore applications, set input gain = 0 dB:
R5 = 53K6
R6 = 60K4
R7 = 464K

For ETSI applications, set input gain = -2.5 dB:
R5 = 53K6
R6 = 63K4
R7 = 348K

Example of component values for Vdd = 3 V +/- 10%

For Bellcore applications, set input gain = -3 dB:
R5 = 44K2
R6 = 51K1
R7 = 332K

For ETSI applications, set input gain = -5.5 dB:
R5 = 44K2
R6 = 53K6
R7 = 249K

Figure 6 - Application Circuit

Parameter	North America: Bellcore *1	Europe: ETSI *2
Mark (logical 1) frequency	1200 Hz +/- 1%	1300 Hz +/- 1.5%
Space (logical 0) frequency	2200 Hz +/- 1%	2100 Hz +/- 1.5%
Received signal level	-36.20 to -4.23 dBm *3 (12 to 476 mVrms)	-33.78 to -5.78 dBm (-36 to -8 dBV *4) *5
Reject signal level	-48.23 dBm (3 mVrms) (VMWI only)	-47.78 dBm (-50 dBV)
Transmission rate	1200 baud +/- 1%	1200 baud +/- 1%
Twist	-6 to +10 dB	-6 to +6 dB
Signal to noise ratio	Single tone (f): -18 dB (f<=60 Hz) -12 dB (60<f<=120 Hz) -6 dB (120<f<=200 Hz) +25 dB (200<f<3200 Hz) +6 dB (f>=3200 Hz)	>= 25 db (300 to 3400 Hz)
MT88E39 FSK input gain for Vdd = 5 V +/-10%	0 dB	-2.5 dB

Table 1 - FSK signal characteristics specified by some standard bodies

Note:
*1: Recommended by TIA/EIA-716. Bellcore has agreed to the values and will incorporate them into its future standards.
*2: ETS 300 778-1 (On-hook) Sep 97, ETS 300 778-2 (Off-hook) Jan 97.
*3: dBm = Decibels above or below a reference power of 1 mW into 600 ohms. 0 dBm = 0.7746 Vrms.
*4: dBV = Decibels above or below a reference voltage of 1 Vrms. 0 dBV = 1 Vrms.
*5: On-hook signal range. The Off-hook signal levels are inside this range: -30.78 to -7.78 dBm.

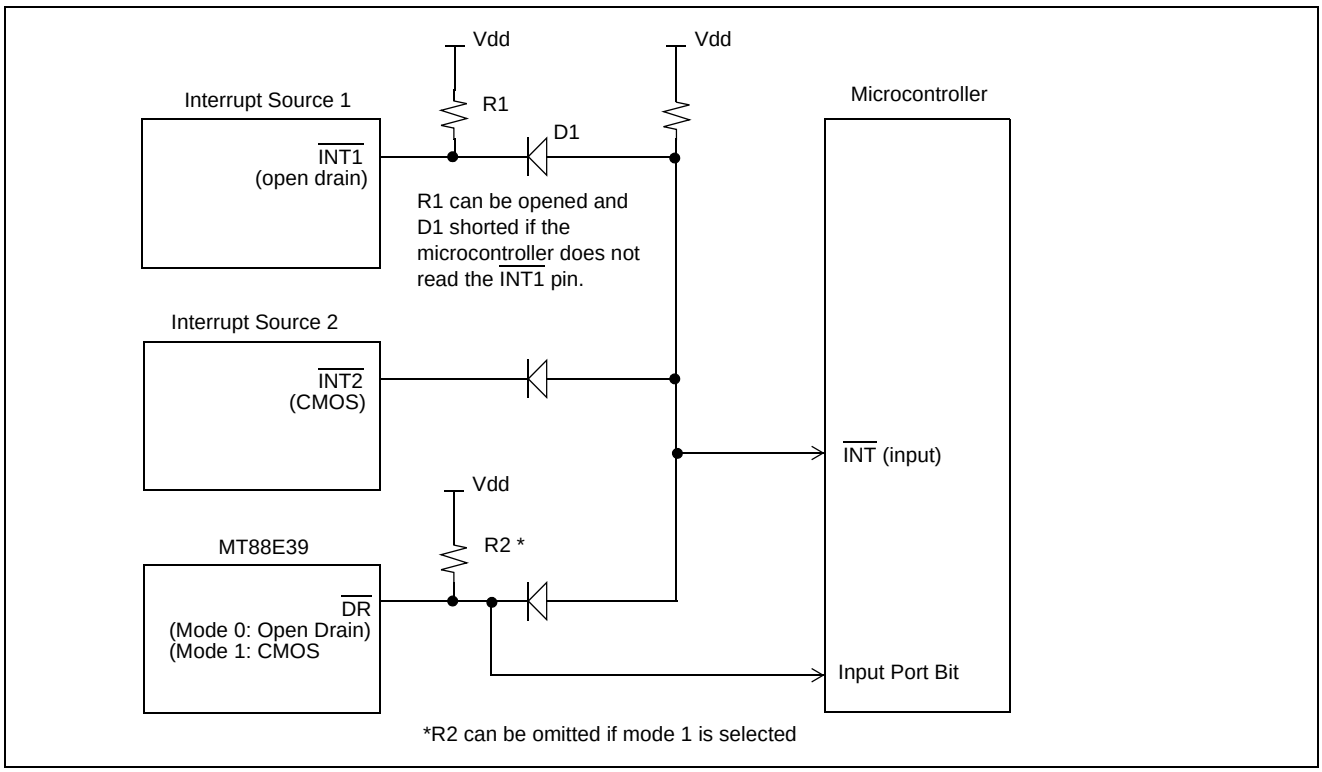


Figure 7 - Application Circuit (multiple interrupt source)

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter	Symbol	Min.	Max.	Units
1	DC Power Supply Voltage V_{DD} to V_{SS}	V_{DD}	-0.3	6	V
2	Voltage on any pin	V_P	-0.3	V_{DD}+0.3	V
3	Current at any pin (except V_{DD} and V_{SS})	$I_{I/O}$		±10	mA
4	Storage Temperature	T_{ST}	-65	+150	°C
5	Package Power Dissipation	P_D		500	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	2.7		5.5	V	
2	Clock Frequency	f_{OSC}		3.579545		MHz	
3	Tolerance on Clock Frequency	Δfc			±0.2	%	
4	Operating Temperature		-40		+85	°C	

DC Electrical Characteristics†

		Characteristics	Sym.	Min.	Typ.*	Max.	Units	Test Conditions
1	SUPPLY	Standby Supply Current	I_{DDQ}		0.1	15	µA	Notes* 1
2		Operating Supply Current V_{DD} = 3.0 V, 25°C V_{DD} = 5.0 V, 25°C	I_{DD}		 1.2 1.9	 2.0 3.0	 mA mA	Notes* 2
3	$\overline{DR}$, CD, DATA, DCLK	Sink Current	I_{OL}	2.5			mA	V_{OL} = 0.1 V_{DD}
4		Source current DATA DCLK (in mode 0) DR, CD (in mode 1)	I_{OH}	0.8			mA	V_{OH} = 0.9 V_{DD}
5	$\overline{DR}$, $\overline{CD}$	Output hi-Z current (in mode 0)	I_{OZ}			10	µA	V_{OZ}=V_{SS} to V_{DD}
6	PWDN, DCLK (in mode 1)	Schmitt Input High Threshold Schmitt Input Low Threshold	V_{T+} V_{T-}	0.48*V_{DD} 0.28*V_{DD}		0.68*V_{DD} 0.48*V_{DD}	V V	
7		Schmitt Hysteresis	V_{HYS}	0.2			V	
8	MODE	CMOS Input High Voltage CMOS Input Low Voltage	V_{IH} V_{IL}	0.7*V_{DD} V_{SS}		V_{DD} 0.3*V_{DD}	V	
9	PWDN, DCLK, MODE	Input Current	I_{IN}			10	µA	$V_{SS} \le V_{IN} \le V_{DD}$
10	VRef	Output Voltage	V_{Ref}	0.5*V_{DD} - 0.1		0.5*V_{DD} + 0.1	V	No Load
11		Output Resistance	R_{Ref}			2	k Ω	

† DC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
* Typical figures are at 25°C and are for design aid only.

Note 1: PWDN = Vdd. FSK input = 0 mVrms. Digital inputs at either Vdd or Vss. No current drawn from output pins.

Note 2: PWDN = Vss. FSK input = 0 mVrms. With no current drawn from Vref, OSC2 and all digital pins.

Electrical Characteristics† - Gain Setting Amplifier

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input Leakage Current	I_{IN}			1	µA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input Resistance	R_{in}	5			MΩ	
3	Input Offset Voltage	V_{OS}			25	mV	
4	Power Supply Rejection Ratio	PSRR	30			dB	1 kHz ripple on V_{DD}
5	Common Mode Rejection	CMRR	30			dB	$V_{CMmin} \le V_{IN} \le V_{CMmax}$
6	DC Open Loop Voltage Gain	A_{VOL}	40			dB	
7	Unity Gain Bandwidth	f_C	0.2			MHz	
8	Output Voltage Swing	V_O	0.5		V_{DD}-0.7	V	Load ≥ 100 kΩ
9	Capacitive Load (GS)	C_L			50	pF	
10	Resistive Load (GS)	R_L	100			kΩ	
11	Common Mode Voltage Range	V_{CM}	1.0		V_{DD}-1.0	V	

† Electrical characteristics are over recommended operating conditions, unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FSK

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	Input Detection Level		-37.78 -40 10		-1.78 -4 631	dBm dBV mVrms	1, 2, 3, 4
2	Input Baud Rate		1188	1200	1212	baud	6
3	Input Frequency Detection Bell 202 1 (Mark) Bell 202 0 (Space) CCITT V.23 1 (Mark) CCITT V.23 0 (Space)		 1188 2178 1280.5 2068.5	 1200 2200 1300 2100	 1212 2222 1319.5 2131.5	 Hz Hz Hz Hz	
4	Input Noise Tolerance 20 log	SNR	20			dB	3, 4, 5
5	Twist=20 $\log(\frac{V_{Mark}}{V_{Space}})$		-6		10	dB	

† AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Notes*:
1. dBm = Decibels above or below a reference power of 1 mW into 600 Ω. 0 dBm = 0.7746 Vrms.
2. dBV = Decibels above or below a reference voltage of 1 Vrms. 0 dBV = 1 Vrms.
3. Input op-amp configured to 0 dB gain at Vdd = 5 V+/-10%, -3 dB at Vdd = 3 V+/-10%.
4. Mark and Space frequencies have the same amplitude.
5. Band limited random noise (200-3400 Hz). Present when FSK signal present.
6. OSC1 at 3.579545 MHz ±0.2%.

AC Electrical Characteristics† - Timing

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	PWDN OSC1	Power-up time	t_{PU}			50	ms	
2		Power-down time	t_{PD}		100	1000	µs	1
3	$\overline{CD}$	Input FSK to $\overline{CD}$ low delay	t_{IAL}			25	ms	
4		Input FSK to $\overline{CD}$ high delay	t_{IAH}	10			ms	
5		Hysteresis		10			ms	

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.
Notes*:
1. The device will stop functioning within this time, but more time may be required to reach I_{DDQ}.

AC Electrical Characteristics† - 3-Wire FSK Interface Timing (Mode 0)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units.	Notes*
1	DATA	Rate		1188	1200	1212	bps	1, 6
2		Input FSK to DATA delay	t_{IDD}		1	5	ms	
3	DATA DCLK	Rise time	t_R			200	ns	3
4		Fall time	t_F			200	ns	3
5		DATA to DCLK delay	t_{DCD}	6	416		µs	1, 2, 5, 6
6		DCLK to DATA delay	t_{CDD}	6	416		µs	1, 2, 5, 6
7	DCLK	Frequency		1200.4	1202.8	1205.2	Hz	2
8		High time	t_{CH}	415	416	417	µs	2
9		Low time	t_{CL}	415	416	417	µs	2
10	DCLK $\overline{DR}$	DCLK to $\overline{DR}$ delay	t_{CRD}	415	416	417	µs	2
11	$\overline{DR}$	Rise time	t_{RR}			10	µs	4
12		Fall time	t_{FF}			200	ns	4
13		Low time	t_{RL}	415	416	417	µs	2

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.
Notes*:
1. FSK input data at 1200 ±12 baud.
2. OSC1 at 3.579545 MHz ±0.2%.
3. 10 k to V_{SS}, 50pF to V_{SS}.
4. 10 k to V_{DD}, 50pF to V_{SS}.
5. Function of signal condition.
6. For a repeating mark space sequence, the data stream will typically have equal 1 and 0 bit durations.

AC Electrical Characteristics† - 3-Wire FSK Interface Timing (Mode 1)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	DCLK	Frequency	f_{DCLK1}			1	MHz	See Fig. 12
2		Duty Cycle		30		70	%	
3		Rise Time				100	ns	
4	DCLK $\overline{DR}$	DCLK low setup time to $\overline{DR}$	t_{DDS}	500			ns	See Fig. 12
5		DCLK low hold time to $\overline{DR}$	t_{DDH}	500			ns	See Fig. 12

† AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C and are for design aid only, not guaranteed and not subject to production testing.

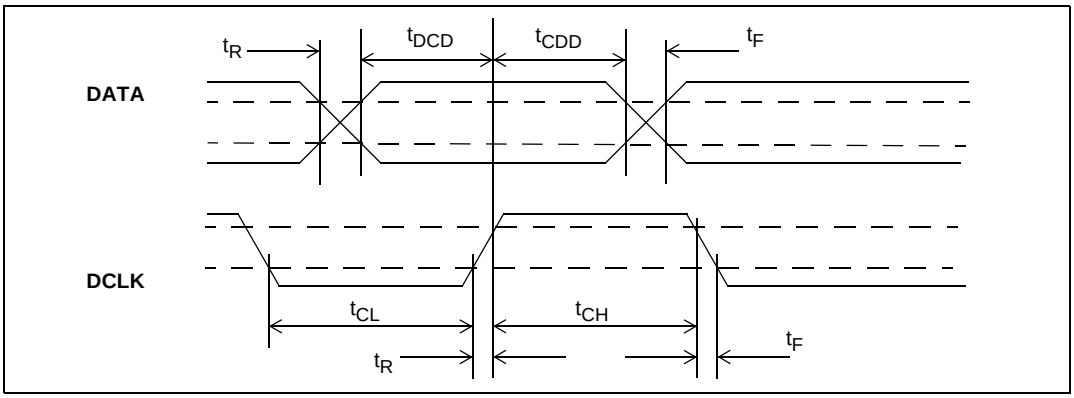


Figure 8 - DATA and DCLK Output Timing (Mode 0)

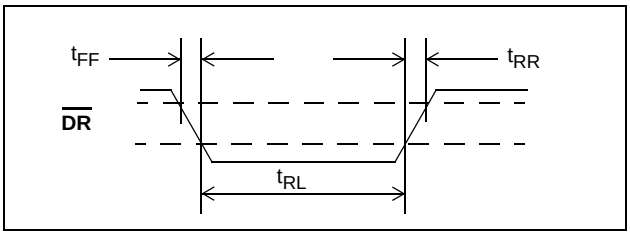


Figure 9 - $\overline{DR}$ Output Timing (Mode 0)

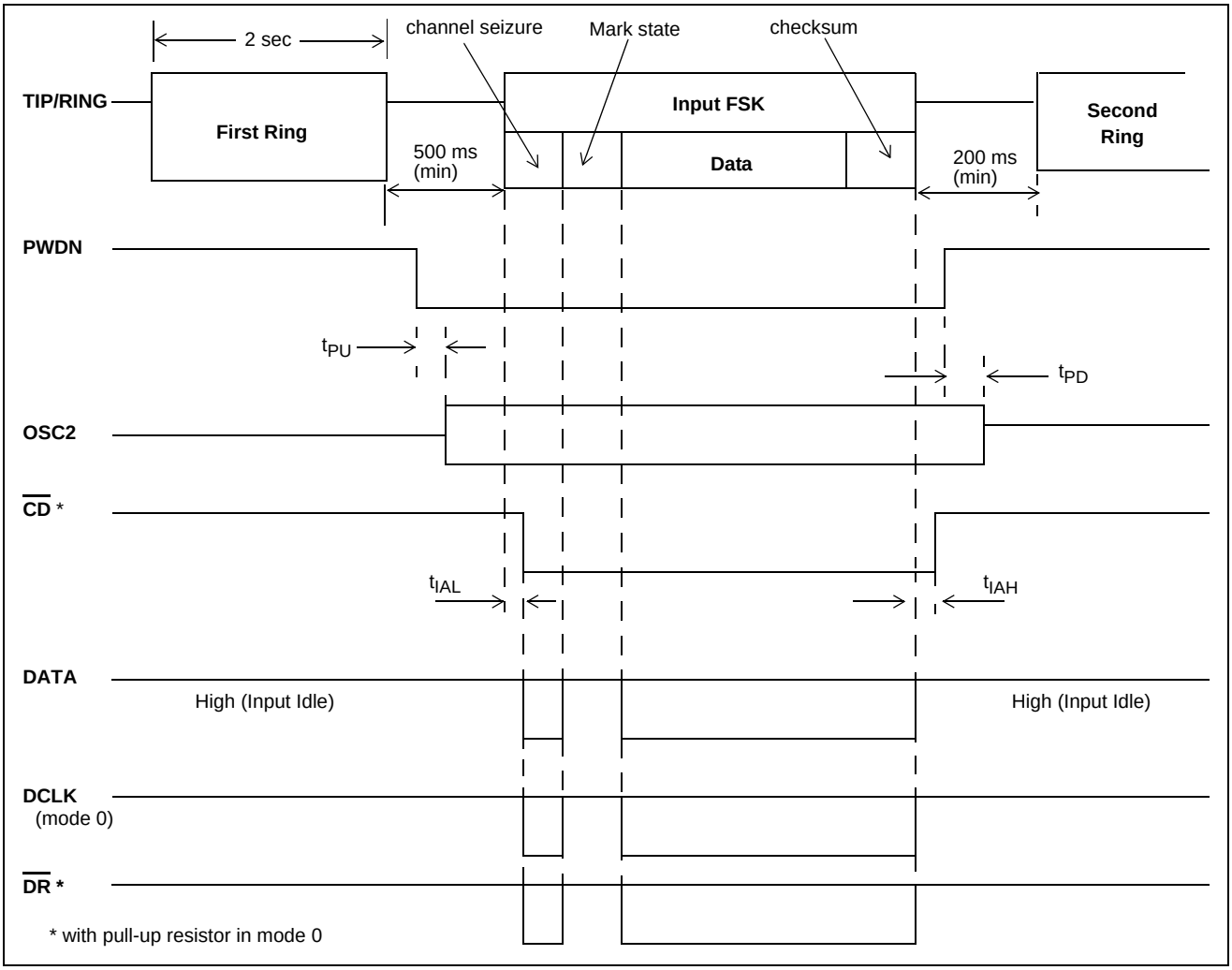


Figure 10 - Input and Output Timing (Bellcore CND Service)

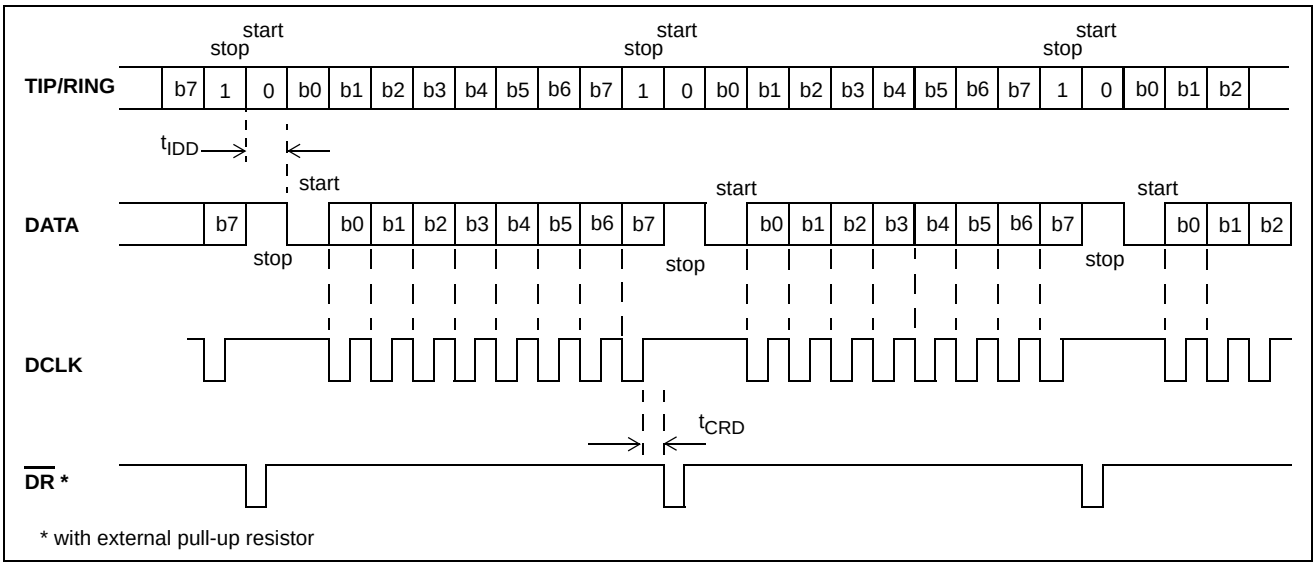


Figure 11 - Serial Data Interface Timing (Mode 0)

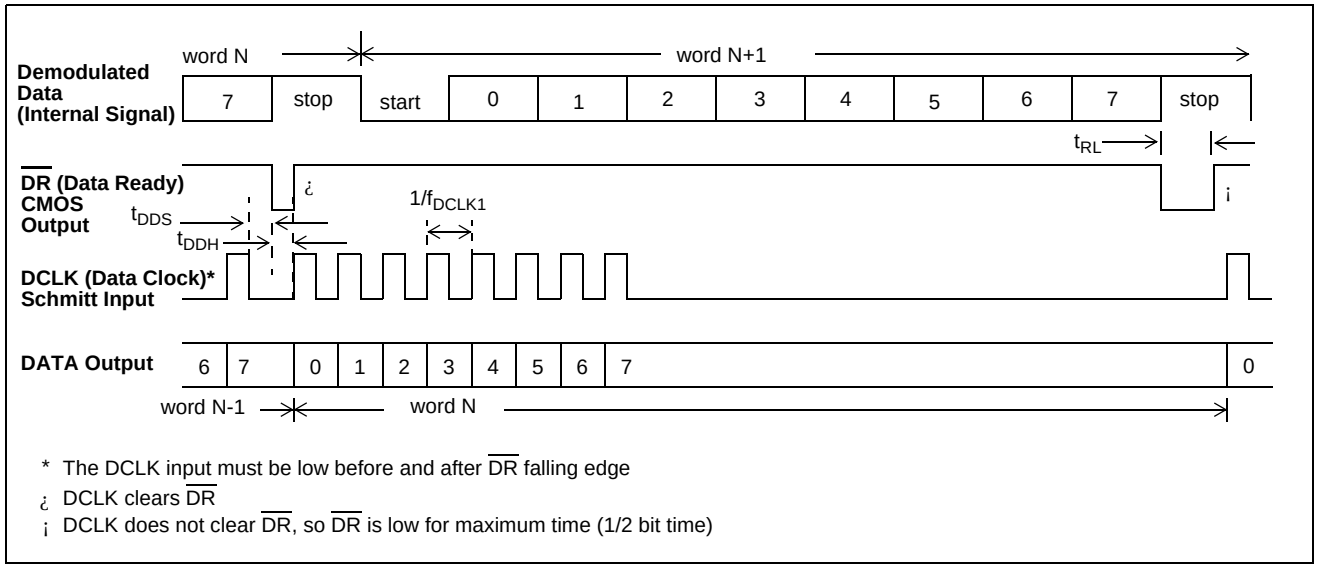
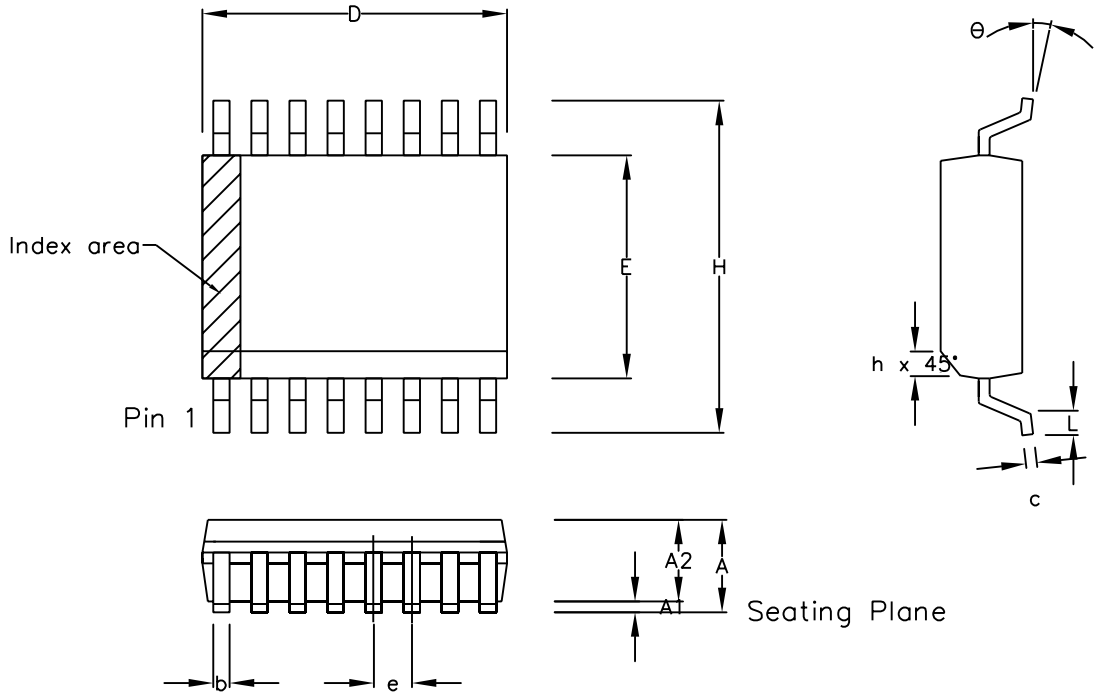


Figure 12 - Serial Data Interface Timing (Mode 1)



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	10.10		10.50		0.398		0.413
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	16						
Conforms to JEDEC MS-013AA Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	6745	201939	213097	
DATE	7Apr95	27Feb97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 16 lead SOIC (0.300" Body Width)

GPD00013

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