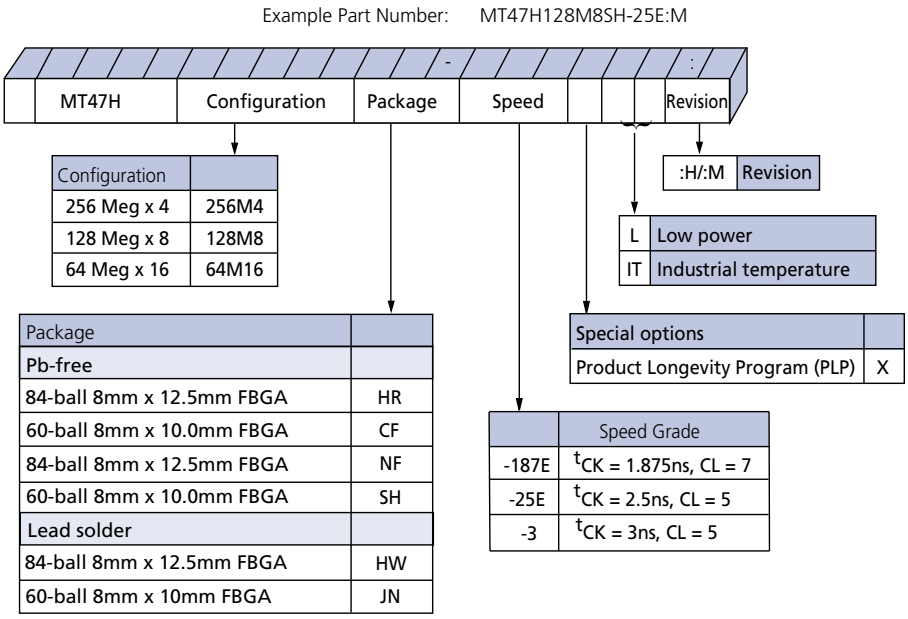
Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)					tRC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	CL = 7	
-187E	400	533	800	800	1066	54
-25E	400	533	800	800	n/a	55
-3	400	533	667	n/a	n/a	55

Table 2: Addressing

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 banks	16 Meg x 8 x 8 banks	8 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	A[13:0] (16K)	A[13:0] (16K)	A[12:0] (8K)
Bank address	BA[2:0] (8)	BA[2:0] (8)	BA[2:0] (8)
Column address	A[11, 9:0] (2K)	A[9:0] (1K)	A[9:0] (1K)

Figure 1: 1Gb DDR2 Part Numbers



Note: 1. Not all speeds and configurations are available in all packages.

FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

Revision History

Rev. A – 5/14

- Initial release; based on 1Gb: x4, x8, x16 DDR2 SDRAM, Rev. AA 04/14 data sheet (09005aef8565148a)

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.