**FAIRCHILD**

*SEMICONDUCTOR* ™

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# MM74HCT138
# 3-to-8 Line Decoder

## General Description

The MM74HCT138 decoder utilizes advanced silicon-gate CMOS technology, and are well suited to memory address decoding or data routing applications. Both circuits feature high noise immunity and low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

The MM74HCT138 have 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally HIGH outputs will go LOW. Two active LOW and one active HIGH enables (G1, G2A and G2B) are provided to ease the cascading decoders.

The decoders' output can drive 10 low power Schottky TTL equivalent loads and are functionally and pin equivalent to the 74LS138. All inputs are protected from damage due to static discharge by diodes to $V_{CC}$ and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

## Features

■ TTL input compatible
■ Typical propagation delay: 20 ns
■ Low quiescent current: 80 μA maximum (74HCT Series)
■ Low input current: 1 μA maximum
■ Fanout of 10 LS-TTL loads

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| MM74HCT138M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HCT138SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HCT138MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HCT138N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram

**Pin Assignments for DIP, SOIC, SOP and TSSOP**



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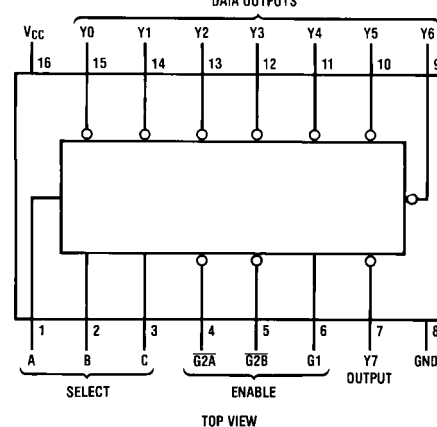
## Truth Table

| Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | Select | | | | | | | | | | |
| G1 | $\overline{G2}$ (Note 1) | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH Level
L = LOW Level
X = Don't Care
**Note 1:** $\overline{G2} = \overline{G2A} + \overline{G2B}$

## Logic Diagram

MM74HCT138
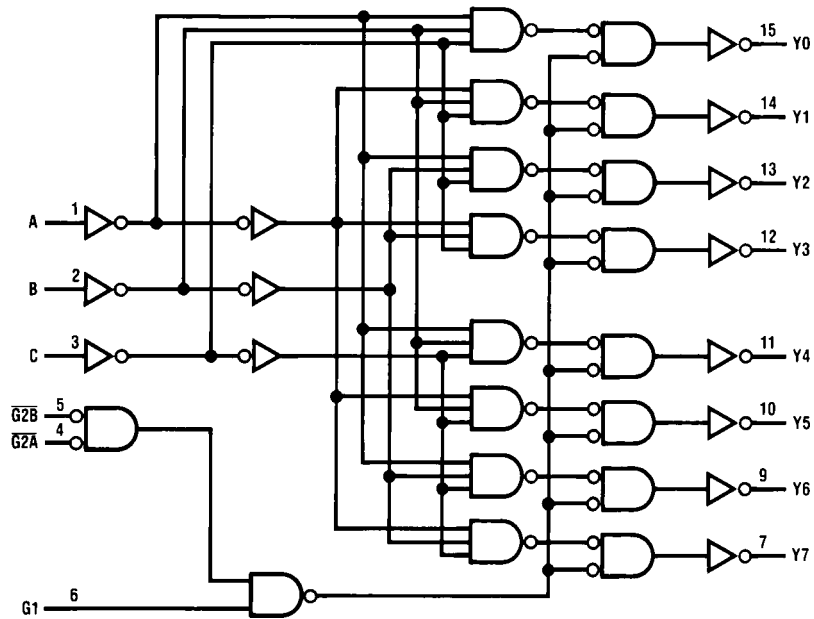
## Absolute Maximum Ratings (Note 2)

(Note 3)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to $V_{CC}$ +1.5V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$ +0.5V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ±20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| (Note 4) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature ($T_L$) | |
| (Soldering 10 seconds) | 260°C |

## Recommended Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 4.5 | 5.5 | V |
| DC Input or Output Voltage | | | |
| ($V_{IN}$, $V_{OUT}$) | 0 | $V_{CC}$ | V |
| Operating Temperature Range ($T_A$) | −40 | +85 | °C |
| Input Rise or Fall Times | | | |
| ($t_r$, $t_f$) | | 500 | ns |

**Note 2:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 3:** Unless otherwise specified all voltages are referenced to ground.

**Note 4:** Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

## DC Electrical Characteristics

$V_{CC}$ = 5V ±10% (unless otherwise specified)

| Symbol | Parameter | Conditions | $T_A$ = 25°C | $T_A$ = −40 to 85°C | $T_A$ = −55 to 125°C | Units |
|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | | 2.0 | 2.0 | 2.0 | V |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | | 0.8 | 0.8 | 0.8 | V |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $|I_{OUT}|$ = 20 μA | $V_{CC}$ | $V_{CC}$− 0.1 | $V_{CC}$− 0.1 | $V_{CC}$− 0.1 | V |
| | | $|I_{OUT}|$ = 4.0 mA, $V_{CC}$ = 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | $|I_{OUT}|$ = 4.8 mA, $V_{CC}$ = 5.5V | 5.2 | 4.98 | 4.84 | 4.7 | V |
| $V_{OL}$ | Maximum LOW Level Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $|I_{OUT}|$ = 20 μA | 0 | 0.1 | 0.1 | 0.1 | V |
| | | $|I_{OUT}|$ = 4.0 mA, $V_{CC}$ = 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | $|I_{OUT}|$ = 4.8 mA, $V_{CC}$ = 5.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND, $V_{IH}$ or $V_{IL}$ | | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND $I_{OUT}$ = 0 μA | | 8.0 | 80 | 160 | μA |
| | | $V_{IN}$ = 2.4V or 0.5V (Note 5) | | 0.3 | 0.4 | 0.5 | mA |

**Note 5:** This is measured per input pin. All other inputs are held at $V_{CC}$ or ground.

# AC Electrical Characteristics

$T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $t_{PHL}$ | Maximum Propagation Delay, A, B, or C to Output | | 20 | 35 | ns |
| $t_{PLH}$ | Maximum Propagation Delay, A, B, or C to Output | | 13 | 25 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, G1 to Y Output | | 14 | 25 | ns |
| $t_{PLH}$ | Maximum Propagation Delay, G1 to Y Output | | 13 | 25 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output | | 17 | 30 | ns |
| $t_{PLH}$ | Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output | | 13 | 25 | ns |

# AC Electrical Characteristics

$V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

| Symbol | Parameter | Conditions | $T_A = 25°C$ | | $T_A = -40$ to $85°C$ | $T_A = -55$ to $125°C$ | Units |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $t_{PHL}$ | Maximum Propagation Delay A, B, or C to Output | | 24 | 40 | 50 | 60 | ns |
| $t_{PLH}$ | Maximum Propagation Delay A, B, or C to Output | | 18 | 30 | 38 | 45 | ns |
| $t_{PHL}$ | Maximum Propagation Delay G1 to Y Output | | 17 | 30 | 38 | 45 | ns |
| $t_{PLH}$ | Maximum Propagation Delay G1 to Y Output | | 20 | 30 | 38 | 45 | ns |
| $t_{PHL}$ | Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output | | 23 | 35 | 43 | 52 | ns |
| $t_{PLH}$ | Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output | | 18 | 30 | 38 | 45 | ns |
| $t_{THL}$, $t_{TLH}$ | Maximum Output Rise and Fall Time | | | 15 | 19 | 22 | ns |
| $C_{IN}$ | Input Capacitance | | | 5 | 10 | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | (Note 6) | 55 | | | | pF |

**Note 6:** $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

## Physical Dimensions inches (millimeters) unless otherwise noted
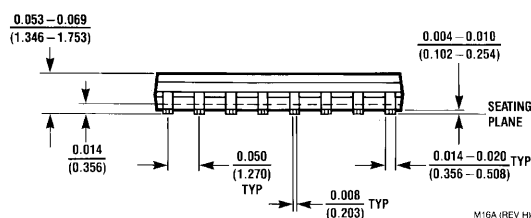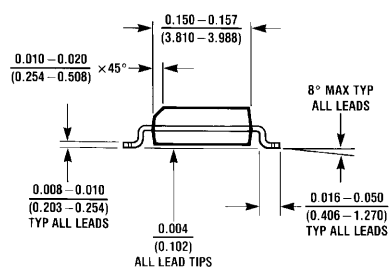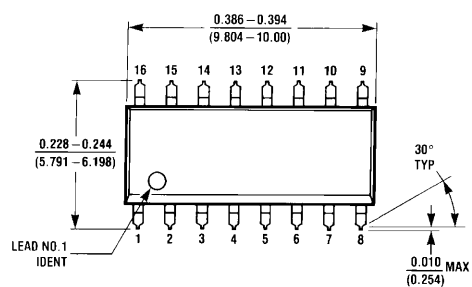


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M16A**
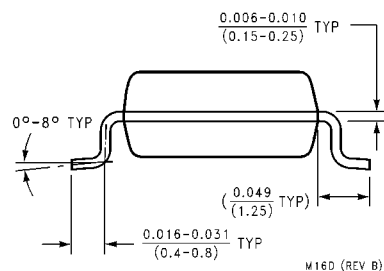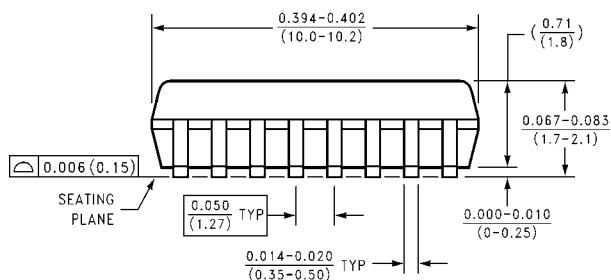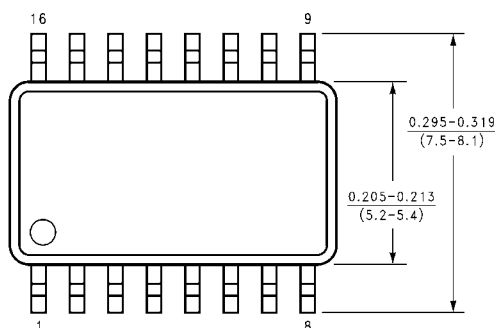


**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M16D**

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# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS METRIC ONLY

LAND PATTERN RECOMMENDATION

DETAIL A
TYPICAL, SCALE: 40X

**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N16E**
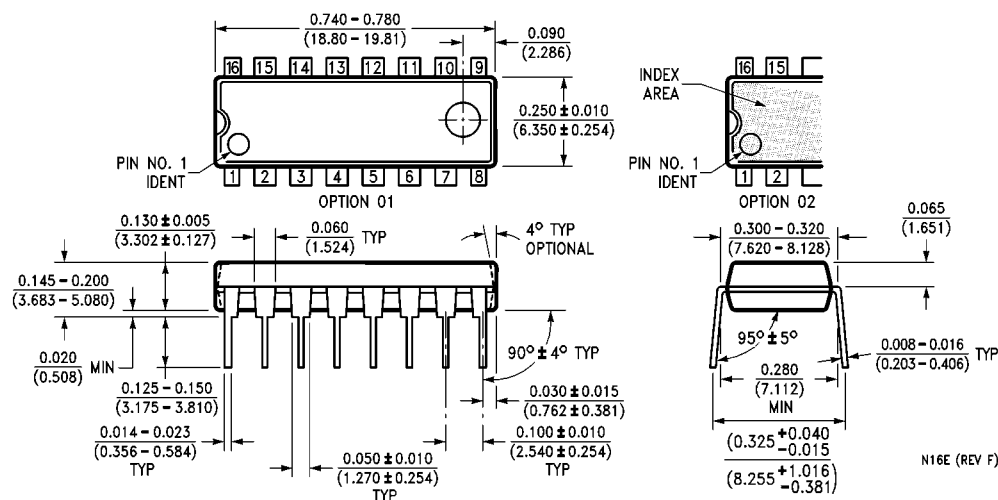
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