Requirements

At a minimum, the evaluation board requires an 8V to 16V supply to power the MIC410x driver. Another supply (up to 100V) may be used to power the MOSFETs at the "HV Supply" terminal. A pulse generator or the output of a PWM control IC may be connected to the HI and/or LI terminals. The board can be used with either of the 4 driver IC's.

MIC4100/3: The HI and LI inputs have a CMOS compatible threshold. The high-side and low-side drivers are independently controlled by the HI and LI inputs. The inputs may be connected to separate PWM sources or can be connected together.

MIC4101/4: Same as the MIC4100/3 but the inputs have a TTL compatible threshold.

Getting Started

The simplest way to observe driver operation is to connect the "High Side Fet Source" terminal to ground (or any voltage potential under 100V) and apply a PWM signal to the "HI" and/or "LI" input terminals. DC and AC parameters can be measured in this configuration. The included SO-8 MOSFETs can be removed or replaced with different FETs. D^2PAK locations are provided on the back of the board.

The source terminal of the high-side FET and drain terminal of the low-side FET are floating and accessible through the board terminals. This allows the board to be used with different power topologies such as the synchronous buck, half-bridge, full-bridge or two transistor forward converter.

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
U1	MIC4100BM	Micrel.Inc[1]	Buck controller	1
	MIC4101BM	Micrel.Inc[1]		OR
	MIC4103BM	Micrel.Inc[1]		OR
	MIC4104BM	Micrel.Inc[1]		OR
Q1,Q2	Si4484EY	Vishay/Siliconix[2]	100V N-channel MOSFET	2
Q1A, Q2A		Vishay/Siliconix[2]	open location for D2PAK FETs	0
C1, C2	VJ0603Y104KXXAT	Vishay[2]	0.1uf/25V, X7R ceramic cap 0603 size	2
C3	C4532X7R2A105M	TDK[3]	1uf, 100V, ceramic, X7R	1
	C3225X7R2A105M.	TDK[3]		OR
	GRM55DR72A105KA01B	MuRata[4]		OR

Notes:

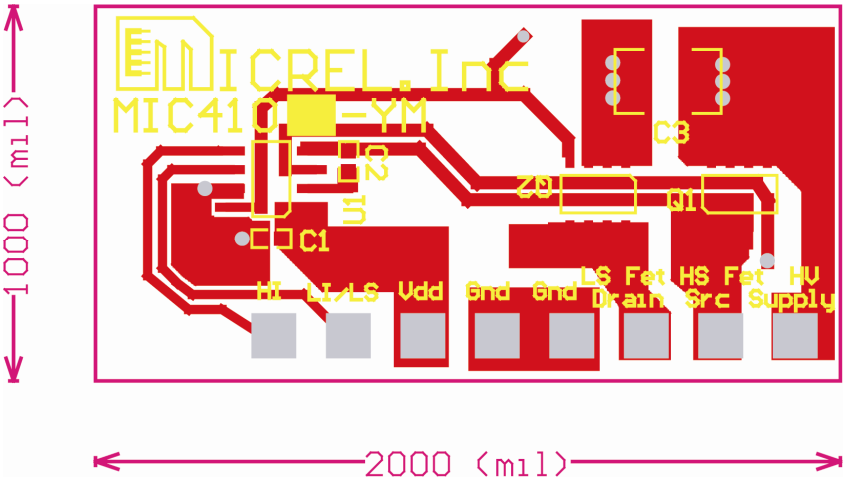
1. Micrel Inc.: 408-944-0800

2. Vishay Corp.: 206-452-5664

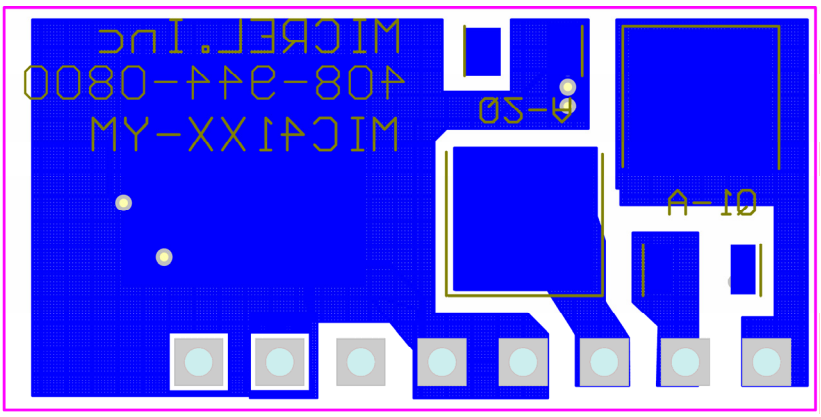
3. TDK: 562-596-1212

4. MuRata: 949-916-4000

Board layout



Top Layer



Bottom Layer

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