NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings†

V_{DD} 7.0V
All inputs and outputs w.r.t. V_{SS} .... -0.6V to V_{DD} +0.6V
Storage temperature ....-65°C to +150°C
Ambient temp. with power applied ....-65°C to +125°C
ESD protection on all pins (HBM) ....> 4 kV

†Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: All parameters apply at V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 5V, T_A = -40°C to +85°C, f_{SAMPLE} = 100 ksps, and fCLK = 16*f_{SAMPLE}, unless otherwise noted.

Parameter	Sym	Min	Typ	Max	Units	Conditions
Conversion Rate:						
Conversion Time	t_{CONV}	—	—	12	clock cycles	
Analog Input Sample Time	t_{SAMPLE}		1.5		clock cycles	
Throughput Rate	f_{SAMPLE}	—	—	100 50	ksps ksps	V_{DD} = V_{REF} = 5V V_{DD} = V_{REF} = 2.7V
DC Accuracy:						
Resolution			12		bits	
Integral Nonlinearity	INL	— —	±0.75 ±1	±1 ±2	LSB LSB	MCP3201-B MCP3201-C
Differential Nonlinearity	DNL	—	±0.5	±1	LSB	No missing codes over temperature
Offset Error		—	±1.25	±3	LSB	
Gain Error		—	±1.25	±5	LSB	
Dynamic Performance:						
Total Harmonic Distortion	THD	—	-82	—	dB	VIN = 0.1V to 4.9V@1 kHz
Signal to Noise and Distortion (SINAD)	SINAD	—	72	—	dB	VIN = 0.1V to 4.9V@1 kHz
Spurious Free Dynamic Range	SFDR	—	86	—	dB	VIN = 0.1V to 4.9V@1 kHz
Reference Input:						
Voltage Range		0.25	—	V_{DD}	V	Note 2
Current Drain		— —	100 .001	150 3	µA µA	 CS = V_{DD} = 5V
Analog Inputs:						
Input Voltage Range (IN+)	IN+	IN-	—	V_{REF}+IN-	V	
Input Voltage Range (IN-)	IN-	V_{SS}-100		V_{SS}+100	mV	
Leakage Current		—	0.001	±1	µA	
Switch Resistance	R_{SS}	—	1K	—	W	See Figure 4-1
Sample Capacitor	C_{SAMPLE}	—	20	—	pF	See Figure 4-1
Digital Input/Output:						
Data Coding Format			Straight Binary			
High Level Input Voltage	V_{IH}	0.7 V_{DD}	—	—	V	
Low Level Input Voltage	V_{IL}	—	—	0.3 V_{DD}	V	

Note 1: This parameter is established by characterization and not 100% tested.
2: See graph that relates linearity performance to V_{REF} level.
3: Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See **Section 6.2 "Maintaining Minimum Clock Speed"** for more information.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: All parameters apply at V_{DD} = 5V, V_{SS} = 0V, V_{REF} = 5V, T_A = -40°C to +85°C, f_{SAMPLE} = 100 ksps, and fCLK = 16*f_{SAMPLE}, unless otherwise noted.						
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
High Level Output Voltage	V_{OH}	4.1	—	—	V	I_{OH} = -1 mA, V_{DD} = 4.5V
Low Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1 mA, V_{DD} = 4.5V
Input Leakage Current	I_{LI}	-10	—	10	µA	V_{IN} = V_{SS} or V_{DD}
Output Leakage Current	I_{LO}	-10	—	10	µA	V_{OUT} = V_{SS} or V_{DD}
Pin Capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	—	10	pF	V_{DD} = 5.0V (**Note 1**) T_A = +25°C, f = 1 MHz
Timing Parameters:						
Clock Frequency	f_{CLK}	— —	— —	1.6 0.8	MHz MHz	V_{DD} = 5V (**Note 3**) V_{DD} = 2.7V (**Note 3**)
Clock High Time	t_{HI}	312	—	—	ns	
Clock Low Time	t_{LO}	312	—	—	ns	
$\overline{CS}$ Fall To First Rising CLK Edge	t_{SUCS}	100	—	—	ns	
CLK Fall To Output Data Valid	t_{DO}	—	—	200	ns	See Test Circuits, Figure 1-2
CLK Fall To Output Enable	t_{EN}	—	—	200	ns	See Test Circuits, Figure 1-2
$\overline{CS}$ Rise To Output Disable	t_{DIS}	—	—	100	ns	See Test Circuits, Figure 1-2 (**Note 1**)
$\overline{CS}$ Disable Time	t_{CSH}	625	—	—	ns	
D_{OUT} Rise Time	t_R	—	—	100	ns	See Test Circuits, Figure 1-2 (**Note 1**)
D_{OUT} Fall Time	t_F	—	—	100	ns	See Test Circuits, Figure 1-2 (**Note 1**)
Power Requirements:						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Operating Current	I_{DD}	— —	300 210	400 —	µA µA	V_{DD} = 5.0V, D_{OUT} unloaded V_{DD} = 2.7V, D_{OUT} unloaded
Standby Current	I_{DDS}	—	0.5	2	µA	$\overline{CS}$ = V_{DD} = 5.0V

Note 1: This parameter is established by characterization and not 100% tested.
2: See graph that relates linearity performance to V_{REF} level.
3: Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, especially at elevated temperatures. See **Section 6.2 "Maintaining Minimum Clock Speed"** for more information.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+85	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.5	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	139	—	°C/W	

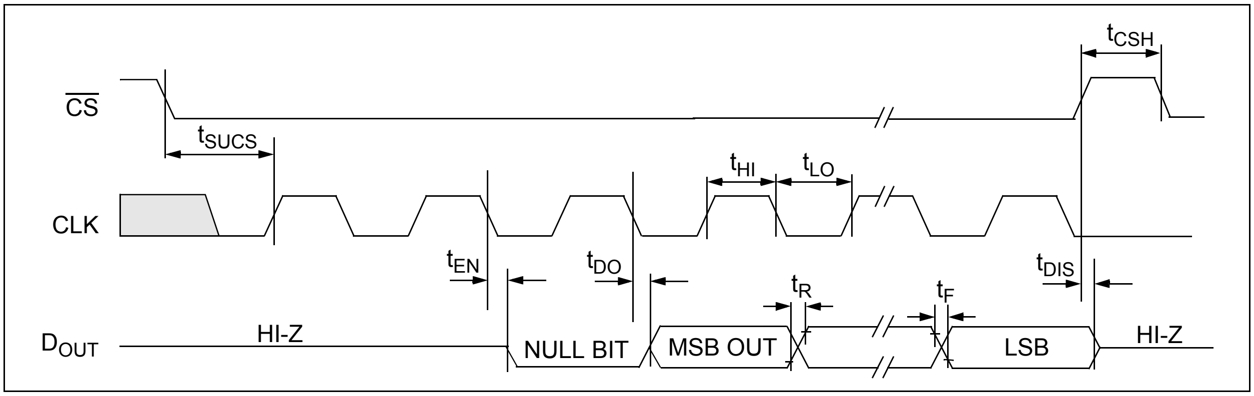


FIGURE 1-1: *Serial Timing.*

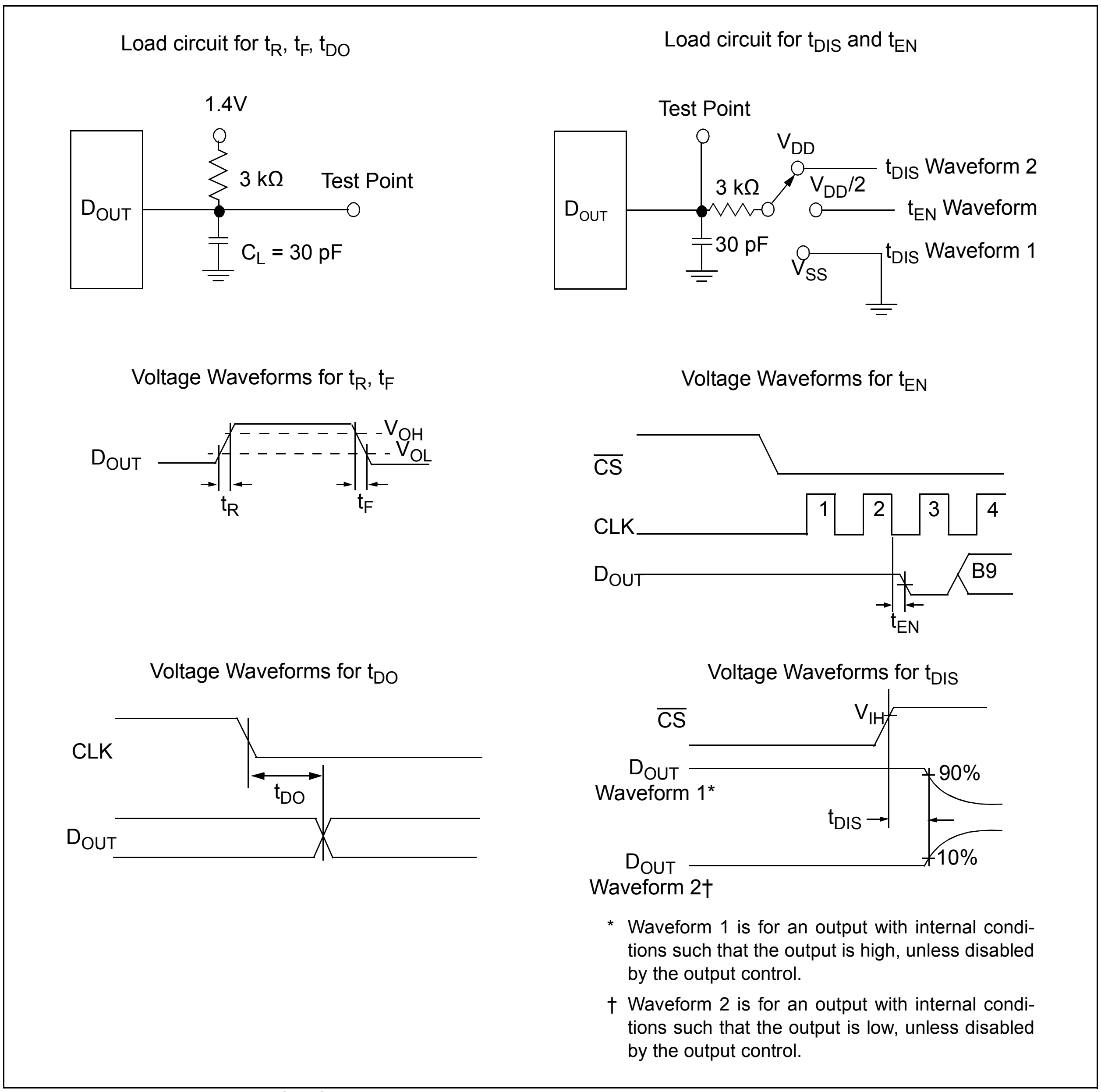


FIGURE 1-2: *Test Circuits.*

NOTES:

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = +25°C$.

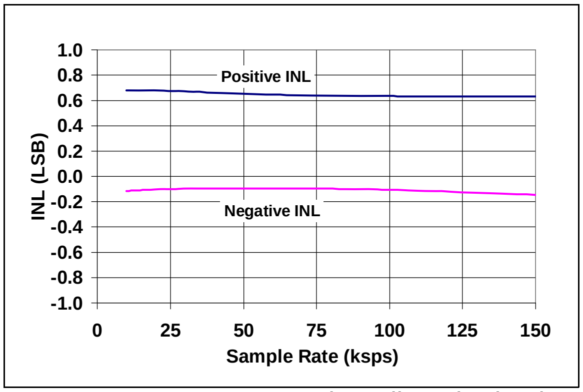


FIGURE 2-1: Integral Nonlinearity (INL) vs. Sample Rate.

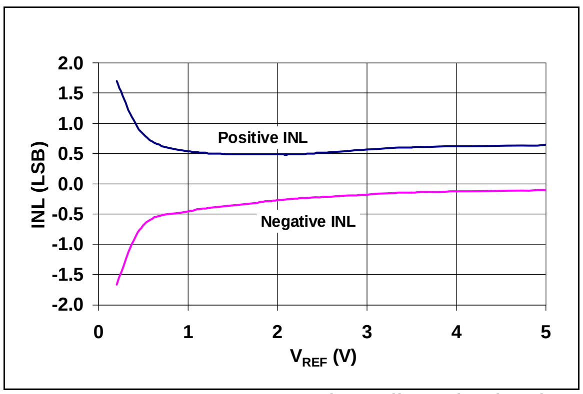


FIGURE 2-2: Integral Nonlinearity (INL) vs. V_{REF}.

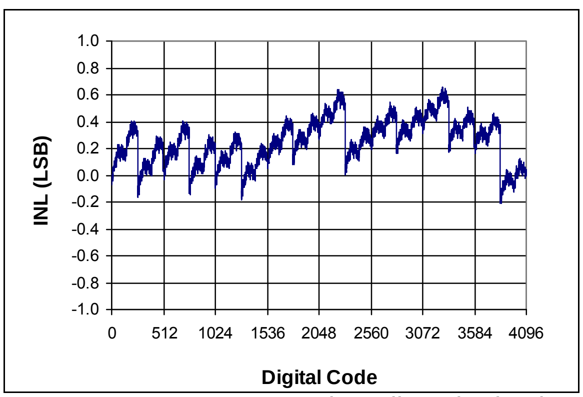


FIGURE 2-3: Integral Nonlinearity (INL) vs. Code (Representative Part).

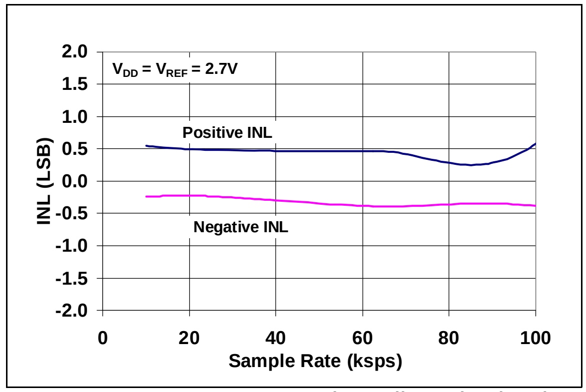


FIGURE 2-4: Integral Nonlinearity (INL) vs. Sample Rate ($V_{DD} = 2.7V$).

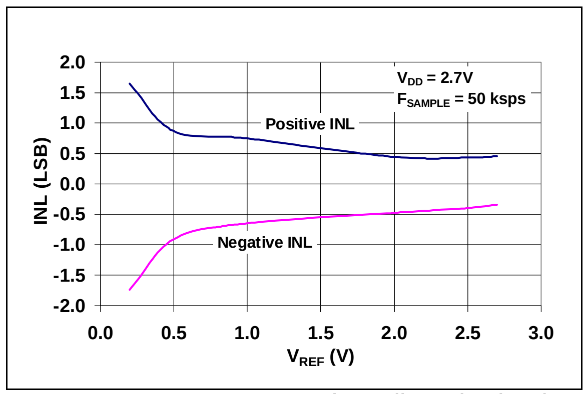


FIGURE 2-5: Integral Nonlinearity (INL) vs. V_{REF} ($V_{DD} = 2.7V$).

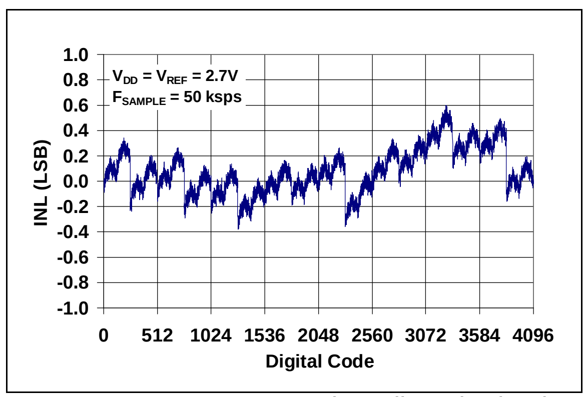


FIGURE 2-6: Integral Nonlinearity (INL) vs. Code (Representative Part, $V_{DD} = 2.7V$).

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = +25°C$.

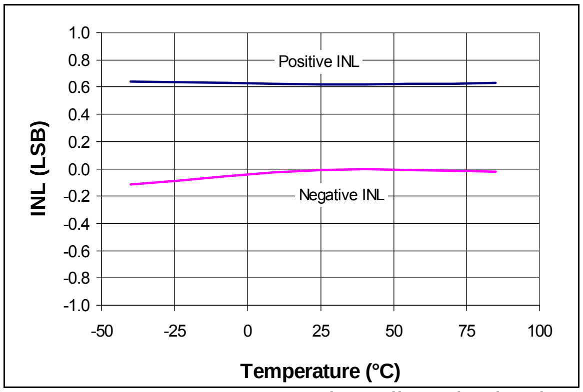


FIGURE 2-7: *Integral Nonlinearity (INL) vs. Temperature.*

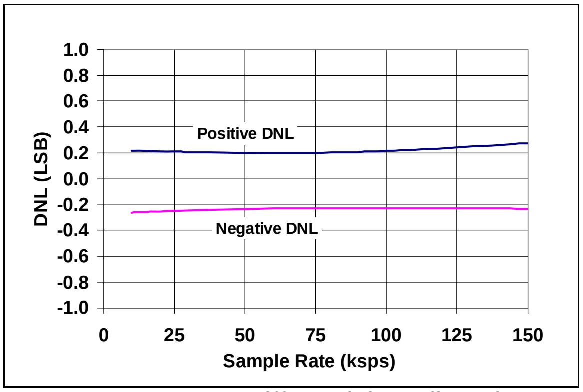


FIGURE 2-8: *Differential Nonlinearity (DNL) vs. Sample Rate.*

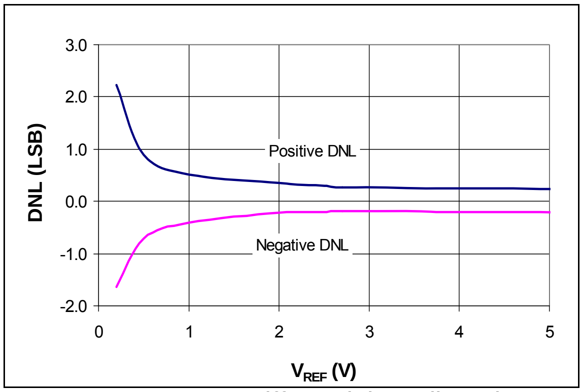


FIGURE 2-9: *Differential Nonlinearity (DNL) vs. V_{REF}*

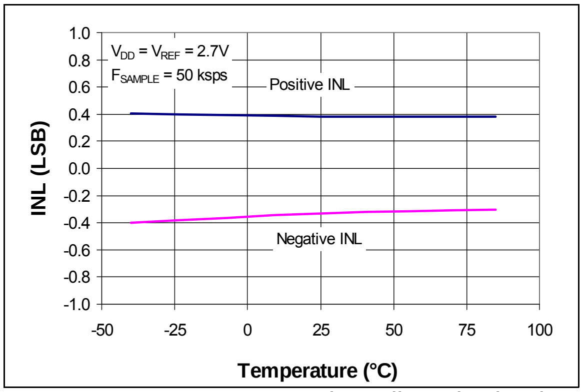


FIGURE 2-10: *Integral Nonlinearity (INL) vs. Temperature (V_{DD} = 2.7V).*

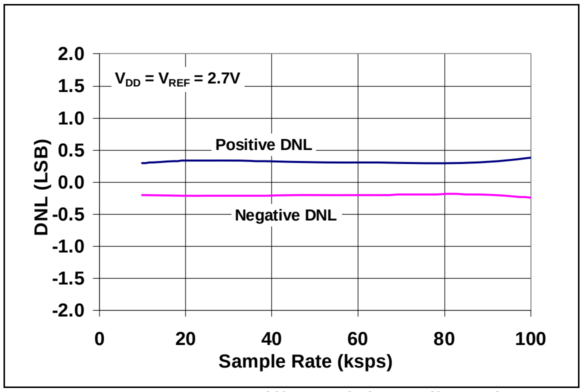


FIGURE 2-11: *Differential Nonlinearity (DNL) vs. Sample Rate (V_{DD} = 2.7V).*

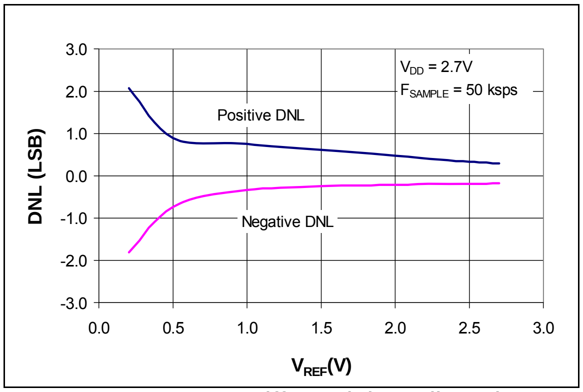


FIGURE 2-12: *Differential Nonlinearity (DNL) vs. V_{REF} (V_{DD} = 2.7V).*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = +25°C$.

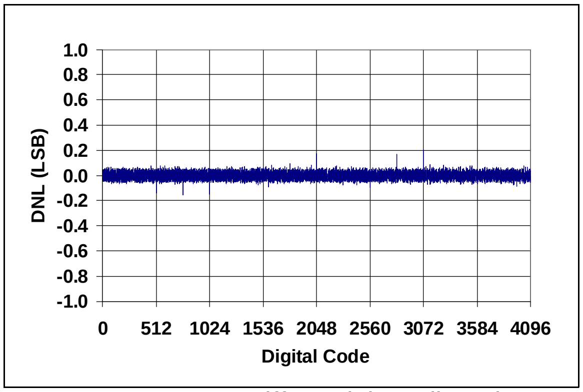


FIGURE 2-13: *Differential Nonlinearity (DNL) vs. Code (Representative Part).*

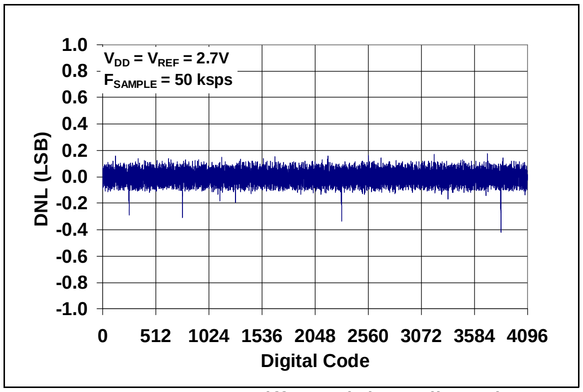


FIGURE 2-16: *Differential Nonlinearity (DNL) vs. Code (Representative Part, $V_{DD} = 2.7V$).*

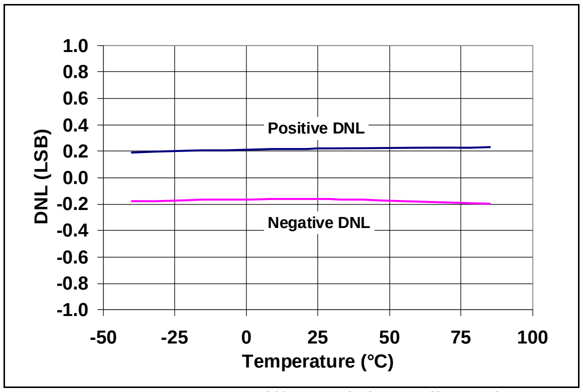


FIGURE 2-14: *Differential Nonlinearity (DNL) vs. Temperature.*

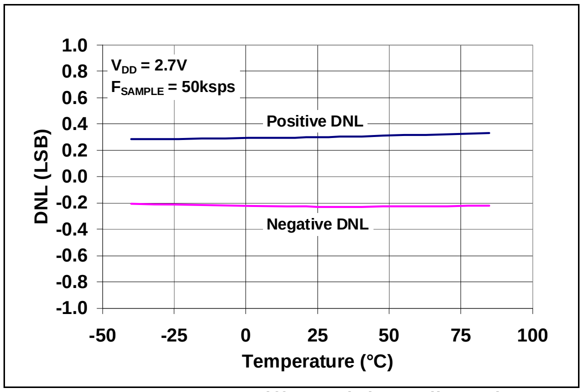


FIGURE 2-17: *Differential Nonlinearity (DNL) vs. Temperature ($V_{DD} = 2.7V$).*

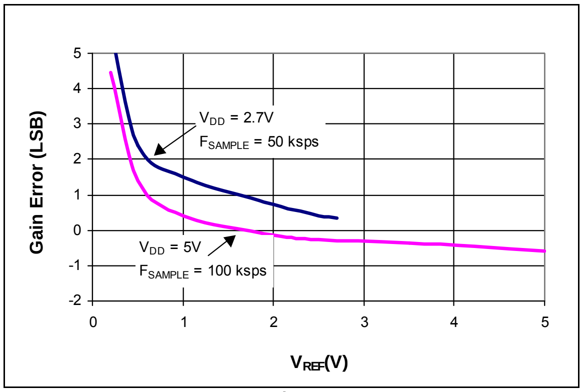


FIGURE 2-15: *Gain Error vs. V_{REF}*

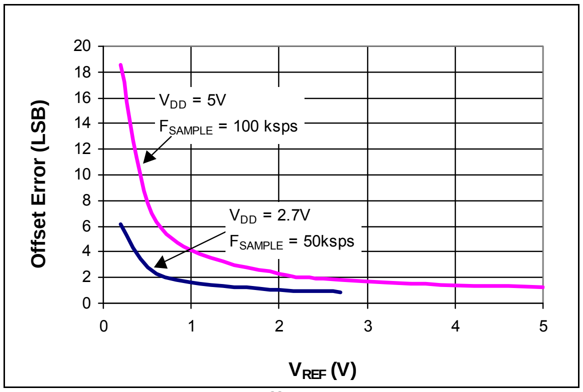


FIGURE 2-18: *Offset Error vs. V_{REF}*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = +25°C$.

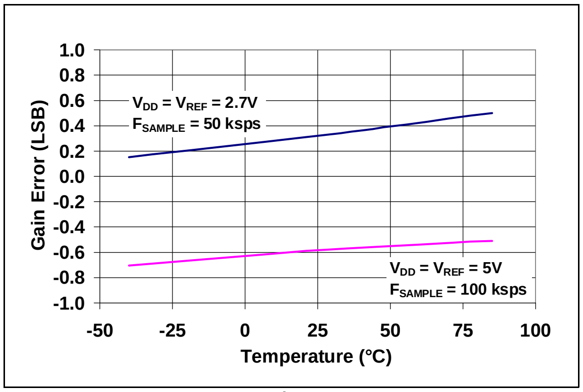


FIGURE 2-19: *Gain Error vs. Temperature.*

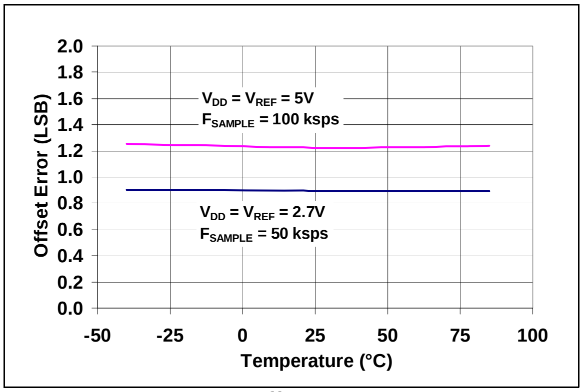


FIGURE 2-22: *Offset Error vs. Temperature.*

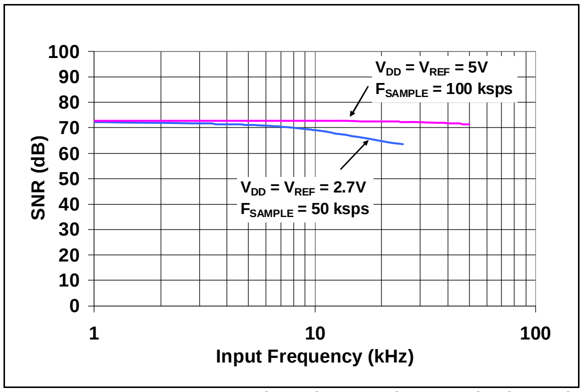


FIGURE 2-20: *Signal-to-Noise Ratio (SNR) vs. Input Frequency.*

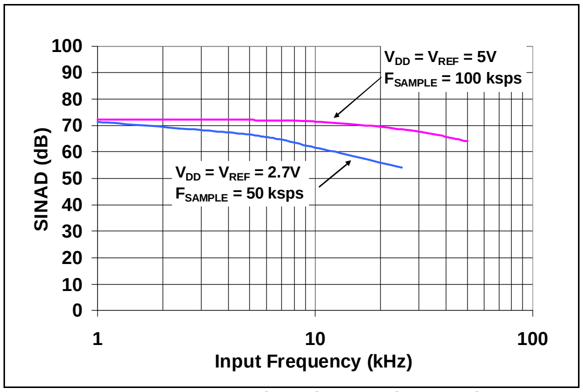


FIGURE 2-23: *Signal-to-Noise and Distortion (SINAD) vs. Input Frequency.*

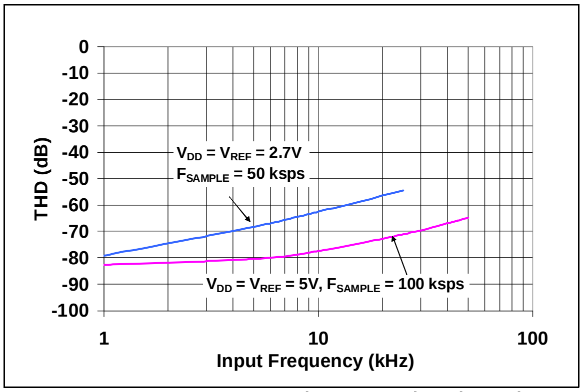


FIGURE 2-21: *Total Harmonic Distortion (THD) vs. Input Frequency.*

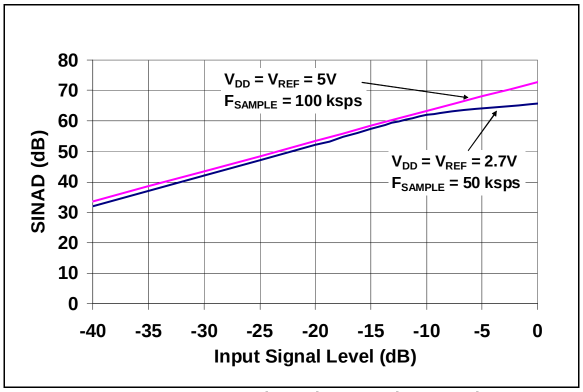


FIGURE 2-24: *Signal-to-Noise and Distortion (SINAD) vs. Input Signal Level.*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = +25°C$.

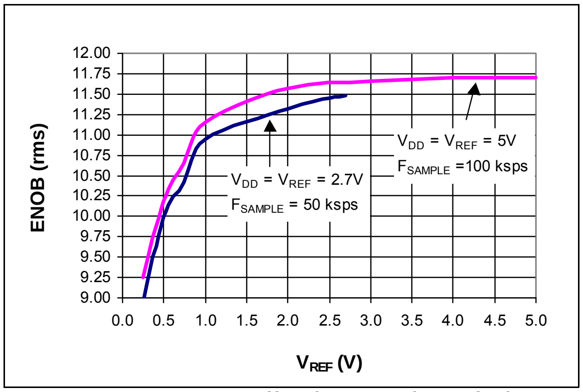


FIGURE 2-25: *Effective Number of Bits (ENOB) vs.* V_{REF}

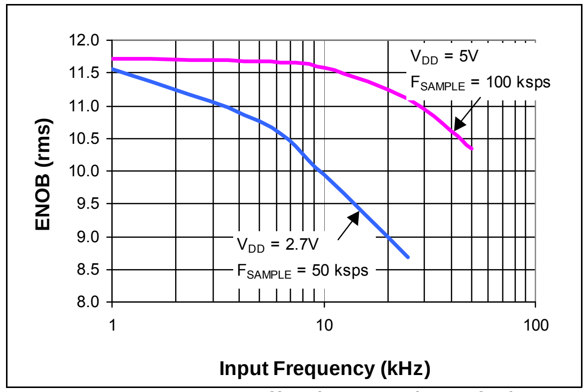


FIGURE 2-28: *Effective Number of Bits (ENOB) vs. Input Frequency.*

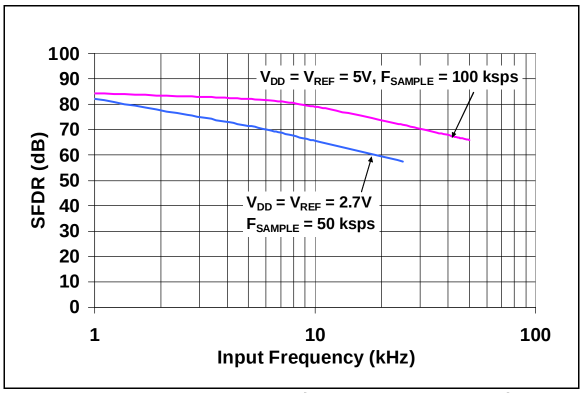


FIGURE 2-26: *Spurious Free Dynamic Range (SFDR) vs. Input Frequency.*

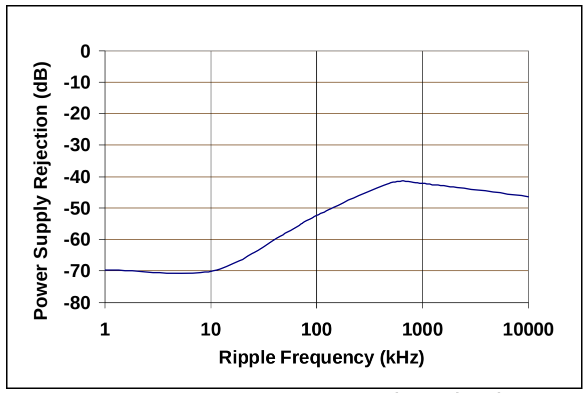


FIGURE 2-29: *Power Supply Rejection (PSR) vs. Ripple Frequency.*

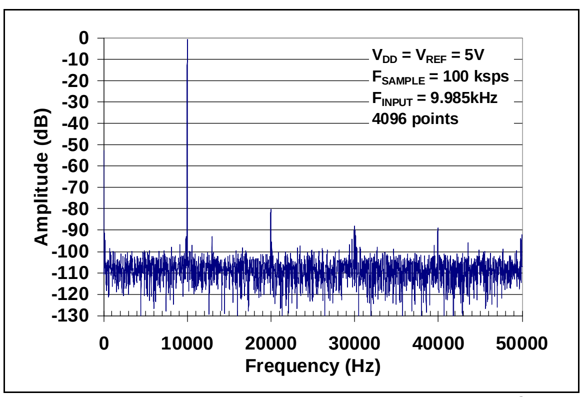


FIGURE 2-27: *Frequency Spectrum of 10 kHz input (Representative Part).*

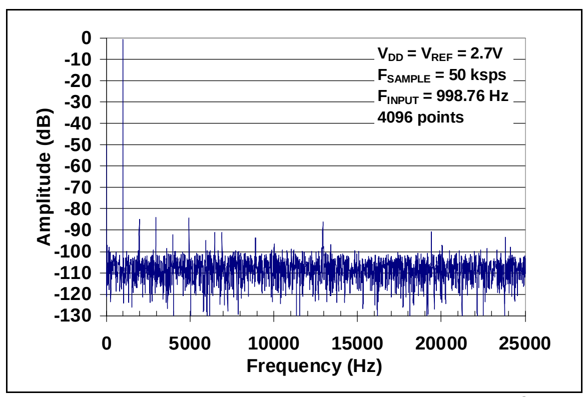


FIGURE 2-30: *Frequency Spectrum of 1 kHz input (Representative Part,* $V_{DD} = 2.7V$*).*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = +25°C$.

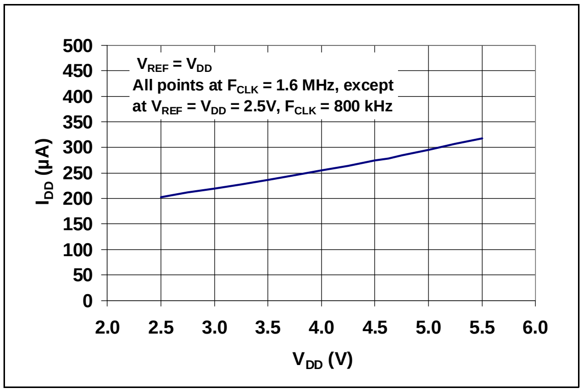


FIGURE 2-31: *I_{DD} vs. V_{DD}.*

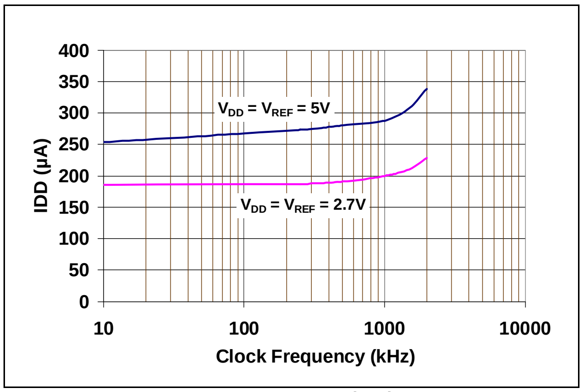


FIGURE 2-32: *I_{DD} vs. Clock Frequency.*

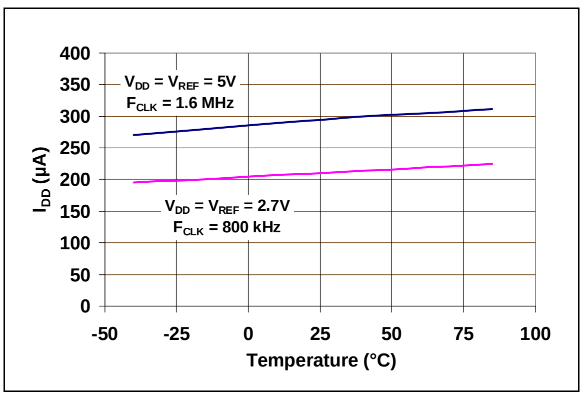


FIGURE 2-33: *I_{DD} vs. Temperature.*

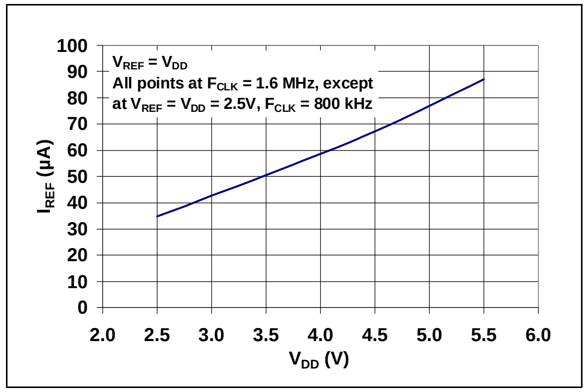


FIGURE 2-34: *I_{REF} vs. V_{DD}.*

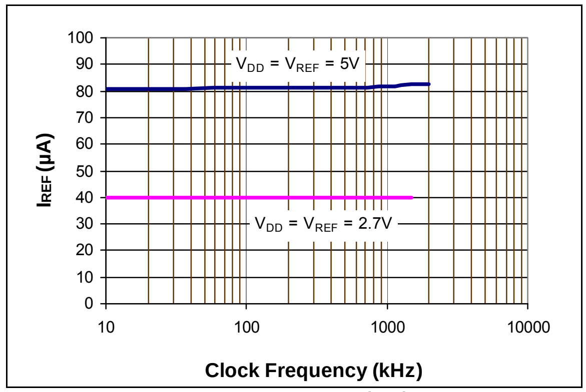


FIGURE 2-35: *I_{REF} vs. Clock Frequency.*

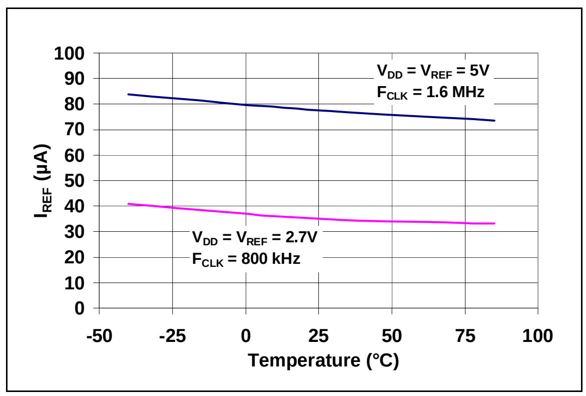


FIGURE 2-36: *I_{REF} vs. Temperature.*

Note: Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 16*f_{SAMPLE}$, $T_A = +25°C$.

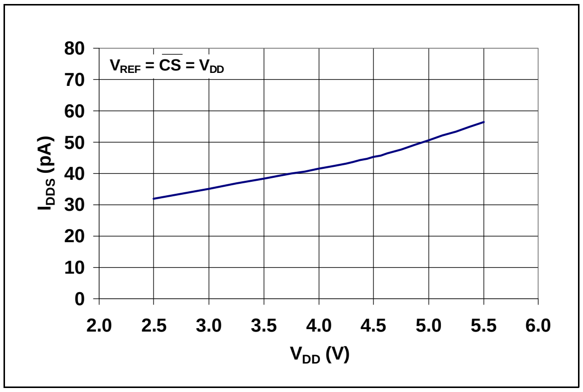


FIGURE 2-37: *I_{DDS} vs. V_{DD}.*

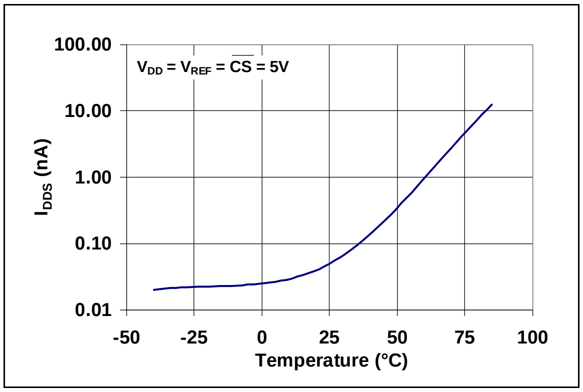


FIGURE 2-38: *I_{DDS} vs. Temperature.*

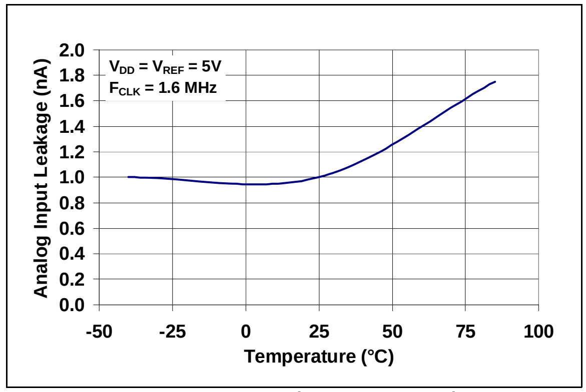


FIGURE 2-39: *Analog Input Leakage Current vs. Temperature.*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

Additional descriptions of the device pins follows.

TABLE 3-1: PIN FUNCTION TABLE

MCP3201 MSOP, PDIP, SOIC, TSSOP	Symbol	Description
1	V_{REF}	Reference Voltage Input
2	IN+	Positive Analog Input
3	IN-	Negative Analog Input
4	V_{SS}	Ground
5	$\overline{CS}$/SHDN	Chip Select/Shutdown Input
6	D_{OUT}	Serial Data Out
7	CLK	Serial Clock
8	V_{DD}	+2.7V to 5.5V Power Supply

3.1 Positive Analog Input (IN+)

Positive analog input. This input can vary from IN- to V_{REF} + IN-.

3.2 Negative Analog Input (IN-)

Negative analog input. This input can vary ±100 mV from V_{SS}.

3.3 Chip Select/Shutdown ($\overline{CS}$/SHDN)

The $\overline{CS}$/SHDN pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The $\overline{CS}$/SHDN pin must be pulled high between conversions.

3.4 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion and to clock out each bit of the conversion as it takes place. See **Section 6.2 "Maintaining Minimum Clock Speed"** for constraints on clock speed.

3.5 Serial Data Output (D_{OUT})

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

NOTES:

4.0 DEVICE OPERATION

The MCP3201 A/D Converter employs a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the first rising edge of the serial clock after $\overline{CS}$ has been pulled low. Following this sample time, the input switch of the converter opens and the device uses the collected charge on the internal sample and hold capacitor to produce a serial 12-bit digital output code. Conversion rates of 100 ksps are possible on the MCP3201 device. See **Section 6.2 "Maintaining Minimum Clock Speed"** for information on minimum clock rates. Communication with the device is done using a 3-wire SPI-compatible interface.

4.1 Analog Inputs

The MCP3201 device provides a single pseudo-differential input. The IN+ input can range from IN- to V_{REF} (V_{REF} + IN-). The IN- input is limited to ±100 mV from the V_{SS} rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

For the A/D Converter to meet specification, the charge holding capacitor (C_{SAMPLE}) must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

In this diagram, it is shown that the source impedance (R_S) adds to the internal sampling switch (R_{SS}) impedance, directly affecting the time that is required to charge the capacitor (C_{SAMPLE}). Consequently, a larger source impedance increases the offset, gain, and integral linearity errors of the conversion.

Ideally, the impedance of the signal source should be near zero. This is achievable with an operational amplifier such as the MCP601, which has a closed loop output impedance of tens of ohms. The adverse affects of higher source impedances are shown in Figure 4-2.

If the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than {[V_{REF} + (IN-)] - 1 LSB}, then the output code will be FFFh. If the voltage level at IN- is more than 1 LSB below V_{SS}, then the voltage level at the IN+ input will have to go below V_{SS} to see the 000h output code. Conversely, if IN- is more than 1 LSB above V_{SS}, then the FFFh code will not be seen unless the IN+ input level goes above V_{REF} level.

4.2 Reference Input

The reference input (V_{REF}) determines the analog input voltage range and the LSB size, as shown below.

EQUATION 4-1:

$$\text{LSB Size} = \frac{V_{REF}}{4096}$$

As the reference input is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D Converter is a function of the analog input signal and the reference input as shown below.

EQUATION 4-2:

$$\text{Digital Output Code} = \frac{4096 * V_{IN}}{V_{REF}}$$

Where:

V_{IN} = Analog Input Voltage = $V(_{IN}+) - V(_{IN}-)$

V_{REF} = Reference Voltage

When using an external voltage reference device, the system designer should always refer to the manufacturer's recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the operation of the A/D Converter.

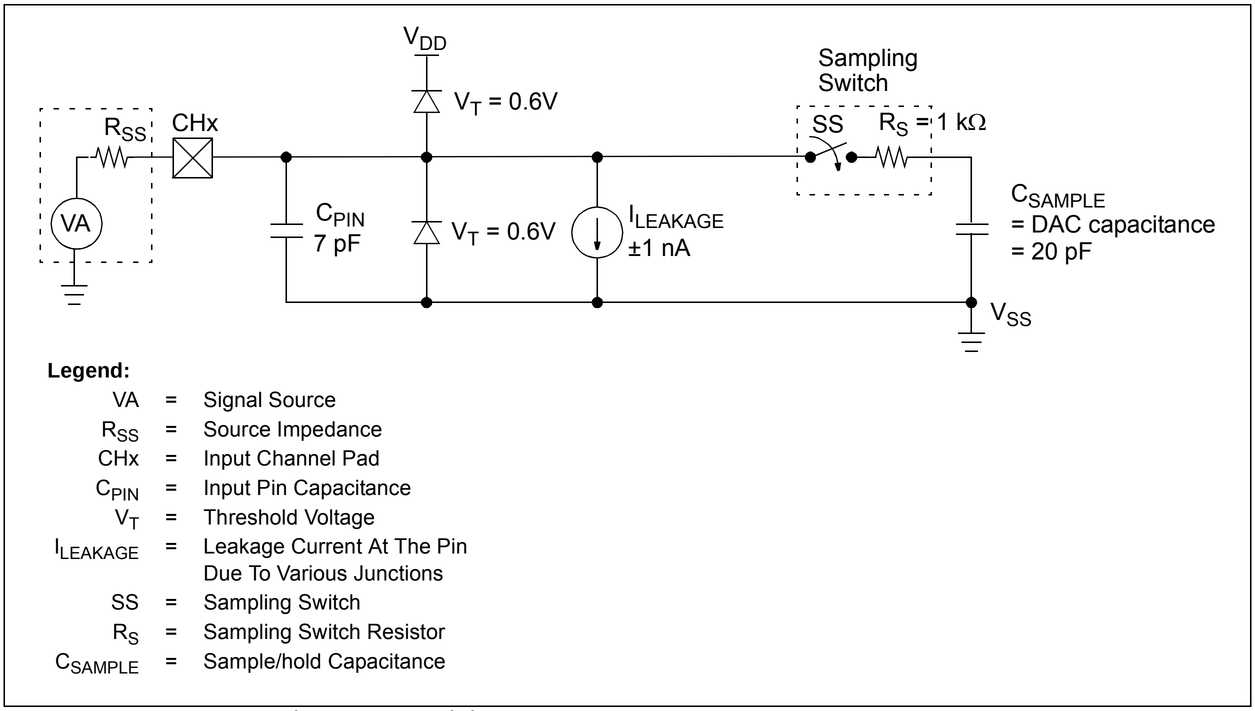


FIGURE 4-1: *Analog Input Model.*

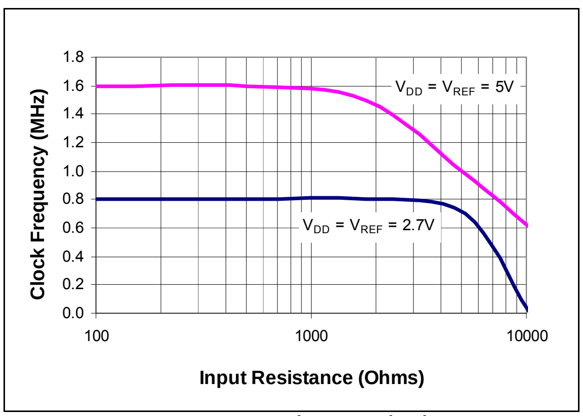
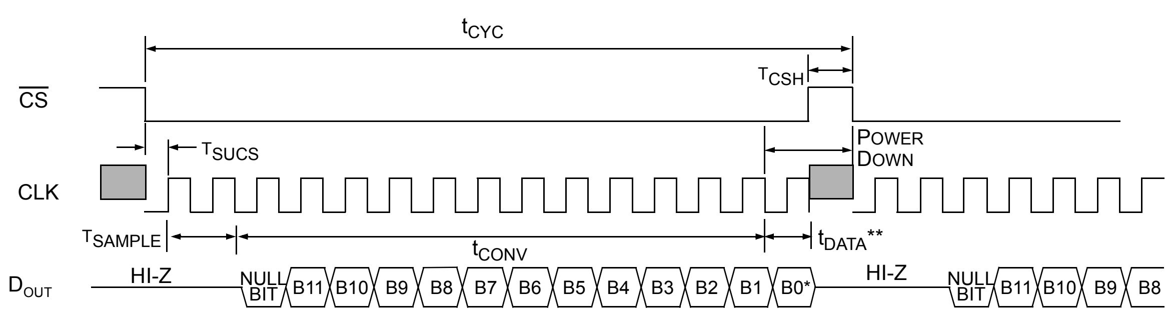


FIGURE 4-2: *Maximum Clock Frequency vs. Input Resistance (R_S) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.*

5.0 SERIAL COMMUNICATIONS

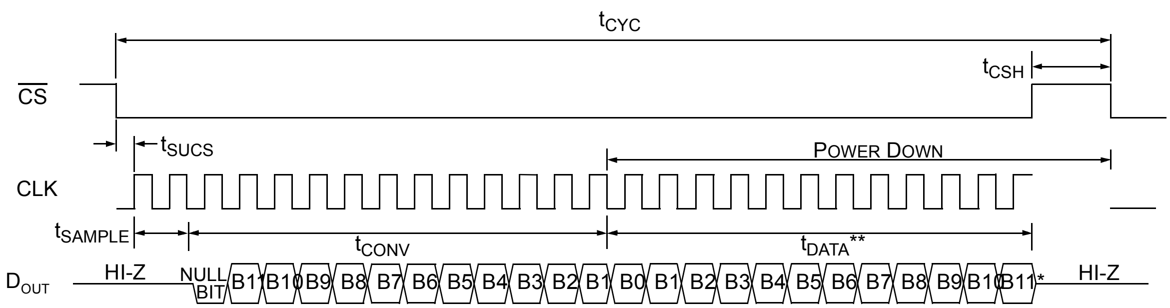
Communication with the device is done using a standard SPI-compatible serial interface. Initiating communication with the MCP3201 device begins with the $\overline{CS}$ going low. If the device was powered up with the $\overline{CS}$ pin low, it must be brought high and back low to initiate communication. The device will begin to sample the analog input on the first rising edge after $\overline{CS}$ goes low. The sample period will end in the falling edge of the second clock, at which time the device will output a low null bit. The next 12 clocks will output the result of the conversion with MSB first, as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the $\overline{CS}$ is held low, the device will output the conversion result LSB first, as shown in Figure 5-2. If more clocks are provided to the device while $\overline{CS}$ is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D Converter will output LSB first data, followed by zeros indefinitely. See Figure 5-2 below.

** t_{DATA}: during this time, the bias current and the comparator power-down and the reference input becomes a high-impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

FIGURE 5-1: *Communication with MCP3201 device using MSB first Format.*



* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D Converter will output zeros indefinitely.

** t_{DATA}: during this time, the bias current and the comparator power-down and the reference input becomes a high-impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

FIGURE 5-2: *Communication with MCP3201 device using LSB first Format.*

NOTES:

6.0 APPLICATIONS INFORMATION

6.1 Using the MCP3201 Device with Microcontroller SPI Ports

With most microcontroller SPI ports, it is required to clock out eight bits at a time. If this is the case, it will be necessary to provide more clocks than are required for the MCP3201. As an example, Figure 6-1 and Figure 6-2 show how the MCP3201 device can be interfaced to a microcontroller with a standard SPI port. Since the MCP3201 always clocks data out on the falling edge of clock, the MCU SPI port must be configured to match this operation. SPI Mode 0,0 (clock idles low) and SPI Mode 1,1 (clock idles high) are both compatible with the MCP3201. Figure 6-1 depicts the operation shown in SPI Mode 0,0, which requires that the CLK from the microcontroller idles in the 'low' state. As shown in the diagram, the MSB is clocked out of the A/D Converter on the falling edge of the third clock pulse. After the first eight clocks have been sent to the device, the microcontroller's receive buffer will contain two unknown bits (the output is at high-impedance for the first two clocks), the null bit and the highest order five bits of the conversion. After the second eight clocks have been sent to the device, the MCU receive register will contain the lowest-order seven bits and the B1 bit repeated as the A/D Converter has begun to shift out LSB first data with the extra clock. Typical procedure would then call for the lower-order byte of data to be shifted right by one bit to remove the extra B1 bit. The B7 bit is then transferred from the high-order byte to the lower-order byte, and then the higher-order byte is shifted one bit to the right as well. Easier manipulation of the converted data can be obtained by using this method.

Figure 6-2 shows the same thing in SPI Mode 1,1 which requires that the clock idles in the high state. As with mode 0,0, the A/D Converter outputs data on the falling edge of the clock and the MCU latches data from the A/D Converter in on the rising edge of the clock.

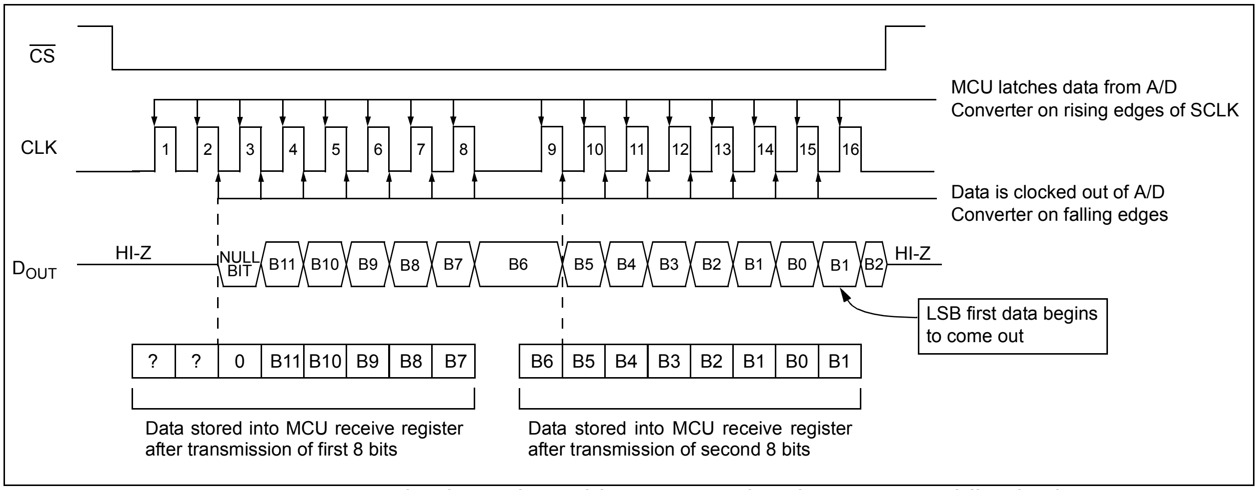


FIGURE 6-1: *SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).*

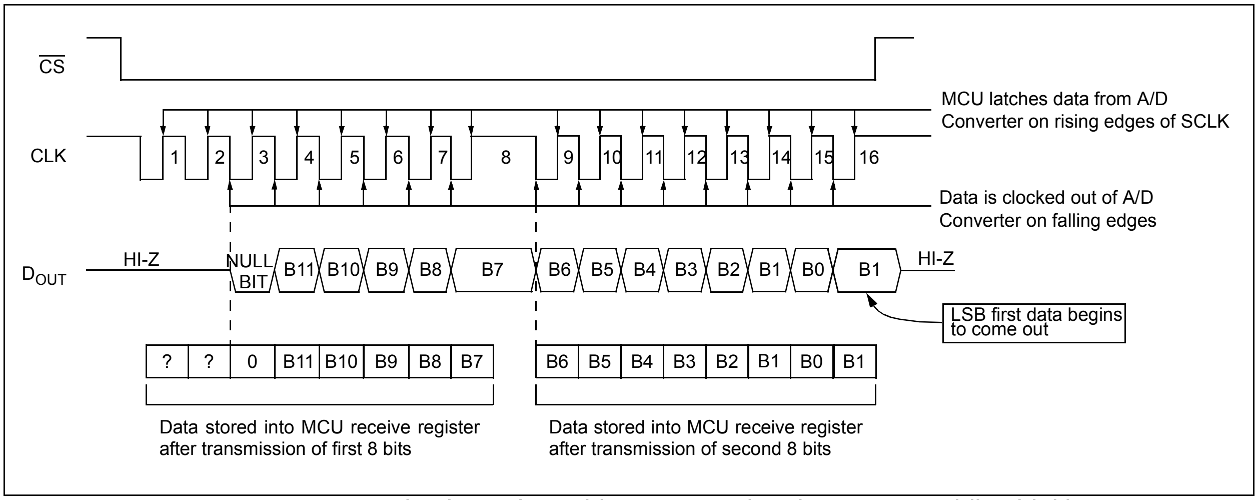


FIGURE 6-2: *SPI Communication using 8-bit segments (Mode 1,1: SCLK idles high).*

6.2 Maintaining Minimum Clock Speed

When the MCP3201 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample cap while the conversion is taking place. At 85°C (worst-case condition), the part will maintain proper charge on the sample capacitor for at least 1.2 ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 12 data bits have been clocked out must not exceed 1.2 ms (effective clock frequency of 10 kHz). Failure to meet this criteria may induce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D Converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D Converter is not a low-impedance source, it will have to be buffered or inaccurate conversion results may occur. See Figure 4-2. It is also recommended that a filter be used to eliminate any signals that may be aliased back into the conversion results. This is illustrated in Figure 6-3 where an op amp is used to drive the analog input of the MCP3201 device. This amplifier provides a low-impedance source for the converter input and a low-pass filter, which eliminates unwanted high-frequency noise.

Low-pass (anti-aliasing) filters can be designed using Microchip's interactive FilterLab® software. FilterLab will calculate capacitor and resistor values, as well as determine the number of poles that are required for the application. For more information on filtering signals, see application note AN699 *"Anti-Aliasing Analog Filters for Data Acquisition Systems."*

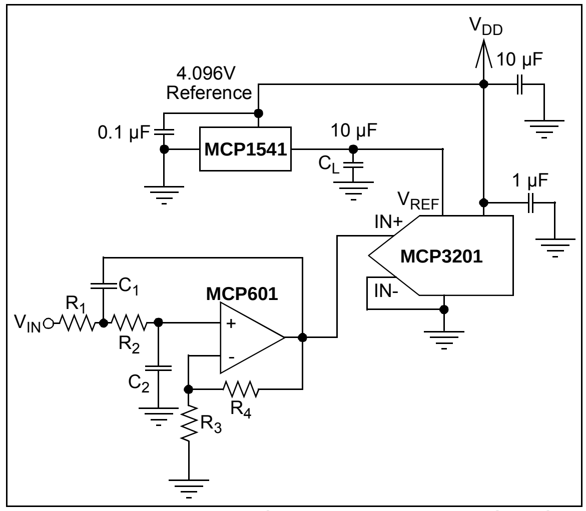


FIGURE 6-3: *The MCP601 Operational Amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3201 device.*

6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 1 µF is recommended.

Digital and analog traces should be separated as much as possible on the board and no traces should run underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high-frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V_{DD} connections to devices in a “star” configuration can also reduce noise by eliminating current return paths and associated errors. See Figure 6-4. For more information on layout tips when using A/D Converter, refer to AN688 *“Layout Tips for 12-Bit A/D Converter Applications”*.

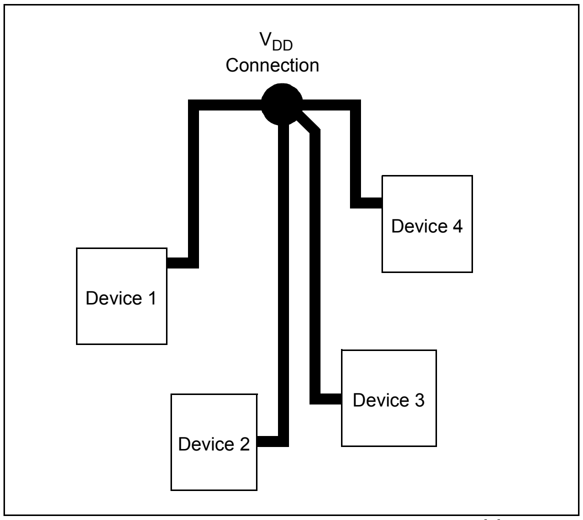


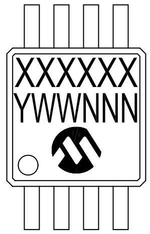
FIGURE 6-4: *V_{DD} traces arranged in a ‘Star’ configuration in order to reduce errors caused by current return paths.*

NOTES:

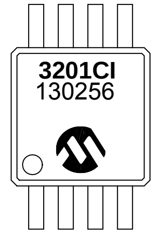
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

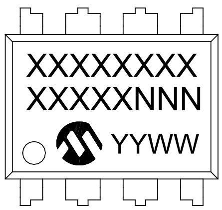
8-Lead MSOP (3x3 mm)



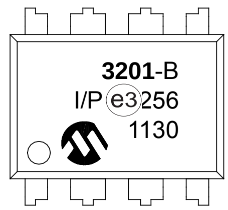
Example



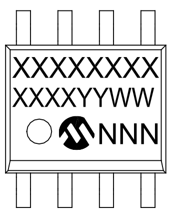
8-Lead PDIP (300 mil)



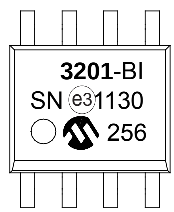
Example



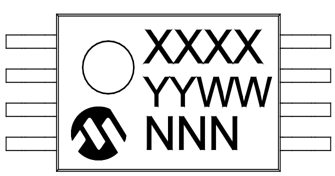
8-Lead SOIC (3.90 mm)



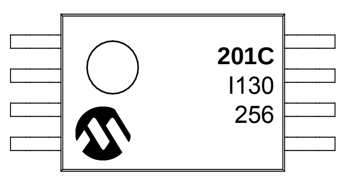
Example



8-Lead TSSOP (4.4 mm)



Example

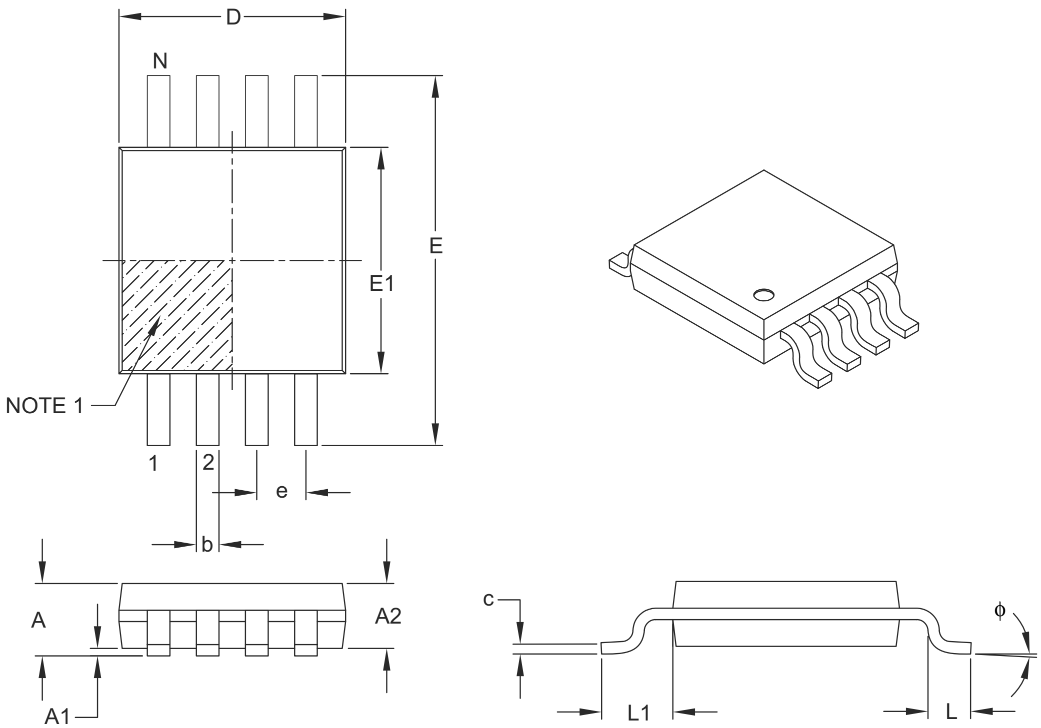


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

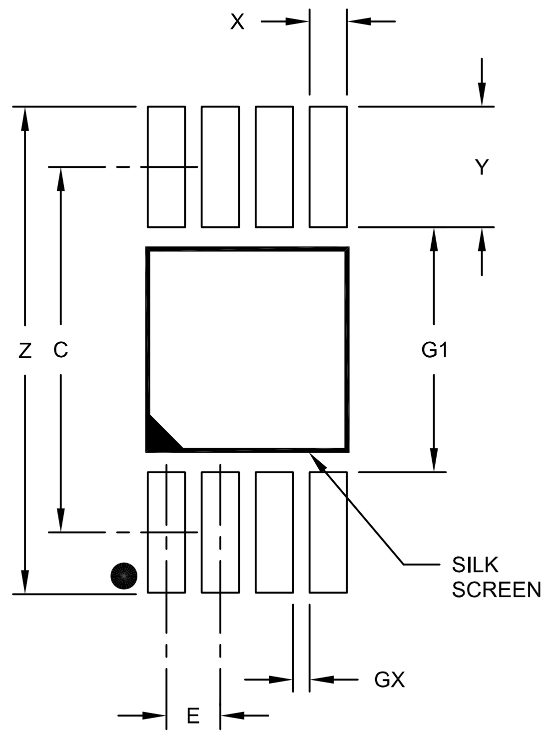
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

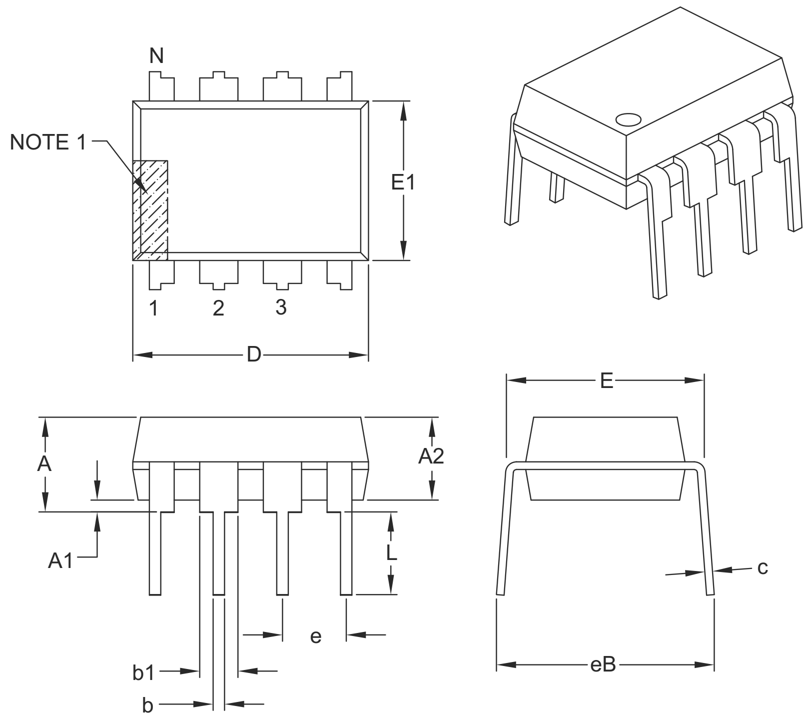
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

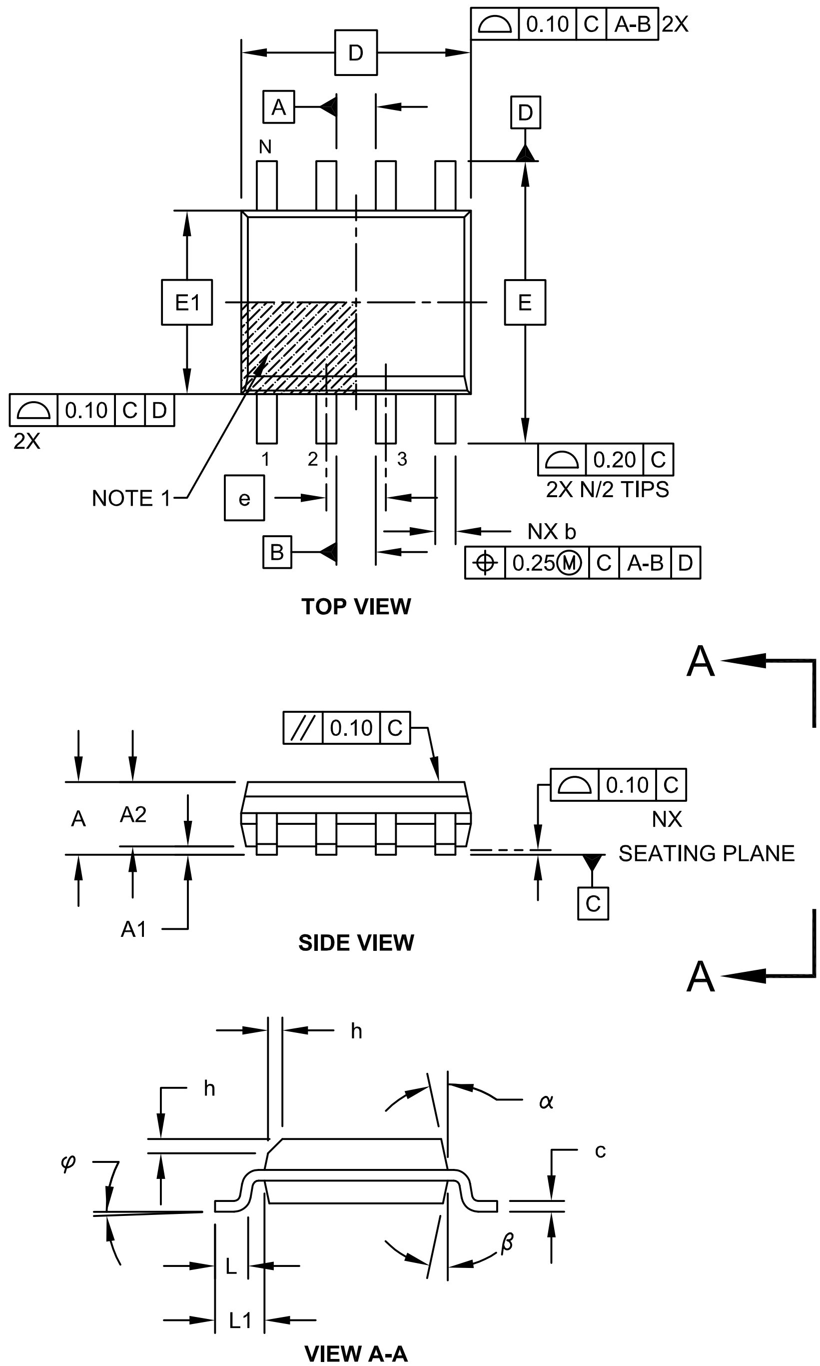
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

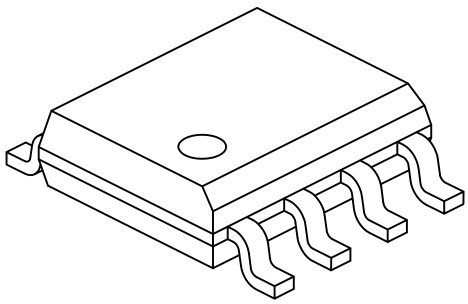
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

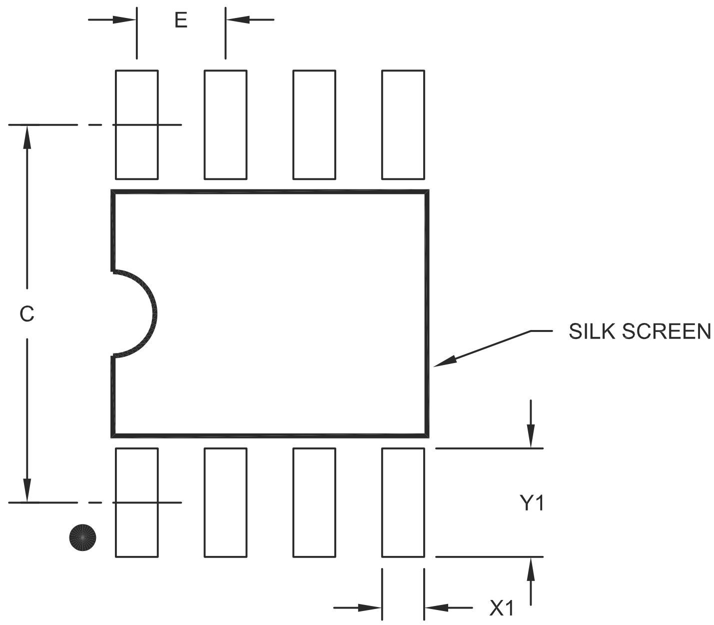
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

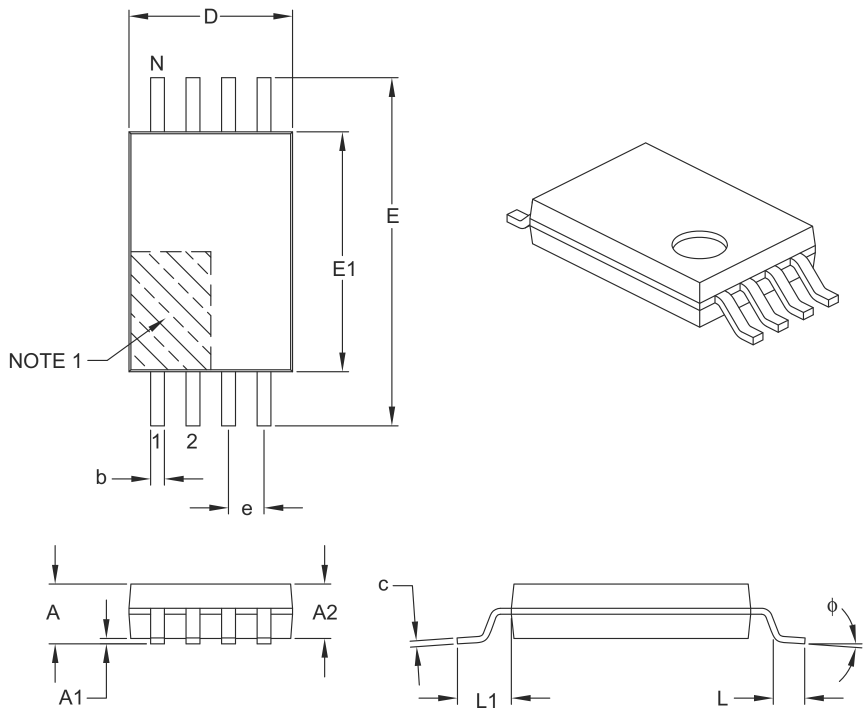
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Number of Pins	N			8	
Pitch	e			0.65 BSC	
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.80	1.00	1.05
Standoff	A1		0.05	–	0.15
Overall Width	E			6.40 BSC	
Molded Package Width	E1		4.30	4.40	4.50
Molded Package Length	D		2.90	3.00	3.10
Foot Length	L		0.45	0.60	0.75
Footprint	L1			1.00 REF	
Foot Angle	ϕ		0°	–	8°
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

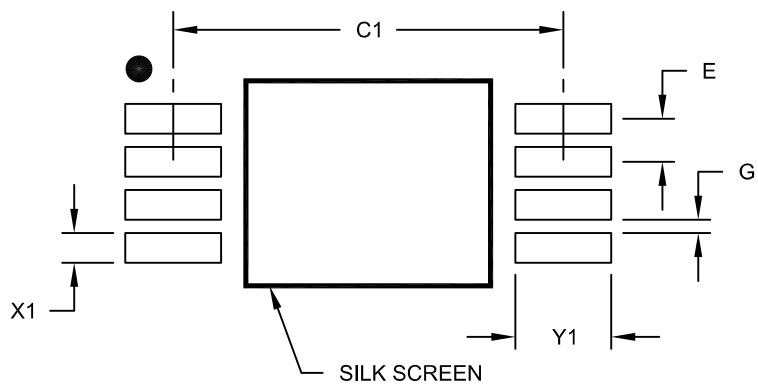
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

NOTES:

APPENDIX A: REVISION HISTORY

Revision F (August 2011)

- Updated **Product Identification System** section.
  - Corrected marking drawings for MSOP packages.
  - Updated PDIP, SOIC, and TSSOP package specification drawings.

Revision E (November 2008)

The following is the list of modifications:

1. Updated **Section 7.0 “Packaging Information”.**
2. Updated **Product Identification System** section.

Revision D (January 2007)

The following is the list of modifications:

1. This revision includes updates to the packaging diagrams.

Revision C (August 2001)

The following is the list of modifications:

1. This revision includes undocumented changes.

Revision B (August 1999)

The following is the list of modifications:

1. This revision includes undocumented changes.

Revision A (September 1998)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	/XX
Device	Grade	Temperature Range	Package

Device:	MCP3201:	12-Bit A/D Converter w/SPI Interface
	MCP3201T:	12-Bit A/D Converter w/SPI Interface (Tape and Reel)
Grade:	B:	= ± LSB max INL (MSOP and TSSOP not available)
	C:	= ± LSB max INL
Temperature Range:	I	= -40°C to+85°C(Industrial)
Package:	MS	= Plastic Micro Small Outline (MSOP), 8-lead
	P	= Plastic DIP (300 mil Body), 8-lead
	SN	= Plastic SOIC (150 mil Body), 8-lead
	ST	= Plastic TSSOP (4.4 mm), 8-lead

Examples:

a) MCP3201-BI/P: B Grade, Industrial Temperature, 8LD PDIP package.

b) MCP3201-BI/SN: B Grade, Industrial Temperature, 8LD SOIC package.

c) MCP3201-CI/P: C Grade, Industrial Temperature, 8LD PDIP package.

d) MCP3201-CI/MS: C Grade, Industrial Temperature, 8LD MSOP package.

e) MCP3201-CI/SN: C Grade, Industrial Temperature, 8LD SOIC package.

f) MCP3201-CI/ST: C Grade, Industrial Temperature, 8LD TSSOP package.

g) MCP3201T-BI/SN: Tape and Reel, B Grade, Industrial Temperature, 8LD SOIC package.

h) MCP3201T-CI/MS: Tape and Reel, C Grade, Industrial Temperature, 8LD MSOP package.

i) MCP3201T-CI/SN: Tape and Reel, C Grade, Industrial Temperature, 8LD SOIC package.

j) MCP3201T-CI/ST: Tape and Reel, C Grade, Industrial Temperature, 8LD TSSOP package.

NOTES:

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Printed on recycled paper.

ISBN: 978-1-61341-572-6

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