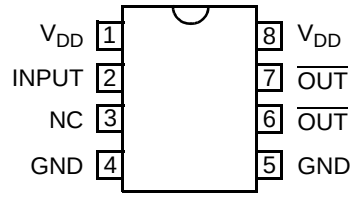
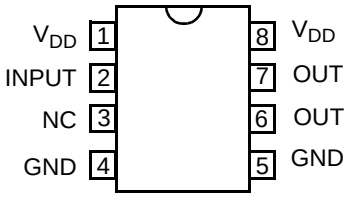
## Package Types

### 8-Pin PDIP/SOIC

**MCP1406**

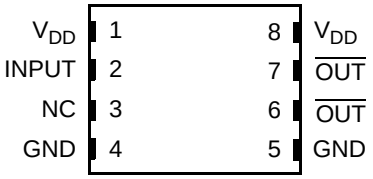



**MCP1407**

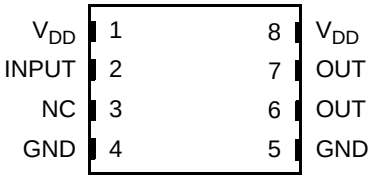



### 8-Pin 6x5 DFN

**MCP1406**

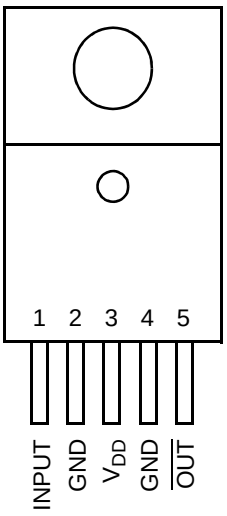



**MCP1407**



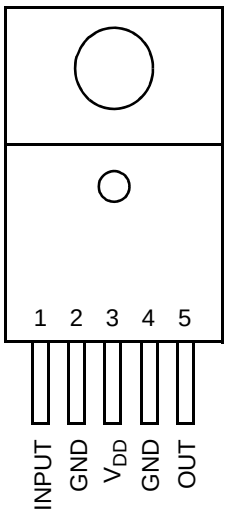

### 5-Pin TO-220

**MCP1406**




Tab is common to $V_{DD}$

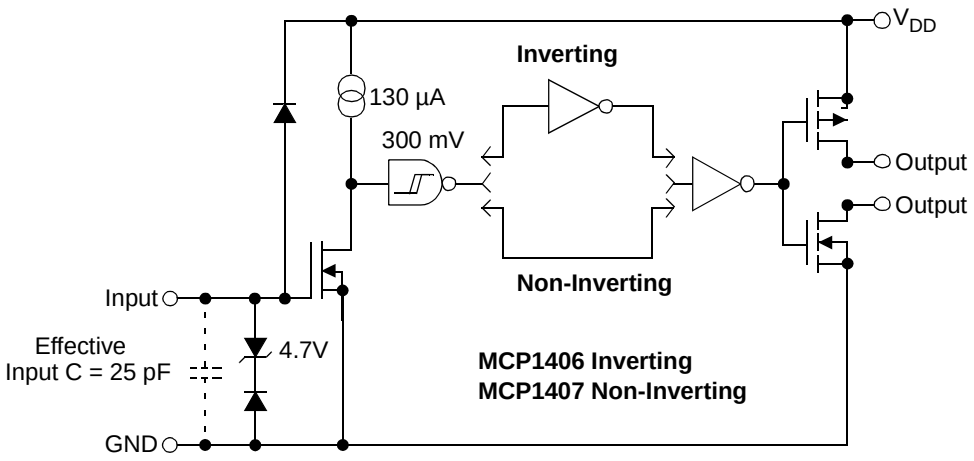
**MCP1407**




**Note 1:** Duplicate pins must both be connected for proper operation.

**2:** Exposed pad of the DFN package is electrically isolated.

## Functional Block Diagram(1)




**Note 1:** Unused inputs should be grounded.

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage .....+20V
Input Voltage .....($V_{DD}$ + 0.3V) to (GND – 5V)
Input Current ($V_{IN}$>$V_{DD}$).....50 mA

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, $T_A$ = +25°C, with 4.5V ≤ $V_{DD}$ ≤ 18V.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| Logic '1', High Input Voltage | $V_{IH}$ | 2.4 | 1.8 | — | V | |
| Logic '0', Low Input Voltage | $V_{IL}$ | — | 1.3 | 0.8 | V | |
| Input Current | $I_{IN}$ | –10 | — | 10 | µA | 0V ≤ $V_{IN}$ ≤ $V_{DD}$ |
| Input Voltage | $V_{IN}$ | -5 | — | $V_{DD}$+0.3 | V | |
| **Output** | | | | | | |
| High Output Voltage | $V_{OH}$ | $V_{DD}$ – 0.025 | — | — | V | DC Test |
| Low Output Voltage | $V_{OL}$ | — | — | 0.025 | V | DC Test |
| Output Resistance, High | $R_{OH}$ | — | 2.1 | 2.8 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| Output Resistance, Low | $R_{OL}$ | — | 1.5 | 2.5 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| Peak Output Current | $I_{PK}$ | — | 6 | — | A | $V_{DD}$ = 18V **(Note 2)** |
| Continuous Output Current | $I_{DC}$ | 1.3 | | | A | **Note 2**, **Note 3** |
| Latch-Up Protection Withstand Reverse Current | $I_{REV}$ | — | 1.5 | — | A | Duty cycle ≤ 2%, t ≤ 300 µsec. |
| **Switching Time (Note 1)** | | | | | | |
| Rise Time | $t_R$ | — | 20 | 30 | ns | **Figure 4-1**, **Figure 4-2** $C_L$ = 2500 pF |
| Fall Time | $t_F$ | — | 20 | 30 | ns | **Figure 4-1**, **Figure 4-2** $C_L$ = 2500 pF |
| Delay Time | $t_{D1}$ | — | 40 | 55 | ns | **Figure 4-1**, **Figure 4-2** |
| Delay Time | $t_{D2}$ | — | 40 | 55 | ns | **Figure 4-1**, **Figure 4-2** |
| **Power Supply** | | | | | | |
| Supply Voltage | $V_{DD}$ | 4.5 | — | 18.0 | V | |
| Power Supply Current | $I_S$ | — | 130 | 250 | µA | $V_{IN}$ = 3V |
| | $I_S$ | — | 35 | 100 | µA | $V_{IN}$ = 0V |

**Note 1:** Switching times ensured by design.
**2:** Tested during characterization, not production tested.
**3:** Valid for AT and MF packages only. $T_A$ = +25°C

## DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

| **Electrical Specifications:** Unless otherwise indicated, operating temperature range with 4.5V ≤ $V_{DD}$ ≤ 18V. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Input** | | | | | | |
| Logic '1', High Input Voltage | $V_{IH}$ | 2.4 | — | — | V | |
| Logic '0', Low Input Voltage | $V_{IL}$ | — | — | 0.8 | V | |
| Input Current | $I_{IN}$ | –10 | — | +10 | µA | 0V ≤ $V_{IN}$ ≤ $V_{DD}$ |
| Input Voltage | $V_{IN}$ | -5 | — | $V_{DD}$+0.3 | V | |
| **Output** | | | | | | |
| High Output Voltage | $V_{OH}$ | $V_{DD}$ – 0.025 | — | — | V | DC TEST |
| Low Output Voltage | $V_{OL}$ | — | — | 0.025 | V | DC TEST |
| Output Resistance, High | $R_{OH}$ | — | 3.0 | 5.0 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| Output Resistance, Low | $R_{OL}$ | — | 2.3 | 5.0 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| **Switching Time (Note 1)** | | | | | | |
| Rise Time | $t_R$ | — | 25 | 40 | ns | **Figure 4-1**, **Figure 4-2** $C_L$ = 2500 pF |
| Fall Time | $t_F$ | — | 25 | 40 | ns | **Figure 4-1**, **Figure 4-2** $C_L$ = 2500 pF |
| Delay Time | $t_{D1}$ | — | 50 | 65 | ns | **Figure 4-1**, **Figure 4-2** |
| Delay Time | $t_{D2}$ | — | 50 | 65 | ns | **Figure 4-1**, **Figure 4-2** |
| **Power Supply** | | | | | | |
| Supply Voltage | $V_{DD}$ | 4.5 | — | 18.0 | V | |
| Power Supply Current | $I_S$ | — | 200 | 500 | µA | $V_{IN}$ = 3V |
| | | — | 50 | 150 | | $V_{IN}$ = 0V |

**Note 1:** Switching times ensured by design.

## TEMPERATURE CHARACTERISTICS

| **Electrical Specifications:** Unless otherwise noted, all parameters apply with 4.5V ≤ $V_{DD}$ ≤ 18V. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | –40 | — | +125 | °C | |
| Maximum Junction Temperature | $T_J$ | — | — | +150 | °C | |
| Storage Temperature Range | $T_A$ | –65 | — | +150 | °C | |
| **Package Thermal Resistances** | | | | | | |
| Thermal Resistance, 8L-6x5 DFN | $\theta_{JA}$ | — | 33.2 | — | °C/W | Typical four-layer board with vias to ground plane |
| Thermal Resistance, 8L-PDIP | $\theta_{JA}$ | — | 125 | — | °C/W | |
| Thermal Resistance, 8L-SOIC | $\theta_{JA}$ | — | 155 | — | °C/W | |
| Thermal Resistance, 5L-TO-220 | $\theta_{JA}$ | — | 71 | — | °C/W | |

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V <= $V_{DD}$ <= 18V.

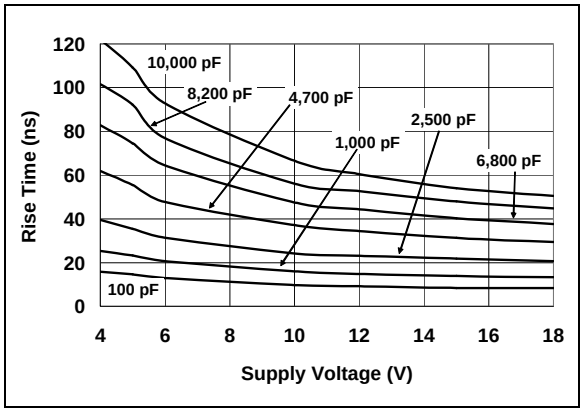



***FIGURE 2-1:*** *Rise Time vs. Supply Voltage.*

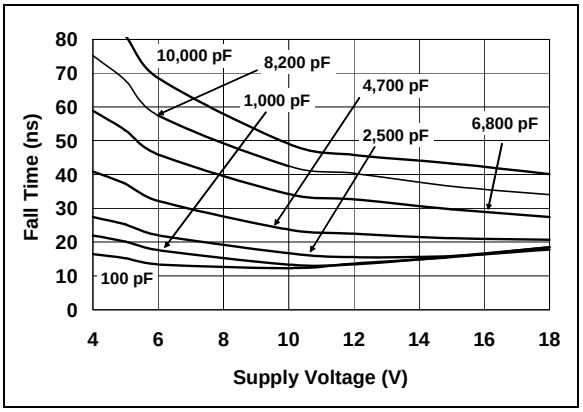



***FIGURE 2-4:*** *Fall Time vs. Supply Voltage.*

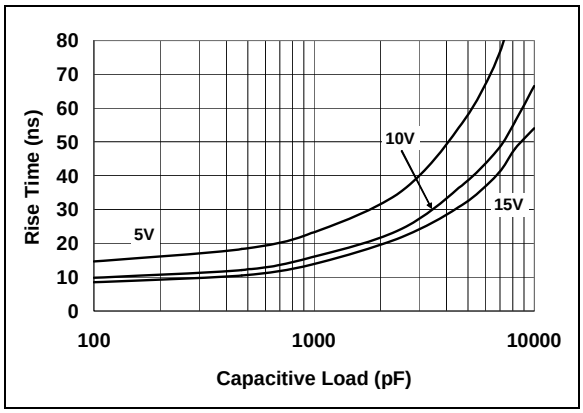



***FIGURE 2-2:*** *Rise Time vs. Capacitive Load.*

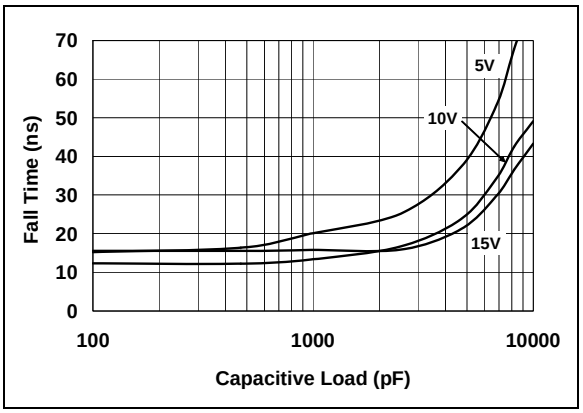



***FIGURE 2-5:*** *Fall Time vs. Capacitive Load.*

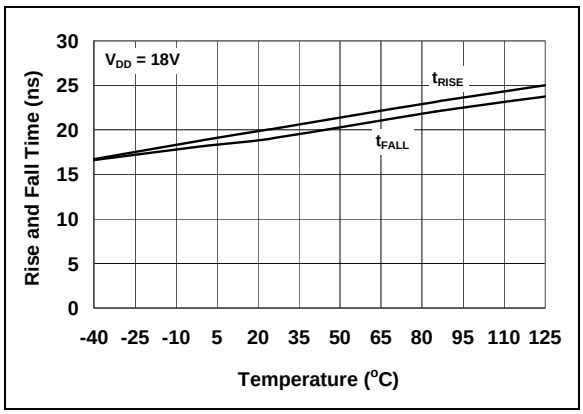



***FIGURE 2-3:*** *Rise and Fall Times vs. Temperature.*

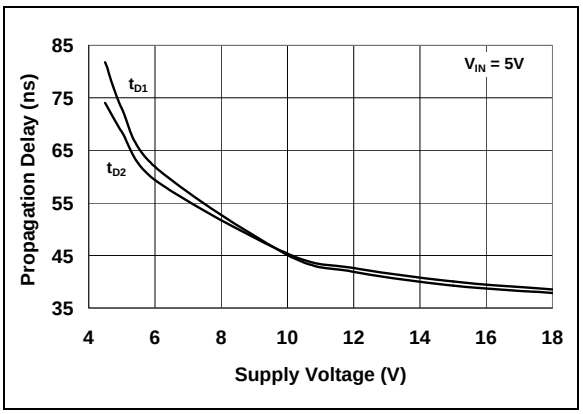



***FIGURE 2-6:*** *Propagation Delay vs. Supply Voltage.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V <= $V_{DD}$ <= 18V.

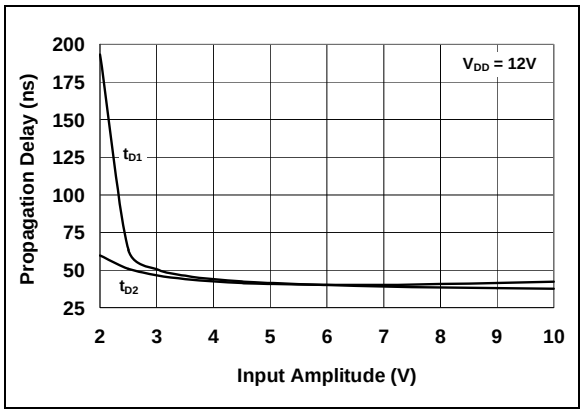



***FIGURE 2-7:*** *Propagation Delay Time vs. Input Amplitude.*

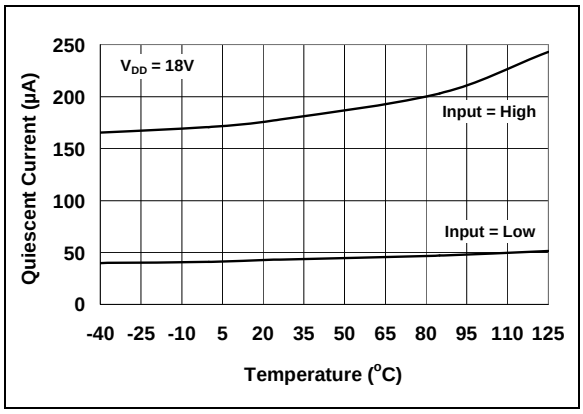



***FIGURE 2-10:*** *Quiescent Current vs. Temperature.*

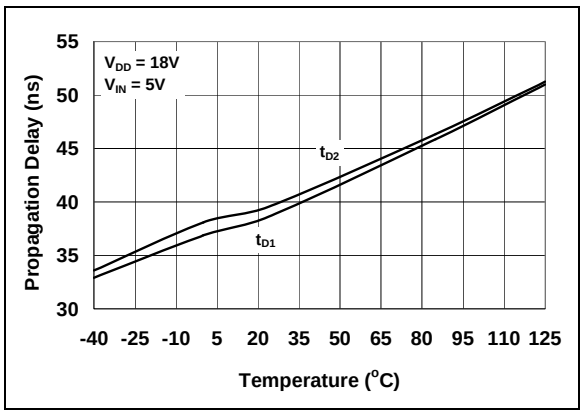



***FIGURE 2-8:*** *Propagation Delay Time vs. Temperature.*

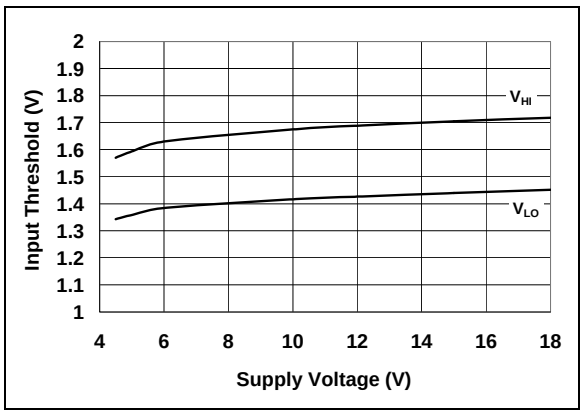



***FIGURE 2-11:*** *Input Threshold vs. Supply Voltage.*

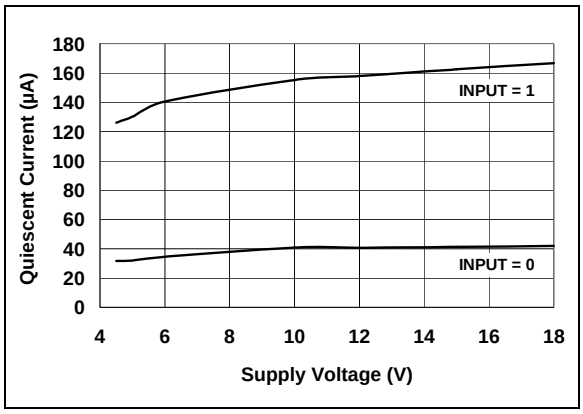



***FIGURE 2-9:*** *Quiescent Current vs. Supply Voltage.*

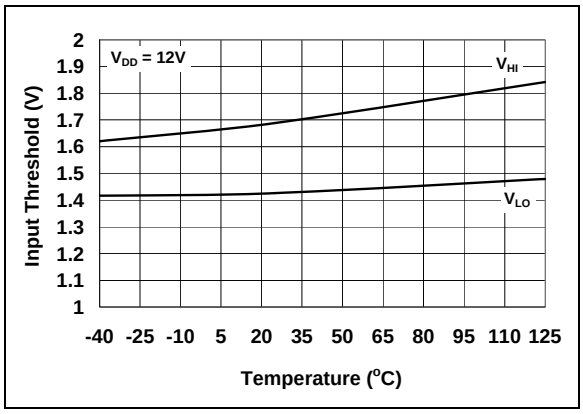



***FIGURE 2-12:*** *Input Threshold vs. Temperature.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V <= $V_{DD}$ <= 18V.

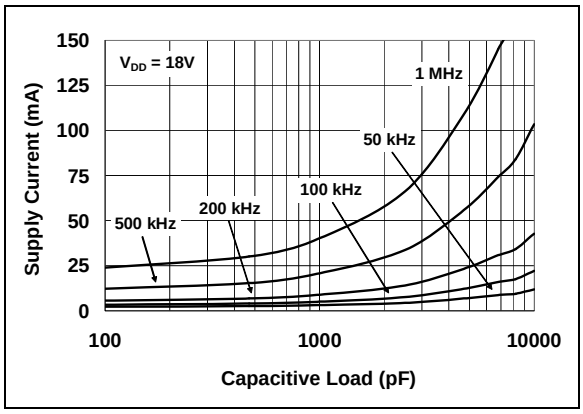



***FIGURE 2-13:*** *Supply Current vs. Capacitive Load.*

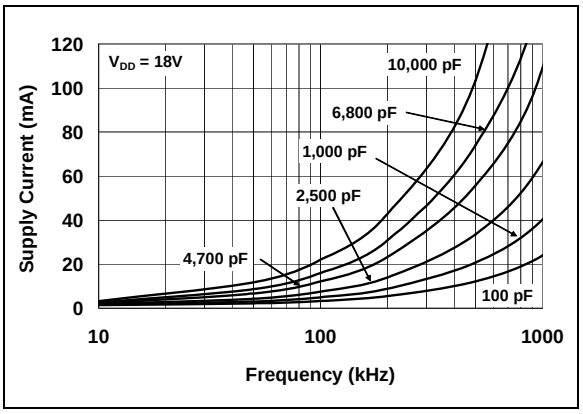



***FIGURE 2-16:*** *Supply Current vs. Frequency.*

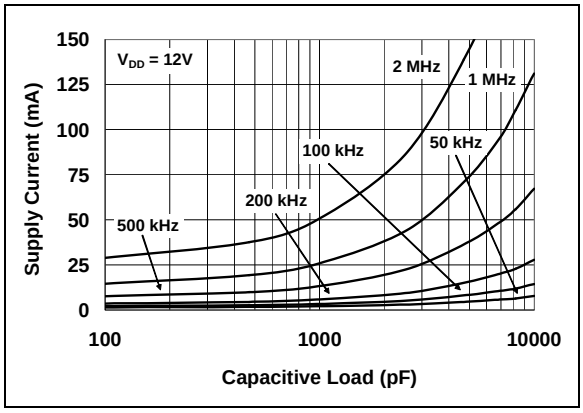



***FIGURE 2-14:*** *Supply Current vs. Capacitive Load.*

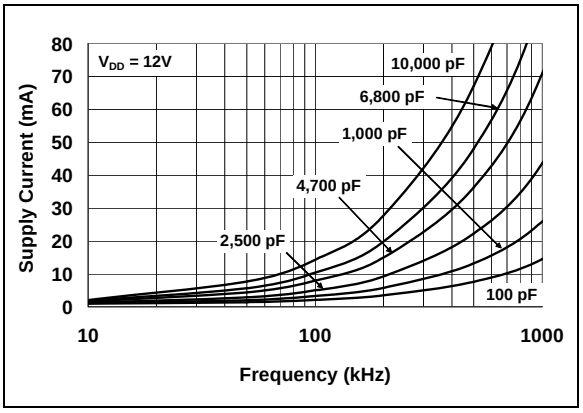



***FIGURE 2-17:*** *Supply Current vs. Frequency.*

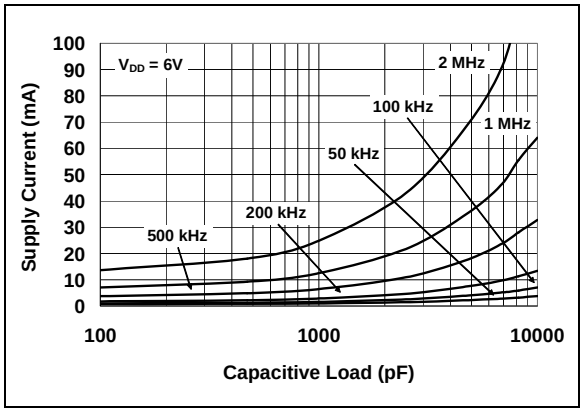



***FIGURE 2-15:*** *Supply Current vs. Capacitive Load.*

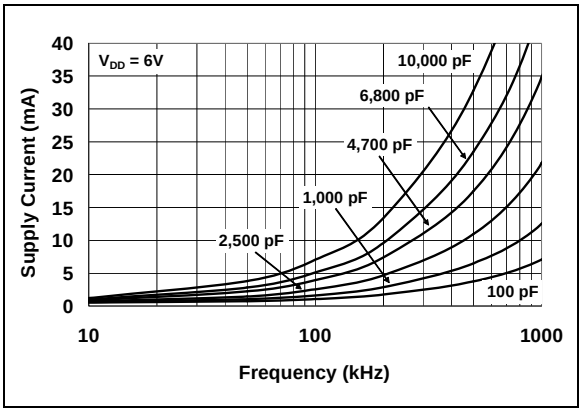



***FIGURE 2-18:*** *Supply Current vs. Frequency.*

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V <= $V_{DD}$ <= 18V.

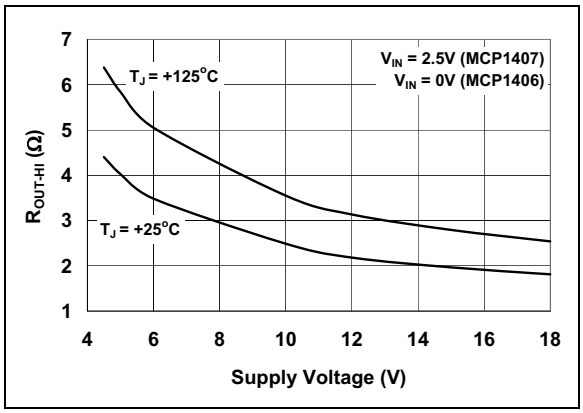



***FIGURE 2-19:*** *Output Resistance (Output High) vs. Supply Voltage.*

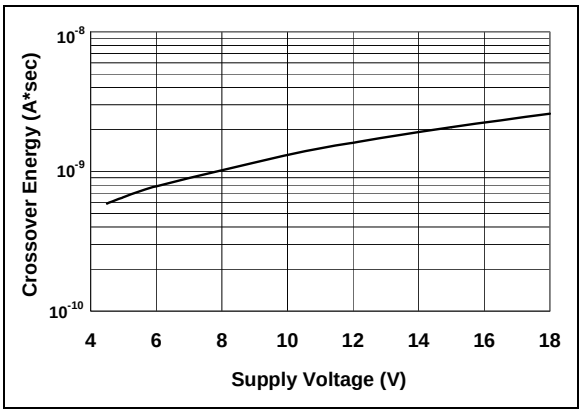



***FIGURE 2-21:*** *Crossover Energy vs. Supply Voltage.*

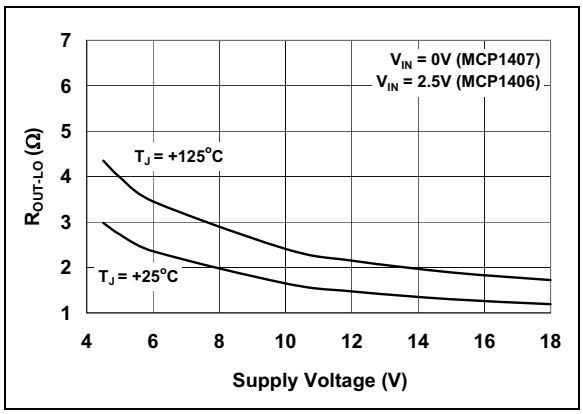



***FIGURE 2-20:*** *Output Resistance (Output Low) vs. Supply Voltage.*

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE(1)**

| 8-Pin PDIP, SOIC | 8-Pin DFN | 5-Pin TO-220 | Symbol | Description |
|---|---|---|---|---|
| 1 | 1 | — | $V_{DD}$ | Supply Input |
| 2 | 2 | 1 | INPUT | Control Input |
| 3 | 3 | — | NC | No Connection |
| 4 | 4 | 2 | GND | Ground |
| 5 | 5 | 4 | GND | Ground |
| 6 | 6 | 5 | OUTPUT | CMOS Push-Pull Output |
| 7 | 7 | — | OUTPUT | CMOS Push-Pull Output |
| 8 | 8 | 3 | $V_{DD}$ | Supply Input |
| — | PAD | — | NC | Exposed Metal Pad |
| — | — | TAB | $V_{DD}$ | Metal Tab at $V_{DD}$ Potential |

**Note 1:** Duplicate pins must be connected for proper operation.

### 3.1 Supply Input ($V_{DD}$)

$V_{DD}$ is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with local capacitors. The bypass capacitors provide a localized low-impedance path for the peak currents that are to be provided to the load.

### 3.2 Control Input (INPUT)

The MOSFET driver input is a high-impedance, TTL/CMOS-compatible input. The input also has hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals, and to provide noise immunity.

### 3.3 Ground (GND)

Ground is the device return pin. The ground pin should have a low impedance connection to the bias supply source return. High peak currents will flow out the ground pin when the capacitive load is being discharged.

### 3.4 CMOS Push-Pull Output (OUTPUT)

The output is a CMOS push-pull output that is capable of sourcing peak currents of 6A ($V_{DD}$ = 18V). The low output impedance ensures the gate of the external MOSFET will stay in the intended state even during large transients. The output pins also have reverse current latch-up ratings of 1.5A.

### 3.5 Exposed Metal Pad

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board to aid in heat removal from the package.

### 3.6 TO-220 Metal Tab

The metal tab on the TO-220 package is at $V_{DD}$ potential. This metal tab is not intended to be the $V_{DD}$ connection to MCP1406/07. $V_{DD}$ should be supplied using the Supply Input pin of the TO-220.

# 4.0 APPLICATION INFORMATION

## 4.1 General Information

MOSFET drivers are high-speed, high current devices which are intended to provide high peak currents to charge the gate capacitance of external MOSFETs or IGBTs. In high frequency switching power supplies, the PWM controller may not have the drive capability to directly drive the power MOSFET. A MOSFET driver like the MCP1406/07 family can be used to provide additional drive current capability.

## 4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully-off state to a fully-on state are characterized by the drivers' rise time ($t_R$), fall time ($t_F$), and propagation delays ($t_{D1}$ and $t_{D2}$). The MCP1406/07 family of devices is able to make this transition very quickly. Figure 4-1 and Figure 4-2 show the test circuits and timing waveforms used to verify the MCP1406/07 timing.

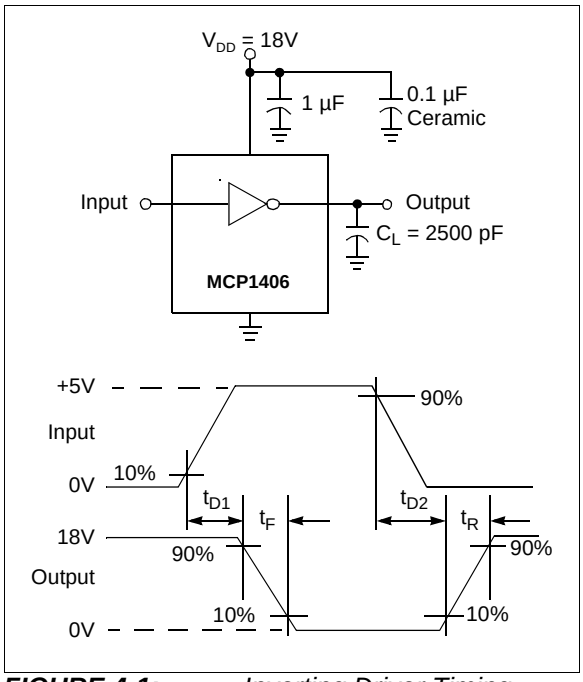



***FIGURE 4-1:*** *Inverting Driver Timing Waveform.*

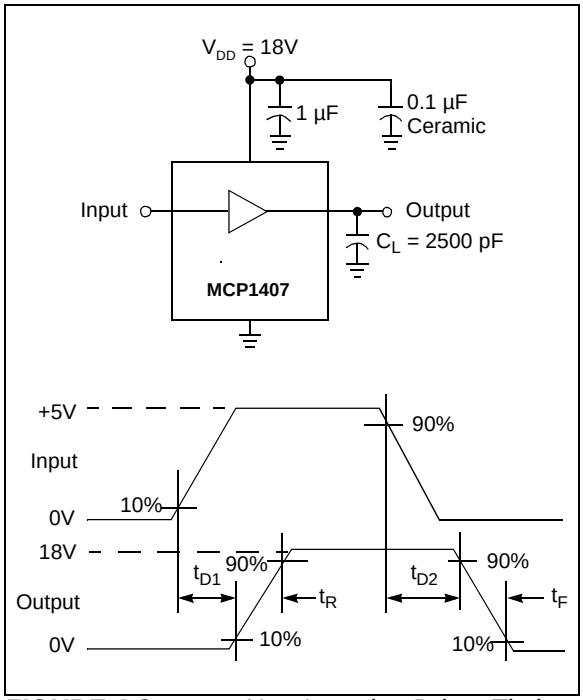



***FIGURE 4-2:*** *Non-Inverting Driver Timing Waveform.*

## 4.3 Decoupling Capacitors

Careful layout and decoupling capacitors are highly recommended when using MOSFET drivers. Large currents are required to charge and discharge capacitive loads quickly. For example, 2.25A are needed to charge a 2500 pF load with 18V in 20 ns.

To operate the MOSFET driver over a wide frequency range with low supply impedance, a ceramic and a low ESR film capacitor are recommended to be placed in parallel between the driver $V_{DD}$ and GND. A 1.0 µF low ESR film capacitor and a 0.1 µF ceramic capacitor placed between pins 1, 8 and 4, 5 should be used. These capacitors should be placed close to the driver to minimized circuit board parasitics and provide a local source for the required current.

## 4.4 PCB Layout Considerations

Proper PCB layout is important in a high current, fast switching circuit to provide proper device operation and robustness of design. PCB trace loop area and inductance should be minimized by the use of a ground plane or ground trace located under the MOSFET gate drive signals, separate analog and power grounds, and local driver decoupling.

The MCP1406/07 devices have two pins each for $V_{DD}$, OUTPUT, and GND. Both pins must be used for proper operation. This also lowers path inductance which will, along with proper decoupling, help minimize ringing in the circuit.

Placing a ground plane beneath the MCP1406/07 will help as a radiated noise shield as well as providing some heat sinking for power dissipated within the device.

## 4.5 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements.

$$P_T = P_L + P_Q + P_{CC}$$

Where:

$P_T$ = Total power dissipation

$P_L$ = Load power dissipation

$P_Q$ = Quiescent power dissipation

$P_{CC}$ = Operating power dissipation

### 4.5.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of frequency, total capacitive load, and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is:

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

f = Switching frequency

$C_T$ = Total load capacitance

$V_{DD}$ = MOSFET driver supply voltage

### 4.5.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends upon the state of the input pin. The MCP1406/07 devices have a quiescent current draw when the input is high of 0.13 mA (typ) and 0.035 mA (typ) when the input is low. The quiescent power dissipation is:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

$I_{QH}$ = Quiescent current in the high state

D = Duty cycle

$I_{QL}$ = Quiescent current in the low state

$V_{DD}$ = MOSFET driver supply voltage

### 4.5.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions; because, for a very short period of time both MOSFETs in the output stage are on simultaneously. This cross-conduction current leads to a power dissipation, as described by the following equation:

$$P_{CC} = CC \times f \times V_{DD}$$

Where:

CC = Cross-conduction constant (A*sec)

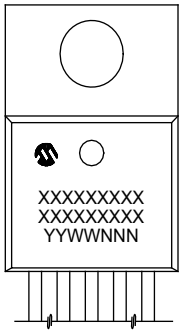
f = Switching frequency

$V_{DD}$ = MOSFET driver supply voltage

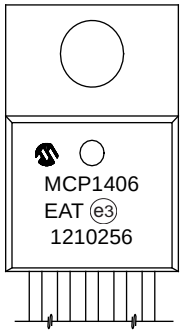
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information (Not to Scale)

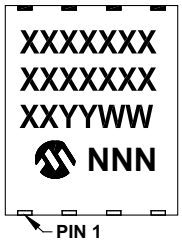
5-Lead TO-220



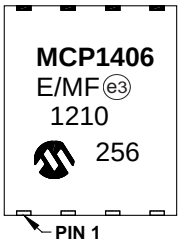

Example



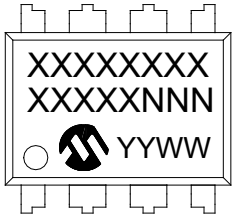

8-Lead DFN-S (6x5x0.9 mm)



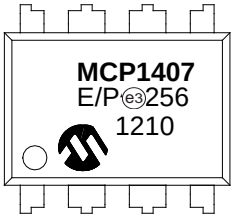

Example




8-Lead PDIP (300 mil)




Example

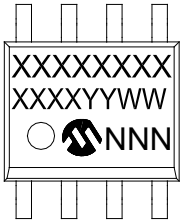



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

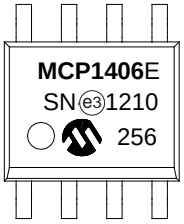
**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 5.1 Package Marking Information (Continued)

8-Lead SOIC (3.90 mm)




Example

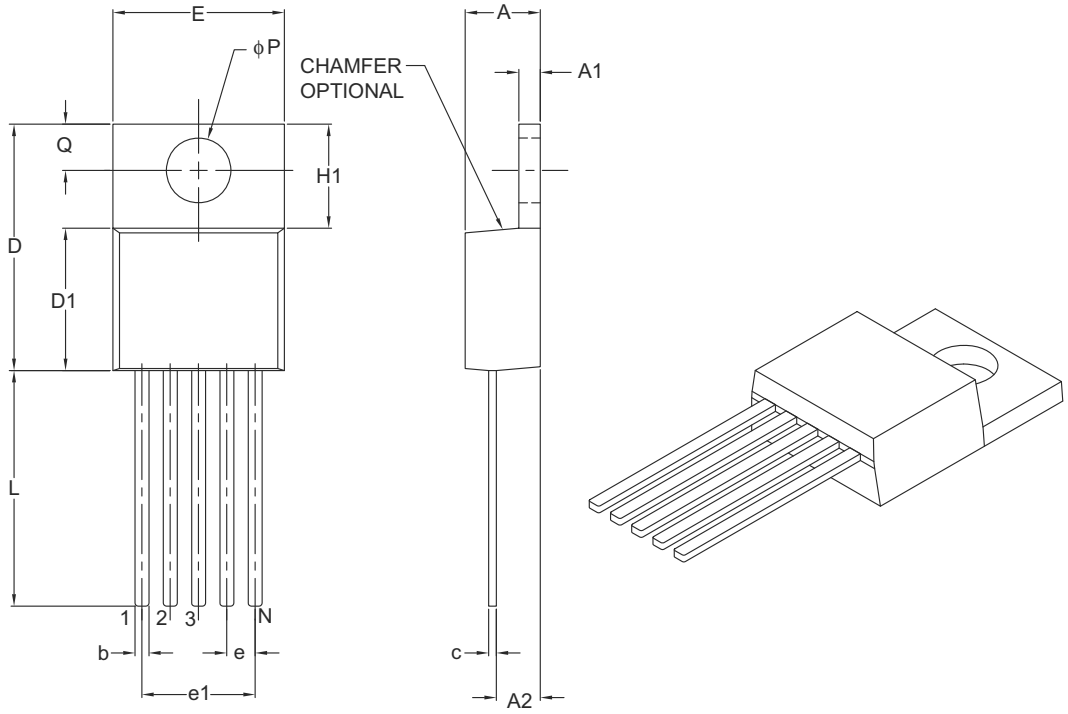



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 5-Lead Plastic Transistor Outline (AT) [TO-220]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 5 | |
| Pitch | e | | .067 BSC | |
| Overall Pin Pitch | e1 | | .268 BSC | |
| Overall Height | A | .140 | – | .190 |
| Overall Width | E | .380 | – | .420 |
| Overall Length | D | .560 | – | .650 |
| Molded Package Length | D1 | .330 | – | .355 |
| Tab Length | H1 | .204 | – | .293 |
| Tab Thickness | A1 | .020 | – | .055 |
| Mounting Hole Center | Q | .100 | – | .120 |
| Mounting Hole Diameter | ϕP | .139 | – | .156 |
| Lead Length | L | .482 | – | .590 |
| Base to Bottom of Lead | A2 | .080 | – | .115 |
| Lead Thickness | c | .012 | – | .025 |
| Lead Width | b | .015 | .027 | .040 |

**Notes:**

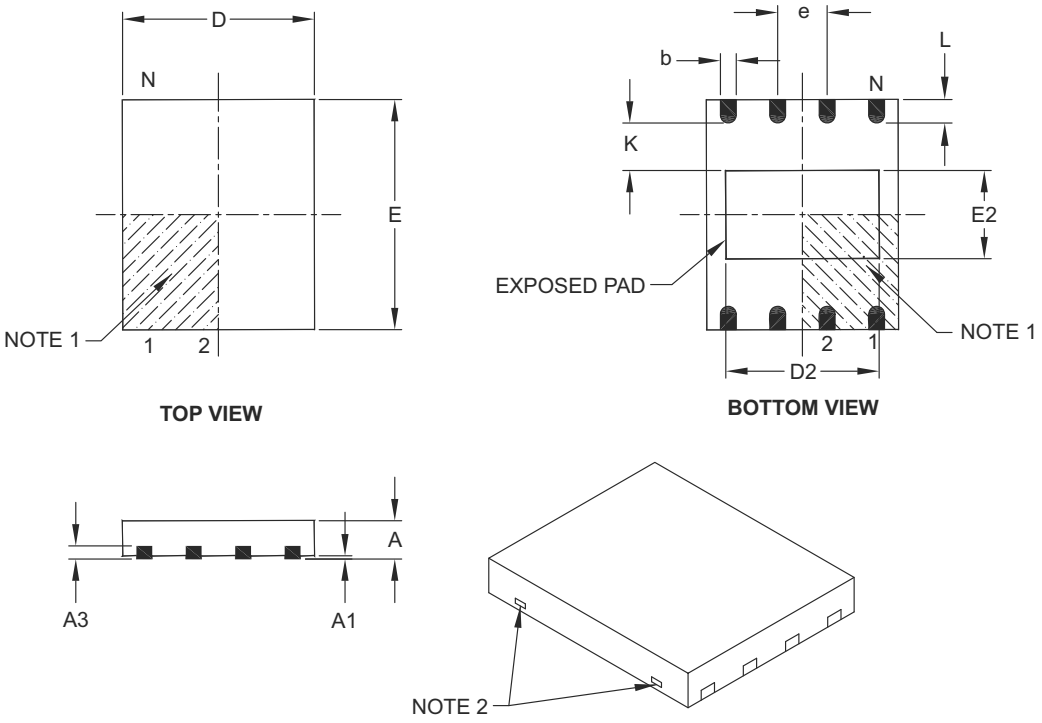
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-036B

## 8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | 0.80 | 0.85 | 1.00 |
| Standoff | A1 | 0.00 | 0.01 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 5.00 BSC | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Length | D2 | 3.90 | 4.00 | 4.10 |
| Exposed Pad Width | E2 | 2.20 | 2.30 | 2.40 |
| Contact Width | b | 0.35 | 0.40 | 0.48 |
| Contact Length | L | 0.50 | 0.60 | 0.75 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

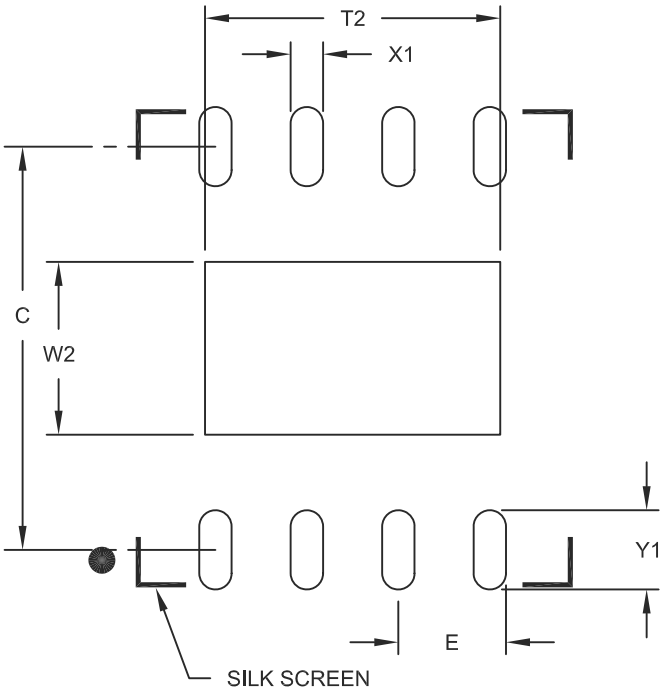
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

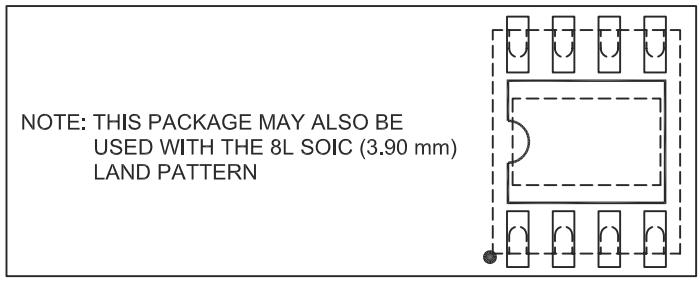
Microchip Technology Drawing C04-122B

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Optional Center Pad Width | W2 | | | 2.40 |
| Optional Center Pad Length | T2 | | | 4.10 |
| Contact Pad Spacing | C | | 5.60 | |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.10 |

Notes:

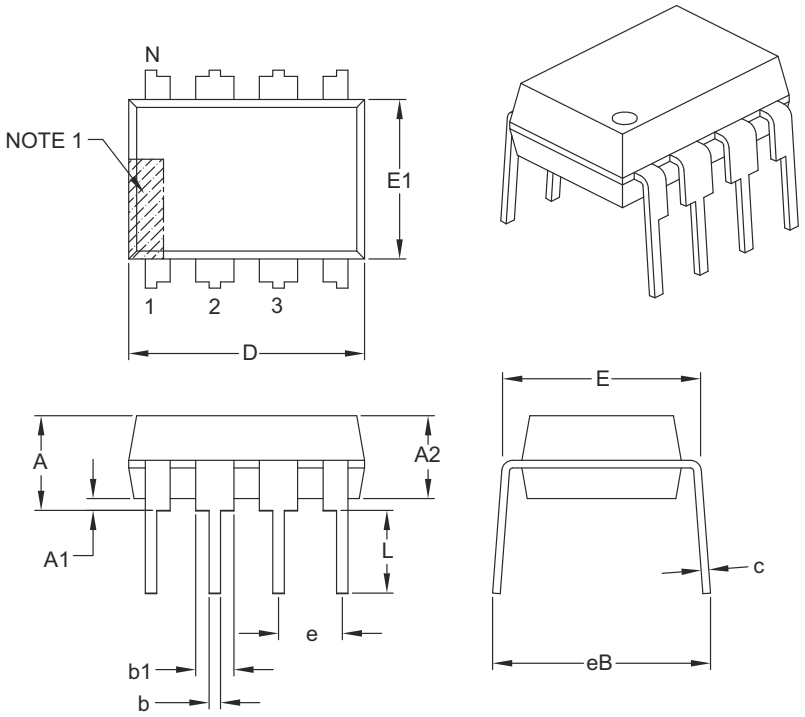
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2122A

## 8-Lead Plastic Dual In-Line (PA) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

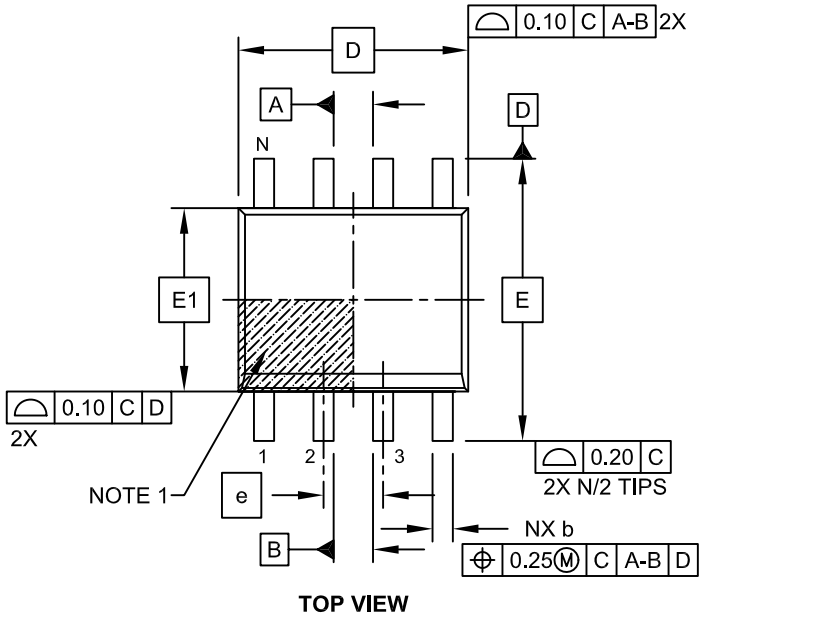
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

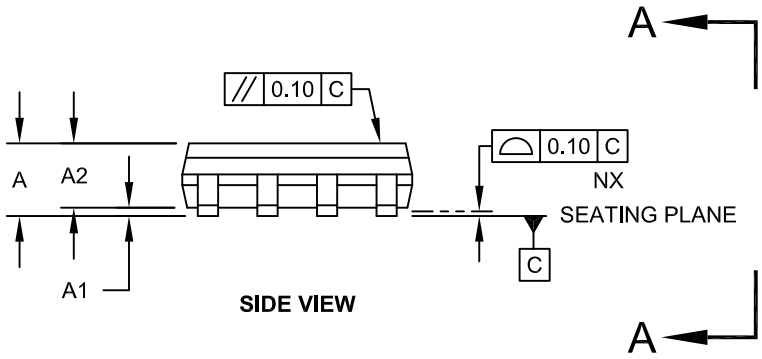
Microchip Technology Drawing C04-018B

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

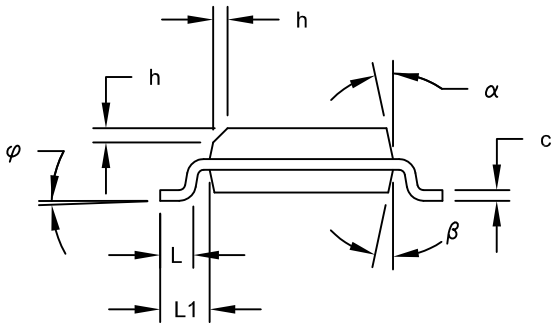
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

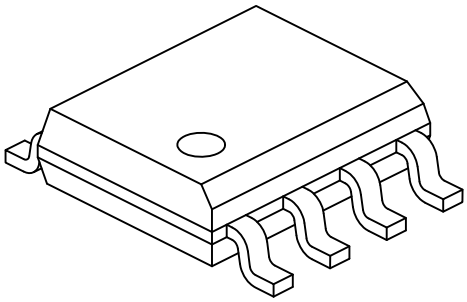



VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

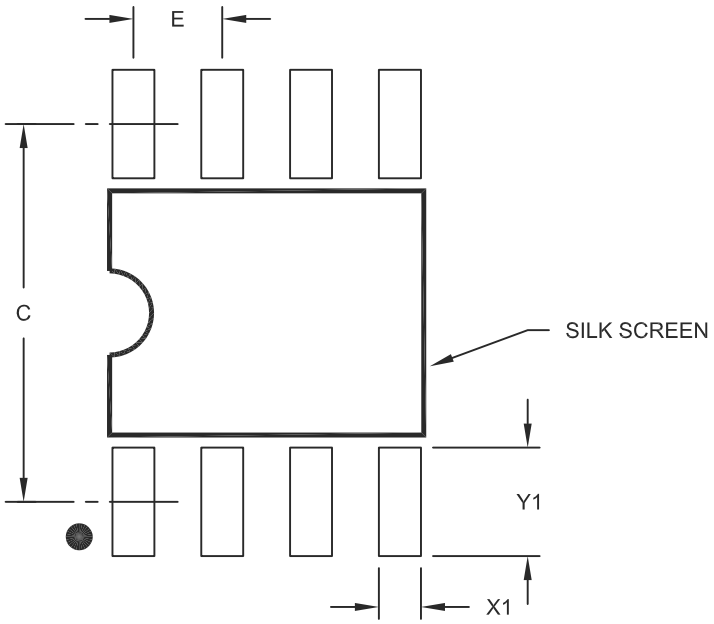
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision B (May 2012)

The following is the list of modifications:

Removed the information referring to the Electrostatic Discharge from the General Description section.

## Revision A (December 2006)

Original release of this document.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Tape & Reel |

| | | |
|---|---|---|
| Device: | MCP1406: | 6A High-Speed MOSFET Driver, Inverting |
| | MCP1406T: | 6A High-Speed MOSFET Driver, Inverting (Tape and Reel) |
| | MCP1407: | 6A High-Speed MOSFET Driver, Non-Inverting |
| | MCP1407T: | 6A High-Speed MOSFET Driver, Non-Inverting (Tape and Reel) |
| Temperature Range: | E = | -40°C to +125°C |
| Package: * | AT = | TO-220, 5-Lead |
| | MF = | Dual, Flat, No-Lead (6x5 mm Body), 8-lead |
| | PA = | Plastic DIP, (300 mil body), 8-lead |
| | SN = | Plastic SOIC (150 mil Body), 8-Lead |

* All package offerings are Pb Free (Lead Free)

**Examples:**

a) MCP1406-E/MF: 6A High-Speed MOSFET Driver, Inverting 8LD DFN package.

b) MCP1406-E/AT: 6A High-Speed MOSFET Driver, Inverting 5LD TO-220 package.

c) MCP1406-E/SN: 6A High-Speed MOSFET Driver, Inverting 8LD SOIC package.

d) MCP1406-E/P: 6A High-Speed MOSFET Driver, Inverting 8LD PDIP package.

e) MCP1406T-E/MF: Tape and Reel, 6A High-Speed MOSFET Driver, Inverting, 8LD DFN pkg.

f) MCP1406T-E/SN: Tape and Reel, 6A High-Speed MOSFET Driver, Inverting, 8LD SOIC pkg.

a) MCP1407-E/MF: 6A High-Speed MOSFET Driver, Non-Inverting 8LD DFN package.

b) MCP1407-E/AT: 6A High-Speed MOSFET Driver, Non-Inverting 5LD TO-220 package.

c) MCP1407-E/SN: 6A High-Speed MOSFET Driver, Non-Inverting 8LD SOIC package.

d) MCP1407-E/P: 6A High-Speed MOSFET Driver, Non-Inverting 8LD PDIP package.

e) MCP1407T-E/MF: Tape and Reel, 6A High-Speed MOSFET Driver, Non-Inverting, 8LD DFN pkg.

f) MCP1407T-E/SN: Tape and Reel, 6A High-Speed MOSFET Driver, Non-Inverting, 8LD SOIC pkg.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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