PIN ASSIGNMENT

B2 [1•	16] V _{DD}
A2 [2	15] A3
(A = B) _{out}	3	14] B3
(A > B) _{in} [4	13] (A > B) _{out}
(A < B) _{in} [5	12] (A < B) _{out}
(A = B) _{in} [6	11] во
A1 [7	10] A0
v _{ss} [8	9] B1
			•





Т	RU	ТН	TAB	LE (x =	Don't	Care))
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Comparing Cascading								Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A < B	A = B	A > B	A < B	A = B	A > B	
A3 > B3	х	х	х	х	х	х	0	0	1	
A3 = B3	A2 > B2	х	х	х	х	х	0	0	1	
A3 = B3	A2 = B2	A1 > B1	х	х	х	х	0	0	1	
A3 = B3	A2 = B2	A1 = B1	A0 > B0	х	х	х	0	0	1	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	0	х	0	0	1	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	0	1	х	0	1	0	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	0	х	1	0	0	
A3 = B3	A2 = B2	A1 = B1	A0 = B0	1	1	х	1	1	0	
A3 = B3	A2 = B2	A1 = B1	A0 < B0	х	х	х	1	0	0	
A3 = B3	A2 = B2	A1 < B1	х	х	х	х	1	0	0	
A3 = B3	A2 < B2	х	х	x	х	х	1	0	0	
A3 < B3	х	х	х	Х	Х	Х	1	0	0	

MC14585B

ELECTRICAL CHARACTERISTICS	(Voltages Referenced to V _{SS}	;)
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			- 5	5°C	25°C			125°C		
Characteristic	Symbol	V _{DD} Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0 10 15	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95		Vdc
	VIL	5.0 10 15	- - -	1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	Vdc
"1" Level ($V_O = 0.5 \text{ or } 4.5 \text{ Vdc}$) ($V_O = 1.0 \text{ or } 9.0 \text{ Vdc}$) ($V_O = 1.5 \text{ or } 13.5 \text{ Vdc}$)	V _{IH}	5.0 10 15	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	- - -	Vdc
$\begin{tabular}{ c c c c } \hline Output Drive Current & & & \\ (V_{OH} = 2.5 \ Vdc) & & Source & \\ (V_{OH} = 4.6 \ Vdc) & & \\ (V_{OH} = 9.5 \ Vdc) & & \\ (V_{OH} = 13.5 \ Vdc) & & \\ \hline \end{tabular}$	I _{ОН}	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2		- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	- - -	- 1.7 - 0.36 - 0.9 - 2.4		mAdc
$\begin{array}{l} (V_{OL} = 0.4 \; Vdc) & Sink \\ (V_{OL} = 0.5 \; Vdc) \\ (V_{OL} = 1.5 \; Vdc) \end{array}$	I _{OL}	5.0 10 15	0.64 1.6 4.2	_ _ _	0.51 1.3 3.4	0.88 2.25 8.8	_ _ _	0.36 0.9 2.4	- - -	mAdc
Input Current	l _{in}	15	-	±0.1	-	± 0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)	I _{DD}	5.0 10 15	- - -	5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	IT	5.0 10 15	$I_{T} = (0.6 \ \mu\text{A/kHz}) \text{ f} + I_{\text{DD}}$ $I_{T} = (1.2 \ \mu\text{A/kHz}) \text{ f} + I_{\text{DD}}$ $I_{T} = (1.8 \ \mu\text{A/kHz}) \text{ f} + I_{\text{DD}}$				μAdc			

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF: I_T(C_L) = I_T(50 pF) + (C_L - 50) Vfk where: I_T is in µA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, $T_A = 25^{\circ}C$)

Characteristic	Symbol	V _{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t _{TLH} , t _{THL}	5.0 10 15	- - -	100 50 40	200 100 80	ns
Turn–On, Turn–Off Delay Time t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 345 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 147 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 105 \text{ ns}$	t _{PLH} , t _{PHL}	5.0 10 15		430 180 130	860 360 260	ns

The formulas given are for the typical characteristics only at 25°C.
 Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low. f in respect to a system clock.





Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A<B) low.

Figure 2. Dynamic Signal Waveforms





MC14585B

LOGIC DIAGRAM



MC14585B

PACKAGE DIMENSIONS

PDIP-16 CASE 648-08 ISSUE T



- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL. 4. DIMENSION B DOES NOT INCLUDE MOLD ELASH
- MOLD FLASH. 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIM	IETERS					
DIM	MIN	MAX	MIN	MAX					
Α	0.740	0.770	18.80	19.55					
В	0.250	0.270	6.35	6.85					
С	0.145	0.175	3.69	4.44					
D	D 0.015 0.021	0.39	0.53						
F	0.040	0.70	1.02	1.77					
G	0.100	BSC	2.54 BSC						
н	0.050	BSC	1.27 BSC						
J	0.008	0.015	0.21	0.38					
ĸ	0.110	0.130	2.80	3.30					
L	0.295 0.305		7.50	7.74					
M	0 °	10 °	0 °	10 °					
S	0.020	0.040	0.51	1.01					

SOIC-16 CASE 751B-05 **ISSUE J**



NOTES:

- NO TES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006)

- MAXIMUM MOLD PHOTHOSION 0. 19 (0.000) PER SIDE.
 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

		MILLIN	IETERS	INC	HES		
	DIM	MIN	MAX	MIN	MAX		
	Α	9.80	10.00	0.386	0.393		
	В	3.80	4.00	0.150	0.157		
	С	1.35	1.75	0.054	0.068		
	D	0.35	0.49	0.014	0.019		
	F	0.40	1.25	0.016	0.049		
	G	1.27	BSC	0.050 BSC			
	J	0.19	0.25	0.008	0.009		
	Κ	0.10	0.25	0.004	0.009		
	М	0 °	7°	0 °	7°		
	Р	5.80	6.20	0.229	0.244		
1	R	0.25	0.50	0.010	0.010		

PACKAGE DIMENSIONS

SOEIAJ-16 CASE 966-01 ISSUE A



 \frown

0.10 (0.004)

е

⊕ 0.13 (0.005) M







NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE
- MOLD FLASH OF PROTROSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. TERMINAL NUMBERS ARE SHOWN FOR
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 THE LEAD WIDTH DIMENSION (b) DOES NOT

5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.10 5.45 0.2		0.215
е	1.27	1.27 BSC) BSC
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10 1.50	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q ₁	0.70	0.90	0.028	0.035
Z		0.78		0.031

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