

8-Bit Parallel DAC in QSOP-16 Package

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND-0.3V to +17V
 REF to GND±25V
 RFB to GND±25V
 Digital Inputs to GND-0.3V to (V_{DD} + 0.3V)
 OUT1, OUT2 to GND.....-0.3V to V_{DD}

Operating Temperature Ranges

MAX5480_CEE.....0°C to +70°C
 MAX5480_EEE.....-40°C to +85°C
 Storage Temperature Range-65°C to +160°C
 Continuous Power Dissipation (T_A = +70°C)
 MAX5480_EE (derate 8.3mW/°C above +70°C)667mW
 Lead Temperature (soldering 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, Circuit of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				8			Bits
Relative Accuracy	INL			±1/2			LSB
Differential Nonlinearity	DNL	All grades guaranteed monotonic over temperature		±1			LSB
Gain Error (Note 1)		T _A = T _{MIN} to T _{MAX}		±1			LSB
Gain Temperature Coefficient (Note 2)				±2			ppm/°C
Supply Rejection	PSR	MAX5480A (Note 3)	T _A = +25°C	0.002	0.08	%FSR/%	
			T _A = T _{MIN} to T _{MAX}	0.01	0.16		
		MAX5480B	T _A = +25°C	0.002			
			T _A = T _{MIN} to T _{MAX}	0.01			
Output Leakage Current (I _{OUT1})		V _{REF} = ±10V DAC code = full scale	T _A = +25°C	±50		nA	
			T _A = T _{MIN} to T _{MAX}	±400			
Output Leakage Current (I _{OUT2})		V _{REF} = ±10V DAC code = zero scale	T _A = +25°C	±50		nA	
			T _A = T _{MIN} to T _{MAX}	±400			
REFERENCE INPUT							
Input Resistance	R _{REF}	pin 15 to GND		5	10	20	kΩ
DYNAMIC PERFORMANCE							
Output Current Settling Time to 1/2LSB		D0–D7 = 0V to V _{DD} or V _{DD} to 0V, $\overline{WR}$ = $\overline{CS}$ = 0V, OUT1 load = 100Ω 13pF	MAX5480A (Note 3)	T _A = +25°C	400		ns
				T _A = T _{MIN} to T _{MAX}	500		
				MAX5480B	T _A = +25°C	250	
AC Feedthrough (OUT1 or OUT2)		V _{REF} = ±10V, 100kHz sine wave, $\overline{WR}$ = $\overline{CS}$ = 0V	MAX5480A (Note 3)	T _A = +25°C	0.25		ns
				T _A = T _{MIN} to T _{MAX}	0.5		
				MAX5480B	T _A = +25°C	0.1	
ANALOG OUTPUTS							
OUT1 Capacitance (Note 3)	C _{OUT1}	D0–D7 = V _{DD} , $\overline{WR}$ = $\overline{CS}$ = 0V		120		pF	
		D0–D7 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V		30			
OUT2 Capacitance (Note 3)	C _{OUT2}	D0–D7 = V _{DD} , $\overline{WR}$ = $\overline{CS}$ = 0V		30		pF	
		D0–D7 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V		120			

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MAX5480

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +5V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = 0V$, Circuit of Figure 1, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Input High Voltage	V _{IH}			2.4			V
Input Low Voltage	V _{IL}					0.8	V
Input Current	I _{IN}	T _A = +25°C; V _{IN} = 0V to V _{DD}				±1	μA
		T _A = T _{MIN} to T _{MAX}				±10	
Input Capacitance (Note 3)	C _{IN}	D0–D7				8	pF
		WR, CS				20	
POWER REQUIREMENTS							
Supply Current	I _{DD}	Digital inputs at 0V or V _{DD}	T _A = +25°C			100	μA
			T _A = T _{MIN} to T _{MAX}			500	
SWITCHING CHARACTERISTICS (Figure 4)							
Chip-Select to Write-Setup Time	t _{CS}	MAX5480A			220		ns
		MAX5480B			35		
Chip-Select to Write-Hold Time	t _{CH}	MAX5480A			0		ns
		MAX5480B			0		
Write Pulse Width	t _{WR}	MAX5480A			220		ns
		MAX5480B			35		
Data-Setup Time	t _{DS}	MAX5480A			170		ns
		MAX5480B			55		
Data-Hold Time	t _{DH}	MAX5480A			10		ns
		MAX5480B			-7		

Note 1: Gain error is measured using internal feedback resistor. Full-scale range (FSR) = V_{REF} .

Note 2: Gain TempCo measured from $+25^{\circ}C$ to T_{MAX} and from $+25^{\circ}C$ to T_{MIN} .

Note 3: Guaranteed by design.

Pin Description

PIN	NAME	FUNCTION
1	OUT1	R-2R Ladder Output
2	OUT2	R-2R Ladder Output, complement of OUT1
3	GND	Ground
4–11	D7–D0	Data Inputs, D7 is the most significant bit.
12	$\overline{CS}$	Chip Select Input. Active Low.
13	$\overline{WR}$	Write Control Input. Active Low.
14	V_{DD}	Power Supply Input, +5V
15	REF	Reference Voltage Input
16	RFB	Feedback Resistor Connection

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Detailed Description

The MAX5480 is an 8-bit multiplying digital-to-analog converter (DAC) that consists of a thin-film R-2R resistor array with CMOS current steering switches. Figure 3 shows a simplified schematic of the DAC. The inverted R-2R ladder divides the voltage or current reference in a binary manner among the eight steering switches. The magnitude of the current appearing at either OUT terminal depends on the number of switches selected; therefore, the output is an analog representation of the digital input. The two OUT terminals must be held at the same potential so a constant current is maintained in each ladder leg. This makes the REF input current independent of switch state and also ensures that the MAX5480 maintains its excellent linearity performance.

Interface-Logic Information

Mode Selection

The inputs $\overline{CS}$ and $\overline{WR}$ control the MAX5480's operating mode (see Table 1).

Write Mode

When $\overline{CS}$ and $\overline{WR}$ are both low, the MAX5480 is in write mode, and its analog output responds to data activity at the D0–D7 data-bus inputs. In this mode, the data latches are transparent (see Tables 2 and 3).

Hold Mode

In hold mode, the MAX5480 retains the data that was present on D0–D7 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. The analog output remains at the value corresponding to the digital code locked in the data latch.

Applications Information

Using the MAX5480 in Voltage-Output Mode (Single Supply)

The MAX5480 can be used either as a current-output DAC (Figures 1 and 6) or as a voltage-output DAC (Figures 2 and 5).

To use the MAX5480 in voltage mode, connect OUT1 to the reference input and connect OUT2 to ground. REF, now the DAC output, is a voltage source with a constant output resistance of 10k Ω (nominally). This output is often buffered with an op amp (Figure 5).

An advantage of voltage-mode operation is single-supply operation for the complete circuit; i.e., a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted in voltage mode. The reference input (voltage at OUT1) must always be positive and is limited to no more than $V_{DD} - 3V$. If the reference voltage exceeds this value, linearity is degraded.

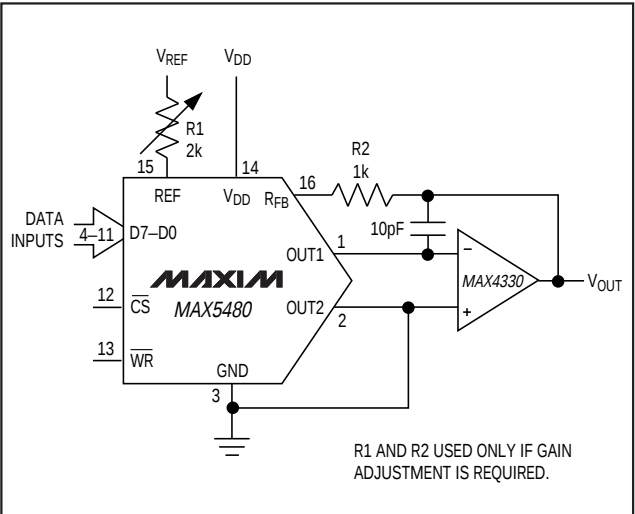


Figure 1. Unipolar Binary Operation (Two-Quadrant Multiplication)

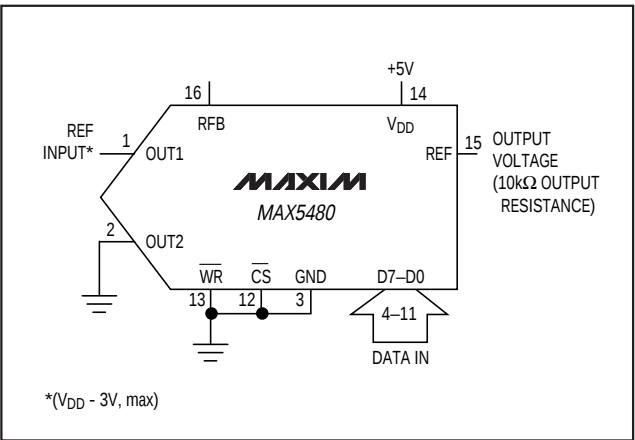


Figure 2. Typical Operating Circuit (Voltage Mode—Unbuffered)

Table 1. Mode-Selection Table

$\overline{CS}$	$\overline{WR}$	MODE	DAC Response
L	L	Write	DAC responds to data bus (D0–D7) inputs.
H X	X H	Hold Hold	Data bus (D0–D7) is locked out; DAC holds last data present when $\overline{CS}$ or $\overline{WR}$ assumed high state.

L = Low State, H = High State, X = Don't Care

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Table 2. Unipolar Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{255}{256} \right)$
1 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{129}{256} \right)$
1 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{128}{256} \right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{127}{256} \right)$
0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{1}{256} \right)$
0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{0}{256} \right) = 0$

NOTE: 1 LSB = $(2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

Table 3. Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1	$+V_{REF} \left(\frac{127}{128} \right)$
1 0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{128} \right)$
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{1}{128} \right)$
0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{127}{128} \right)$
0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{128}{128} \right)$

NOTE: 1 LSB = $(2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

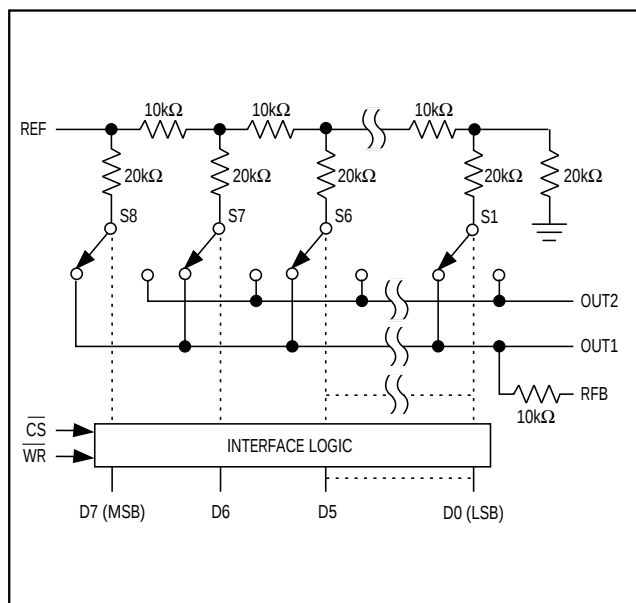


Figure 3. MAX5480 Functional Diagram

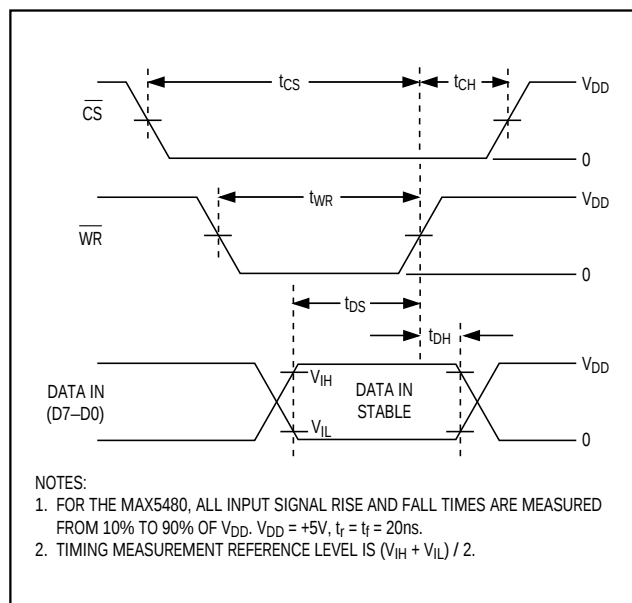


Figure 4. Write-Cycle Timing Diagram

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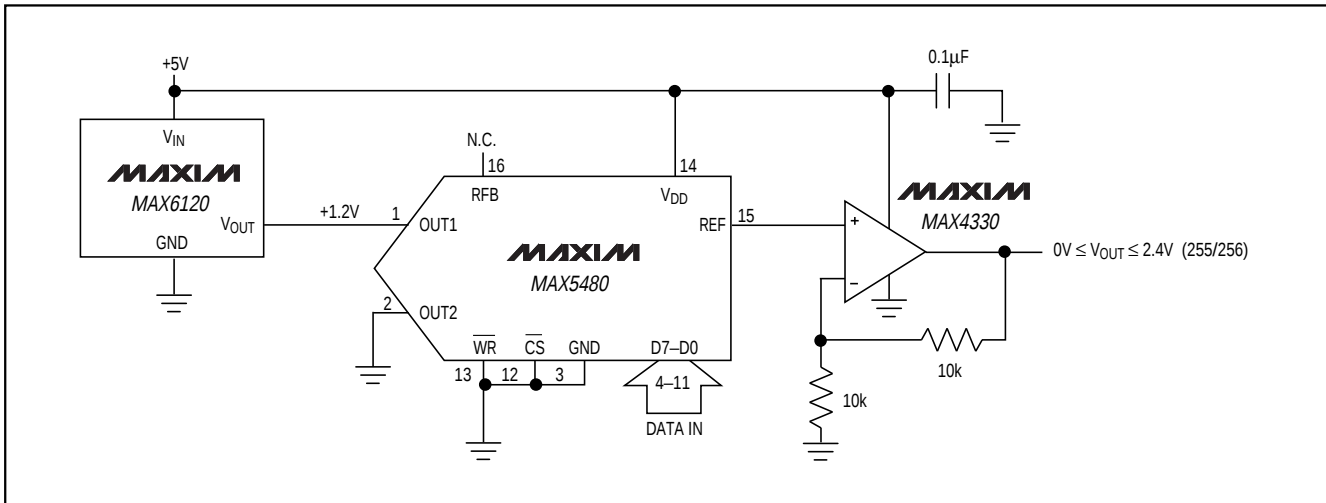


Figure 5. Single-Supply Voltage-Output Mode (Buffered)

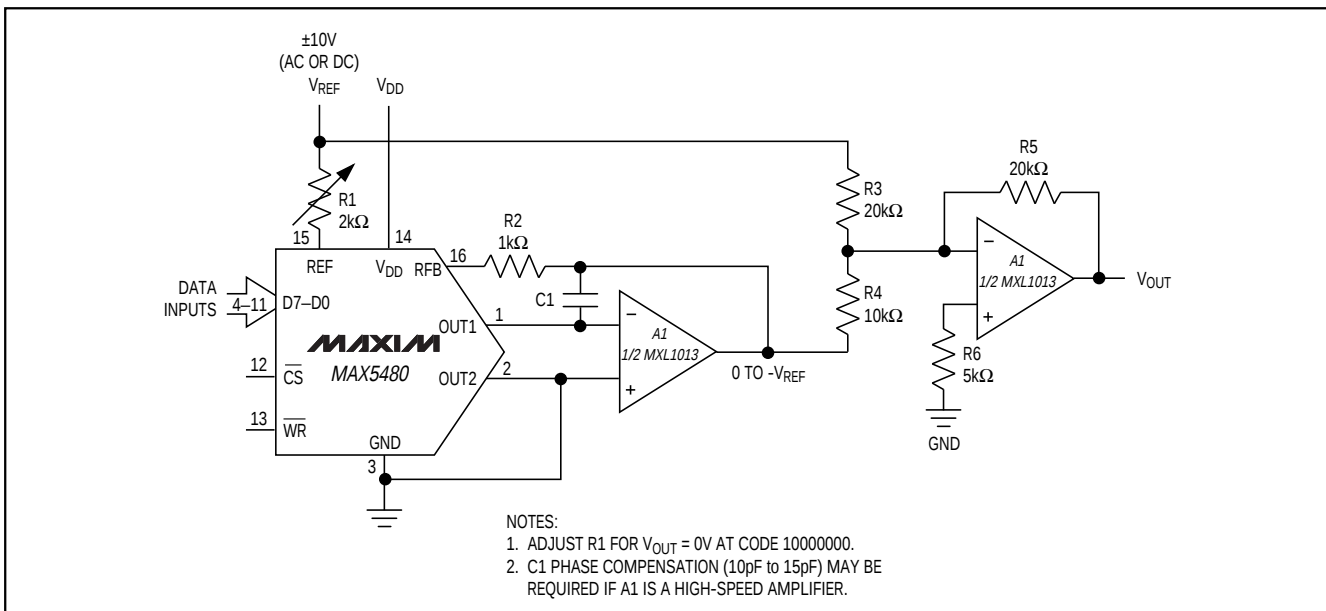


Figure 6. Bipolar (Four-Quadrant) Operation

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6 Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

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