Absolute Maximum Ratings

V_{CC}, RS+, RS- to GND..-0.3V to +30V
OUT to GND..-0.3V to +15V
Differential Input Voltage (V_{RS+} - V_{RS-})............................±0.3V
Current into Any Pin ....±10mA
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 3.9mW/°C above +70°C) 312.6mW
8-Pin SO (derate 7.4mW/°C above +70°C).............588.2mW
3 x 2 UCSP (derate 3.4mW/°C above +70°C) 273.2mW

Operating Temperature Range.......................... -40°C to +85°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow).....................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{RS+} = 0 to 28V, V_{CC} = 2.7V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 2)	V_{CC}			2.7		28	V
Common-Mode Input Range (Note 3)	V_{CMR}			0		28	V
Common-Mode Rejection	CMR	V_{RS+} > 2V			85		dB
Supply Current	I_{CC}	V_{RS+} > 2V, V_{SENSE} = 5mV			30	60	µA
Leakage Current	I_{RS+}, I_{RS-}	V_{CC} = 0V, V_{RS+} = 28V			0.05	1.2	µA
Input Bias Current	I_{RS+}	V_{RS+} > 2V		0		1	µA
		V_{RS+} ≤ 2V		-25		+2	
	I_{RS-}	V_{RS+} > 2V		0		2	
		V_{RS+} ≤ 2V		-50		+2	
Full-Scale Sense Voltage (Note 4)	V_{SENSE}	Gain = 20V/V or 50V/V			150		mV
		Gain = 100V/V			100		
Input Offset Voltage (Note 5)	V_{OS}	T_A = +25°C, V_{CC} = V_{RS+} = 12V	MAX4372_ESA		0.3	±0.8	mV
			MAX4372_EUK, _EBT		0.3	±1.3	
		T_A = T_{MIN} to T_{MAX}, V_{CC} = V_{RS+} = 12V	MAX4372_ESA			±1.1	
			MAX4372_EUK, _EBT			±1.9	
Full-Scale Accuracy (Note 5)		V_{SENSE} = 100mV, V_{CC} = 12V, V_{RS+} = 12V, T_A = +25°C (Note 7)			±0.18	±3	%
Total OUT Voltage Error (Note 6)		V_{SENSE} = 100mV, V_{CC} = 12V, V_{RS+} = 12V (Note 7)				±6	
		V_{SENSE} = 100mV, V_{CC} = 28V, V_{RS+} = 28V (Note 7)			±0.15	±7	
		V_{SENSE} = 100mV, V_{CC} = 12V, V_{RS+} = 0.1V (Note 7)			±1	±28	
		V_{SENSE} = 6.25mV, V_{CC} = 12V, V_{RS+} = 12V (Note 8)			±0.15		

Electrical Characteristics (continued)

(V_{RS+} = 0 to 28V, V_{CC} = 2.7V to 28V, V_{SENSE} = 0V, R_{LOAD} = 1MΩ, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

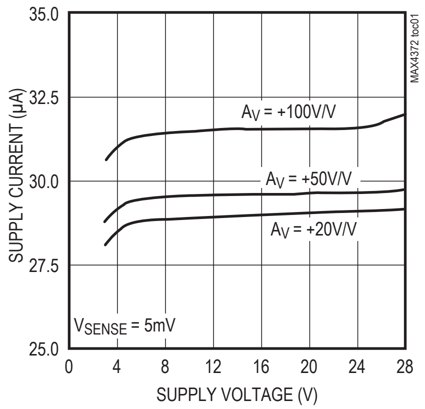
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT Low Voltage (MAX4372T, MAX4372F)	V_{OL}	V_{CC} = 2.7V, V_{SENSE} = -10mV, V_{RS+} = 28V	I_{OUT} = 10µA		2.6		mV
			I_{OUT} = 100µA		9	65	
OUT Low Voltage (MAX4372H)	V_{OL}	V_{CC} = 2.7V, V_{SENSE} = -10mV, V_{RS+} = 12V	I_{OUT} = 10µA		2.6		mV
			I_{OUT} = 100µA		9	65	
OUT High Voltage	V_{CC} - V_{OH}	V_{CC} = 2.7V, I_{OUT} = -500µA, V_{SENSE} = 250mV, V_{RS+} = 28V			0.1	0.25	V
-3dB Bandwidth	BW	V_{RS+} = 12V, V_{CC} = 12V, C_{LOAD} = 10pF	V_{SENSE} = 20mV, gain = 20V/V		275		kHz
			V_{SENSE} = 20mV, gain = 50V/V		200		
			V_{SENSE} = 20mV, gain = 100V/V		110		
			V_{SENSE} = 6.25mV		50		
Gain		MAX4372T			20		V/V
		MAX4372F			50		
		MAX4372H			100		
Gain Accuracy		V_{SENSE} = 20mV to 100mV, V_{RS+} = 12V	T_A = +25°C		±0.25	±2.5	%
			T_A = -40°C to +85°C			±5.5	
OUT Settling Time to 1% of Final Value		Gain = 20V/V, V_{CC} = 12V, V_{RS+} = 12V, C_{LOAD} = 10pF	V_{SENSE} = 6.25mV to 100mV		20		µs
			V_{SENSE} = 100mV to 6.25mV		20		
Capacitive-Load Stability		No sustained oscillations			1000		pF
OUT Output Resistance	R_{OUT}	V_{SENSE} = 100mV			1.5		Ω
Power-Supply Rejection	PSR	V_{OUT} = 2V, V_{RS+} > 2V		75	85		dB
Power-Up Time to 1% of Final Value		V_{CC} = 12V, V_{RS+} = 12V, V_{SENSE} = 100mV, C_{LOAD} = 10pF			0.5		ms
Saturation Recovery Time (Note 9)		V_{CC} = 12V, V_{RS+} = 12V, C_{LOAD} = 10pF			0.1		ms

Note 1: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Guaranteed by PSR test.
Note 3: Guaranteed by OUT voltage error test.
Note 4: Output voltage is internally clamped not to exceed 12V.
Note 5: V_{OS} is extrapolated from the gain accuracy tests.
Note 6: Total OUT voltage error is the sum of gain and offset voltage errors.
Note 7: Measured at I_{OUT} = -500µA (R_{LOAD} = 4kΩ for gain = 20V/V, R_{LOAD} = 10kΩ for gain = 50V/V, R_{LOAD} = 20kΩ for gain = 100V/V).
Note 8: 6.25mV = 1/16 of 100mV full-scale voltage (C/16).
Note 9: The device does not reverse phase when overdriven.

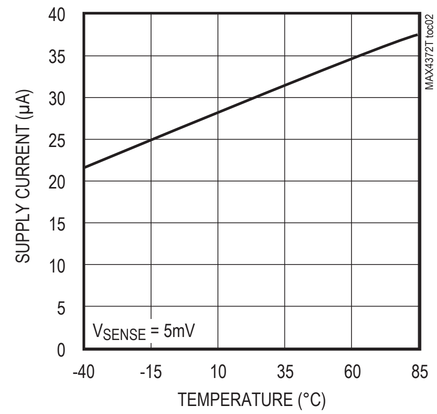
Typical Operating Characteristics

(V_{CC} = 12V, V_{RS+} = 12V, V_{SENSE} = 100mV, T_A = +25°C, unless otherwise noted.)

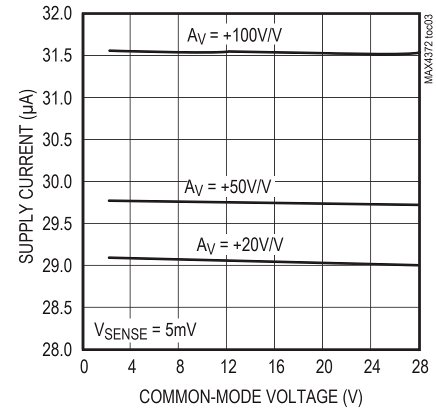
SUPPLY CURRENT vs. SUPPLY VOLTAGE



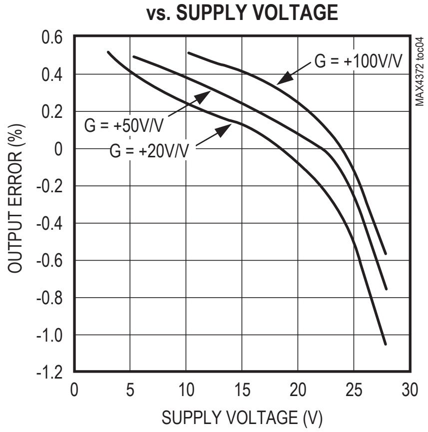
SUPPLY CURRENT vs. TEMPERATURE



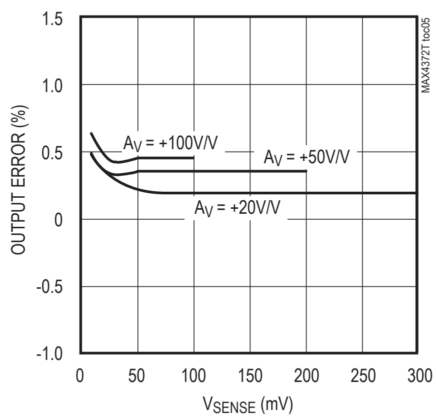
SUPPLY CURRENT vs. COMMON-MODE VOLTAGE



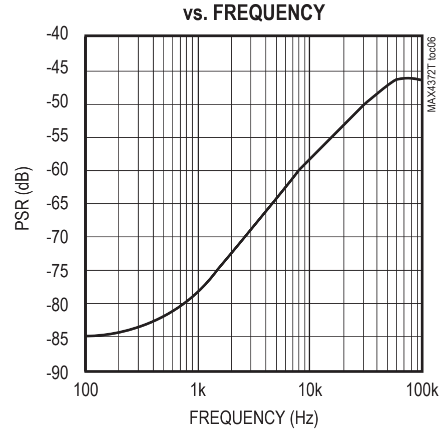
TOTAL OUTPUT ERROR vs. SUPPLY VOLTAGE



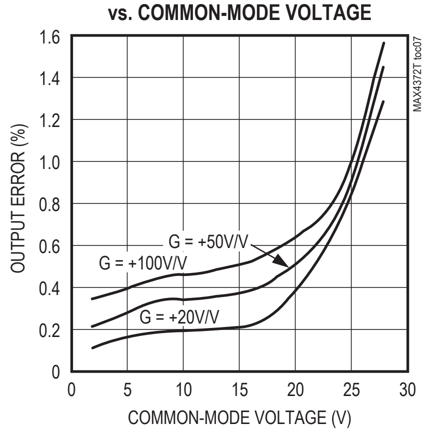
TOTAL OUTPUT ERROR vs. V_{SENSE}



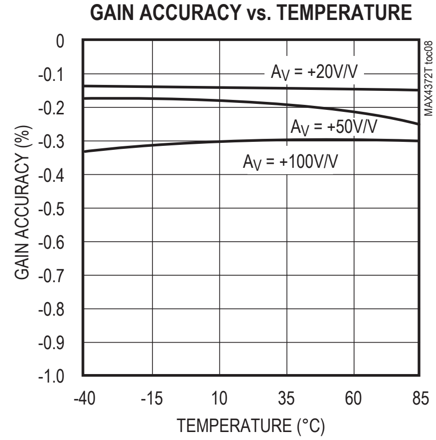
POWER-SUPPLY REJECTION vs. FREQUENCY



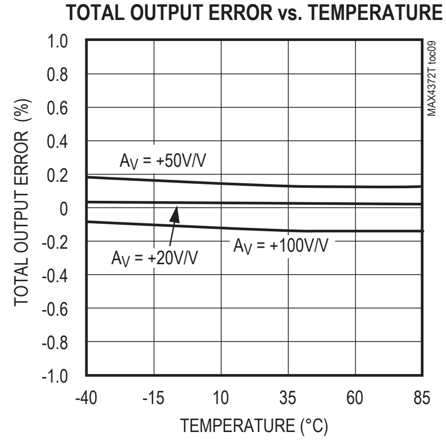
TOTAL OUTPUT ERROR vs. COMMON-MODE VOLTAGE



GAIN ACCURACY vs. TEMPERATURE

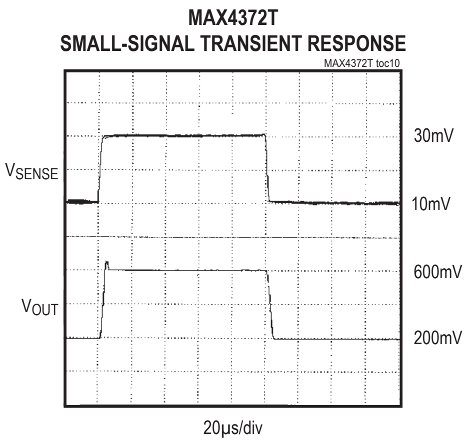


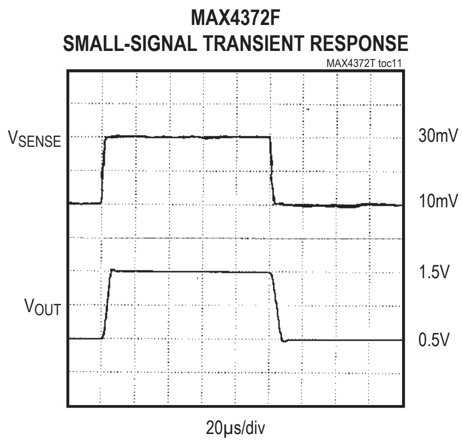
TOTAL OUTPUT ERROR vs. TEMPERATURE

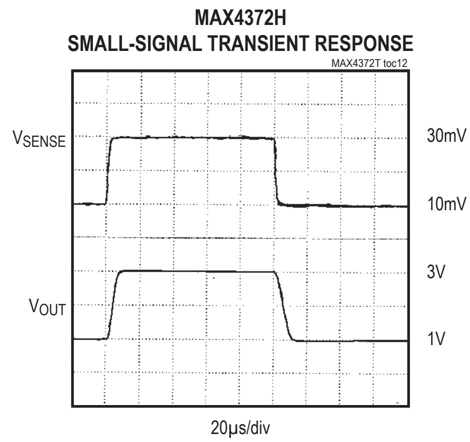


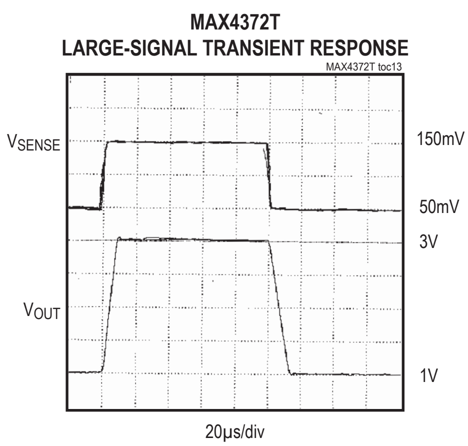
Typical Operating Characteristics (continued)

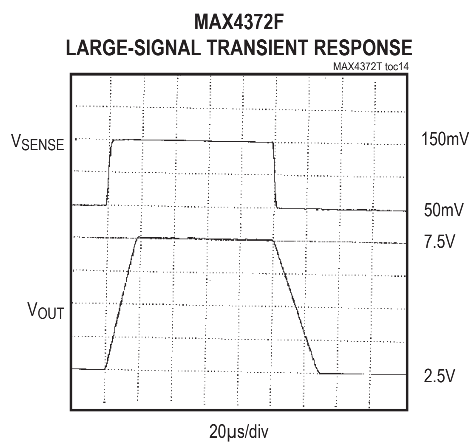
(V_{CC} = 12V, V_{RS+} = 12V, V_{SENSE} = 100mV, T_A = +25°C, unless otherwise noted.)

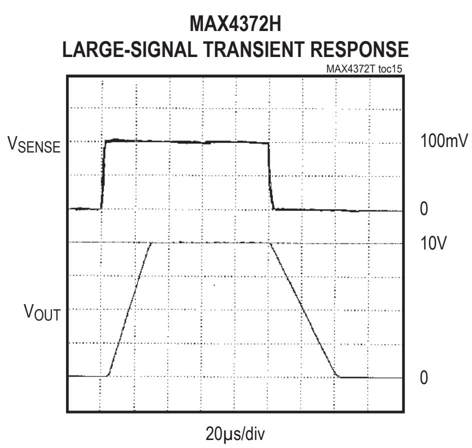


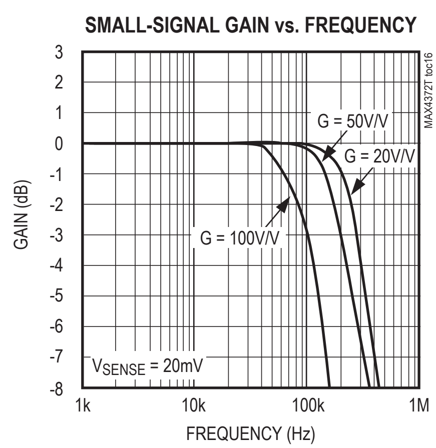












Pin/Bump Description

PIN		BUMP	NAME	FUNCTION
SOT23	SO	UCSP		
1	3	A2	GND	Ground
2	4	A3	OUT	Output Voltage. V_{OUT} is proportional to the magnitude of V_{SENSE} (V_{RS+} - V_{RS-}).
3	1	A1	V_{CC}	Supply Voltage. Use at least a 0.1µF capacitor to decouple V_{CC} from fast transients.
4	8	B1	RS+	Power Connection to the External Sense Resistor
5	6	B3	RS-	Load-Side Connection to the External Sense Resistor
—	2, 5, 7	—	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX4372 high-side current-sense amplifier features a 0 to 28V input common-mode range that is independent of supply voltage. This feature allows the monitoring of current flow out of a battery in deep discharge, and also enables high-side current sensing at voltages far in excess of the supply voltage (V_{CC}).

Current flows through the sense resistor, generating a sense voltage (Figure 1. Functional Diagram). Since A1's inverting input is high impedance, the voltage on the negative terminal equals V_{IN} - V_{SENSE}. A1 forces its positive terminal to match its negative terminal; therefore, the voltage across R_{G1} (V_{IN} - V1-) equals V_{SENSE}. This creates a current to flow through R_{G1} equal to V_{SENSE}/R_{G1}. The transistor and current mirror amplify the current by a factor of β. This makes the current flowing out of the current mirror equal to:

$$I_M = \beta\, V_{SENSE}/R_{G1}$$

A2's positive terminal presents high impedance, so this current flows through R_{GD}, with the following result:

$$V2+ = R_{GD}\, \beta \times V_{SENSE}/R_{G1}$$

R1 and R2 set the closed-loop gain for A2, which amplifies V2+, yielding:

$$V_{OUT} = R_{GD} \times \beta \times V_{SENSE}/R_{G1}\ (1 + R2/R1)$$

The gain of the device equals:

$$\frac{V_{OUT}}{V_{SENSE}} = RGD \times \beta(1 + R2/R1)/R_{G1}$$

Applications Information

Recommended Component Values

The MAX4372 operates over a wide variety of current ranges with different sense resistors. Table 1 lists common resistor values for typical operation of the MAX4372.

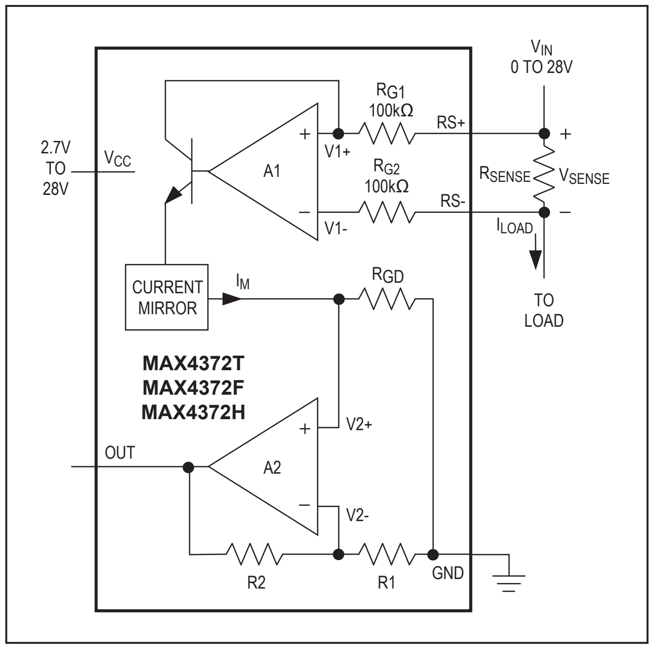


Figure 1. Functional Diagram

Choosing R_{SENSE}

Given the gain and maximum load current, select R_{SENSE} such that V_{OUT} does not exceed V_{CC} - 0.25V or 10V. To measure lower currents more accurately, use a high value for R_{SENSE}. A higher value develops a higher sense voltage, which overcomes offset voltage errors of the internal current amplifier.

In applications monitoring very high current, ensure R_{SENSE} is able to dissipate its own I^2R losses. If the resistor's rated power dissipation is exceeded, its value may drift or it may fail altogether, causing a differential voltage across the terminals in excess of the absolute maximum ratings.

Table 1. Recommended Component Values

FULL-SCALE LOAD CURRENT, I_{LOAD} (A)	CURRENT-SENSE RESISTOR, R_{SENSE} (mΩ)	GAIN (V/V)	FULL-SCALE OUTPUT VOLTAGE (FULL-SCALE V_{SENSE} = 100mV), V_{OUT} (V)
0.1	1000	20	2.0
		50	5.0
		100	10.0
1	100	20	2.0
		50	5.0
		100	10.0
5	20	20	2.0
		50	5.0
		100	10.0
10	10	20	2.0
		50	5.0
		100	10.0

Using a PC Board Trace as R_{SENSE}

If the cost of R_{SENSE} is an issue and accuracy is not critical, use the alternative solution shown in Figure 2. This solution uses copper PC board traces to create a sense resistor. The resistivity of a 0.1in wide trace of 2oz copper is about 30mΩ/ft. The resistance temperature coefficient of copper is fairly high (approximately 0.4%/°C), so systems that experience a wide temperature variance must compensate for this effect. In addition, self-heating introduces a nonlinearity error. Do not exceed the maximum power dissipation of the copper trace.

For example, the MAX4372T (with a maximum load current of 10A and an R_{SENSE} of 5mΩ) creates a full-scale V_{SENSE} of 50mV that yields a maximum V_{OUT} of 1V. R_{SENSE}, in this case, requires about 2in of 0.1in wide copper trace.

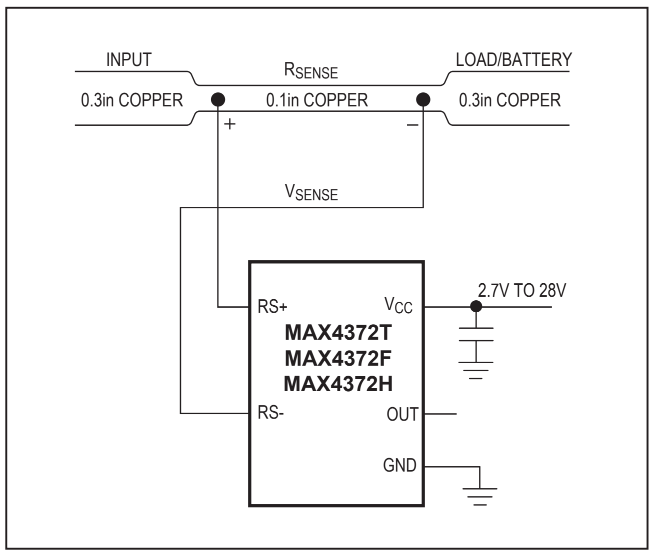


Figure 2. Connections Showing Use of PC Board

UCSP Applications Information

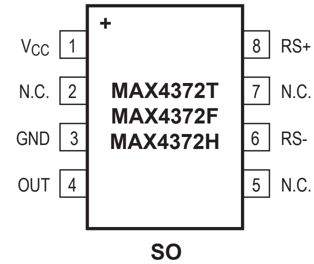
For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, go to the Maxim's website at www.maxim-ic.com/ucsp to find the Application Note: *UCSP—A Wafer-Level Chip-Scale Package*.

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4372FEUK+T	-40°C to +85°C	5 SOT23	ADIV
MAX4372FESA+	-40°C to +85°C	8 SO	—
MAX4372FEBT+T	-40°C to +85°C	3 x 2 UCSP	ACX
MAX4372HEUK+T	-40°C to +85°C	5 SOT23	ADIW
MAX4372HESA+	-40°C to +85°C	8 SO	—
MAX4372HEBT+T	-40°C to +85°C	3 x 2 UCSP	ACZ

+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Pin Configurations (continued)



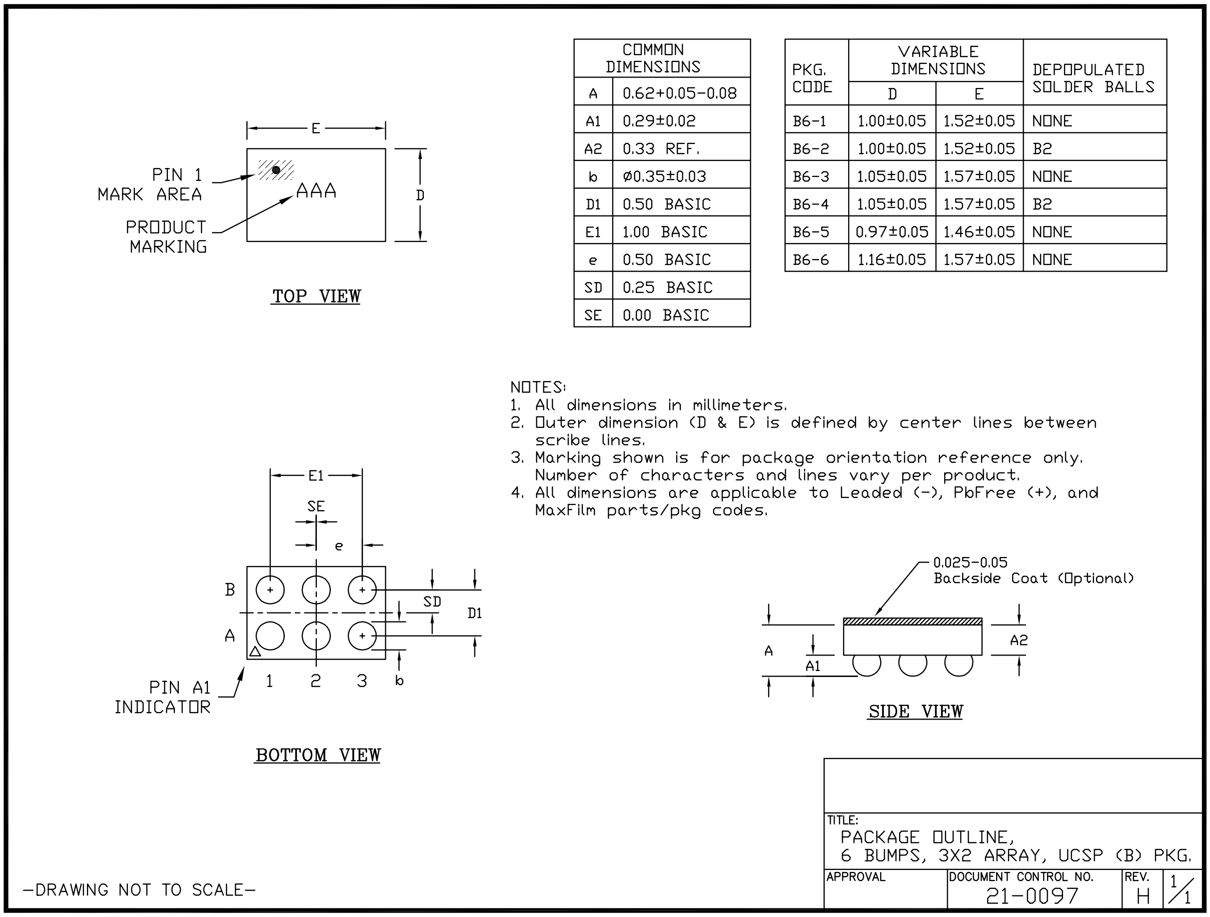
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	U5+1	21-0057	90-0174
8 SO	S8+2	21-0041	90-0096
5 UCSP	B6+2	21-0097	—



COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	0.50 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.00 BASIC

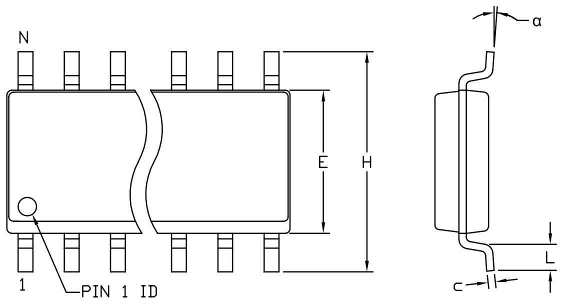
PKG. CODE	VARIABLE DIMENSIONS D	VARIABLE DIMENSIONS E	DEPOPULATED SOLDER BALLS
B6-1	1.00±0.05	1.52±0.05	NONE
B6-2	1.00±0.05	1.52±0.05	B2
B6-3	1.05±0.05	1.57±0.05	NONE
B6-4	1.05±0.05	1.57±0.05	B2
B6-5	0.97±0.05	1.46±0.05	NONE
B6-6	1.16±0.05	1.57±0.05	NONE

NOTES:
1. All dimensions in millimeters.
2. Outer dimension (D & E) is defined by center lines between scribe lines.
3. Marking shown is for package orientation reference only. Number of characters and lines vary per product.
4. All dimensions are applicable to Leaded (-), PbFree (+), and MaxFilm parts/pkg codes.

Note: *MAX4372_EBT uses package code B6-2.*

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



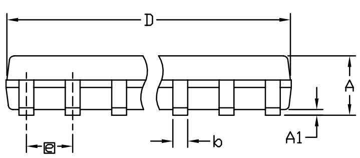
TOP VIEW

END VIEW

COMMON DIMENSIONS				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
b	.014	.019	0.35	0.49
c	.007	.010	0.19	0.25
E	.150	.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
α	0°	8°	0°	8°

VARIATION A				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.189	.197	4.80	5.00
N	8			
MS012	AA			
PKG. CODE	S8-2, S8-4, S8-5, S8-6F, S8-7F, S8-8F, S8-10F, S8-11F, S8-16F			

VARIATION B				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.337	.344	8.55	8.75
N	14			
MS012	AB			
PKG. CODE	S14-1, S14-4, S14-5, S14-6; S14M-4, S14M-5, S14M-6, S14M-7			



SIDE VIEW

VARIATION C				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.386	.394	9.80	10.00
N	16			
MS012	AC			
PKG. CODE	S16-1, S16-3, S16-5, S16-6, S16-8, S16-7F, S16-9F, S16-10F; S16M-3, S16M-6			

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 MM (.006") PER SIDE.
4. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
5. MEETS JEDEC MS012
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

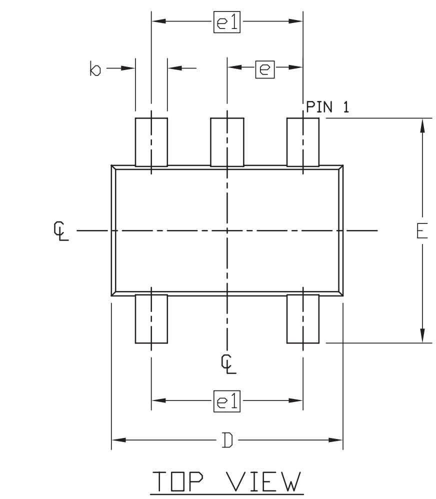
maxim integrated

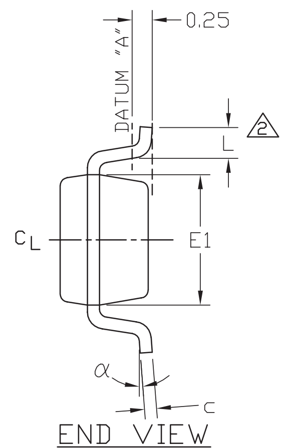
TITLE: PACKAGE OUTLINE, 8L, 14L, 16L SOIC .150 INCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	C	1/1

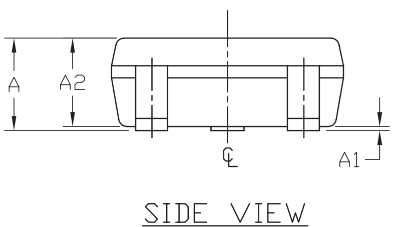
Package Information (continued)

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.





SYMBOL	MIN	NOM	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
c	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1	0.60 REF		
e	0.95 BSC.		
e1	1.90 BSC.		
α	0°	2.5°	8°



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. MEETS JEDEC MO178, VARIATION AA.
5. LEADS TO BE COPLANAR WITHIN 0.10 mm.
6. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
7. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
8. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.
9. PKG CODES: U5-1, U5-2

TITLE: PACKAGE OUTLINE, 5L SOT23

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0057	G	1/1

-DRAWING NOT TO SCALE-

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	7/09	Updated feature in accordance with actual performance of the product	1
5	5/11	Updated V_{RST} conditions to synchronize with tested material and added lead-free designation	1–3, 8

