6A, 2MHz Step-Down Regulator with Integrated Switches

ABSOLUTE MAXIMUM RATINGS

IN, PWRGD to GND .....-0.3V to +6V
V_{DD} to GND .....-0.3V to the lower of +4V or (V_{IN} + 0.3V)
COMP, FB, MODE, REFIN, CTL1, CTL2, SS, FREQ to GND .....-0.3V to (V_{DD} + 0.3V)
OUT, EN to GND .....-0.3V to +6V
BST to LX .....-0.3V to +6V
BST to GND .....-0.3V to +12V
PGND to GND .....-0.3V to +0.3V
LX to PGND .....-0.3V to the lower of +6V or (V_{IN} + 0.3V)
LX to PGND .....-1V to the lower of +6V or (V_{IN} + 1V) for 50ns
$I_{LX(RMS)}$ (Note 1) 6A
V_{DD} Output Short-Circuit Duration .....Continuous
Converter Output Short-Circuit Duration .....Continuous
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 27.8mW/°C above +70°C) 2222mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W
Junction-to-Case Resistance (θ_{JC}) .....6°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{EN} = 5V, C_{VDD} = 2.2µF, T_A = T_J = -40°C to +85°C, typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN						
IN Voltage Range			2.9		5.5	V
IN Supply Current	f_S = 1MHz, no load	V_{IN} = 3.3V		4.9	8	mA
		V_{IN} = 5V		5.2	8.5	
Total Shutdown Current from IN	V_{IN} = 5V, V_{EN} = 0V			10	20	µA
	V_{IN} = V_{DD} = 3.3V, V_{EN} = 0V			45		
3.3V LDO (V_{DD})						
V_{DD} Undervoltage Lockout Threshold	LX starts/stops switching	V_{DD} rising		2.6	2.8	V
		V_{DD} falling	2.35	2.55		
		Minimum glitch-width rejection		10		µs
V_{DD} Output Voltage	V_{IN} = 5V, I_{VDD} = 0 to 10mA		3.1	3.3	3.5	V
V_{DD} Dropout	V_{IN} = 2.9V, I_{VDD} = 10mA				0.08	V
V_{DD} Current Limit	V_{IN} = 5V, V_{DD} = 0V		25	40		mA
BST						
BST Supply Current	V_{BST} = V_{IN} = 5V, V_{LX} = 0 or 5V, V_{EN} = 0V			0.025		µA
PWM COMPARATOR						
PWM Comparator Propagation Delay	10mV overdrive			20		ns
PWM Peak-to-Peak Ramp Amplitude				1		V
PWM Valley Amplitude				0.8		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = 5V, C_{VDD} = 2.2µF, T_A = T_J = -40°C to +85°C, typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ERROR AMPLIFIER						
COMP Clamp Voltage, High	V_{IN} = 2.9V to 5V, V_{FB} = 0.5V, V_{REFIN} = 0.6V			2		V
COMP Clamp Voltage, Low	V_{IN} = 2.9V to 5V, V_{FB} = 0.7V, V_{REFIN} = 0.6V			0.7		V
COMP Slew Rate	V_{FB} step from 0.5V to 0.7V in 10ns			1.6		V/µs
COMP Shutdown Resistance	From COMP to GND, V_{IN} = 3.3V, V_{COMP} = 100mV, V_{EN} = V_{SS} = 0V			6		Ω
Internally Preset Output Voltage Accuracy	V_{REFIN} = V_{SS}, MODE = GND		-1		+1	%
FB Set-Point Value	CTL1 = CTL2 = GND, MODE = GND		0.594	0.6	0.606	V
FB to OUT Resistor	All VID settings except CTL1 = CTL2 = GND		5.5	8	10.5	kΩ
Open-Loop Voltage Gain				115		dB
Error-Amplifier Unity-Gain Bandwidth				28		MHz
Error-Amplifier and REFIN Common-Mode Input Range	V_{DD} = 2.9V to 3.5V		0		V_{DD} - 2	V
Error-Amplifier Maximum Output Current	V_{COMP} = 1V, V_{REFIN} = 0.6V	V_{FB} = 0.7V, sinking	1			mA
		V_{FB} = 0.5V, sourcing	-1			
FB Input Bias Current	CTL1 = CTL2 = GND			-125		nA
CTL_						
CTL_ Input Bias Current	$V_{CTL\_}$ = 0V			-7.2		µA
	$V_{CTL\_}$ = V_{DD}			7.2		
CTL_ Input Threshold	Low, falling			0.8		V
	Open			V_{DD}/2		
	High, rising			V_{DD} - 0.8		
Hysteresis	All VID transitions			50		mV
REFIN						
REFIN Input Bias Current	V_{REFIN} = 0.6V			-185		nA
REFIN Offset Voltage	V_{REFIN} = 0.9V, FB shorted to COMP		-4.5		+4.5	mV
LX (All Pins Combined)						
LX On-Resistance, High Side	I_{LX} = -2A	V_{IN} = V_{BST} - V_{LX} = 3.3V		35		mΩ
		V_{IN} = V_{BST} - V_{LX} = 5V		26	45	
LX On-Resistance, Low Side	I_{LX} = 2A	V_{IN} = 3.3V		25		mΩ
		V_{IN} = 5V		20	35	
LX Current-Limit Threshold	High-side sourcing		9	11		A
	Low-side sinking			11		
	Zero-crossing current threshold, MODE = V_{DD}			0.2		
LX Leakage Current	V_{IN} = 5V, V_{EN} = 0V	V_{LX} = 0V		-0.01		µA
		V_{LX} = 5V		-0.01		

6A, 2MHz Step-Down Regulator with Integrated Switches

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = 5V, C_{VDD} = 2.2µF, T_A = T_J = -40°C to +85°C, typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LX Switching Frequency	V_{IN} = 2.9V to 5.5V	R_{FREQ} = 49.9kΩ	0.9	1	1.1	MHz
		R_{FREQ} = 23.6kΩ	1.8	2	2.2	
Switching Frequency Range			500		2000	kHz
LX Minimum Off-Time					78	ns
LX Maximum Duty Cycle	R_{FREQ} = 49.9kΩ		92	95		%
LX Minimum Duty Cycle	R_{FREQ} = 49.9kΩ			5	15	%
Average Short-Circuit IN Supply Current	OUT connected to GND, V_{IN} = 5V			0.35		A
RMS LX Output Current			6			A
ENABLE						
EN Input Logic-Low Threshold	EN falling				0.9	V
EN Input Logic-High Threshold	EN rising		1.5			V
EN Input Current	V_{EN} = 0 or 5V, V_{IN} = 5V			0.01		µA
MODE						
MODE Input-Logic Threshold	Logic-low, falling			26		%V_{DD}
	Logic V_{DD}/2 or open, rising			50		
	Logic-high, rising			74		
MODE Input-Logic Hysteresis	MODE falling			5		%V_{DD}
MODE Input Bias Current	MODE = GND			-5		µA
	MODE = V_{DD}			5		
SS						
SS Current	V_{SS} = 0.45V, V_{REFIN} = 0.6V, sourcing		6.7	8	9.3	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	Rising			165		°C
Thermal-Shutdown Hysteresis				25		°C
POWER GOOD (PWRGD)						
Power-Good Threshold Voltage	V_{FB} falling, V_{REFIN} = 0.6V		88	90	92	% V_{REFIN}
	V_{FB} rising, V_{REFIN} = 0.6V			92.5		
Power-Good Edge Deglitch	V_{FB} rising or falling			48		Clock cycles
PWRGD Output-Voltage Low	I_{PWRGD} = 4mA			0.03	0.1	V
PWRGD Leakage Current	V_{IN} = V_{PWRGD} = 5V, V_{FB} = 0.7V, V_{REFIN} = 0.6V			0.01		µA
HICCUP OVERCURRENT LIMIT						
Current-Limit Startup Blanking				112		Clock cycles
Autoretry Restart Time				896		Clock cycles

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{EN} = 5V, C_{VDD} = 2.2µF, T_A = T_J = -40°C to +85°C, typical values are at T_A = +25°C, circuit of Figure 1, unless otherwise noted.) (Note 3)

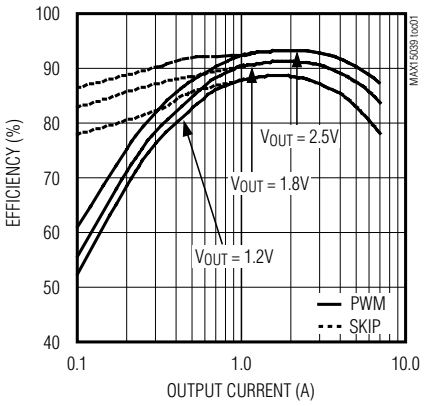
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FB Hiccup Threshold	V_{FB} falling		70		% V_{REFIN}
Hiccup Threshold Blanking Time	V_{FB} falling		28		µs

Note 3: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

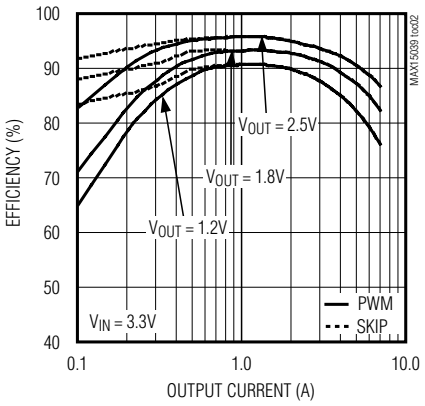
Typical Operating Characteristics

(Typical values are V_{IN} = V_{EN} = 5V, V_{OUT} = 1.8V, R_{FREQ} = 49.9kΩ, I_{OUT} = 6A, T_A = +25°C, circuit of Figure 1, unless otherwise noted.)

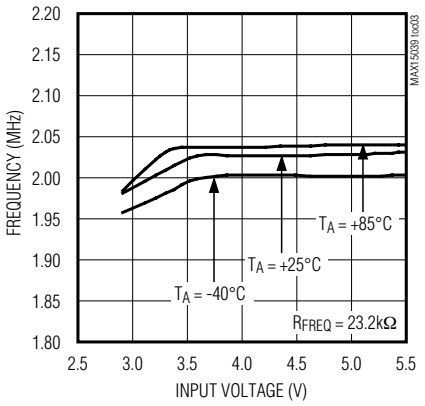
EFFICIENCY vs. OUTPUT CURRENT



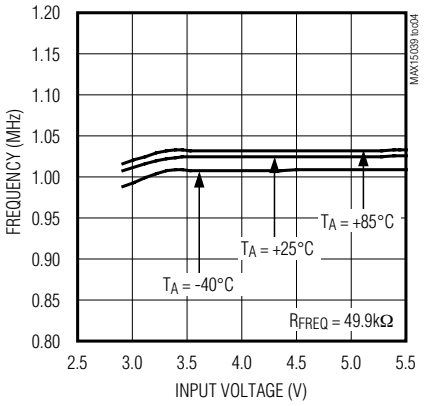
EFFICIENCY vs. OUTPUT CURRENT



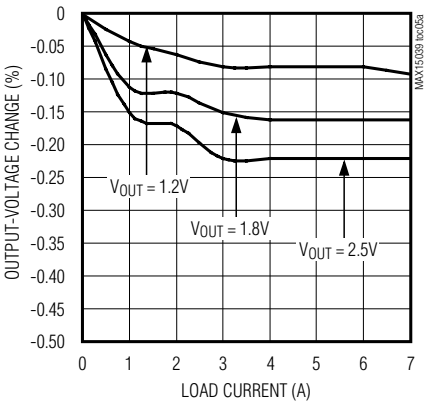
FREQUENCY vs. INPUT VOLTAGE



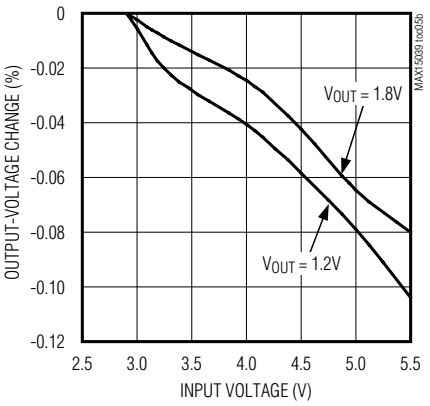
FREQUENCY vs. INPUT VOLTAGE



LOAD REGULATION



LINE REGULATION (LOAD = 6A)

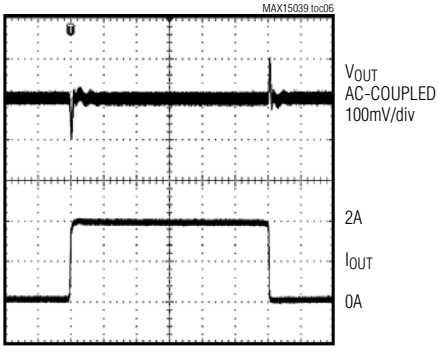


6A, 2MHz Step-Down Regulator with Integrated Switches

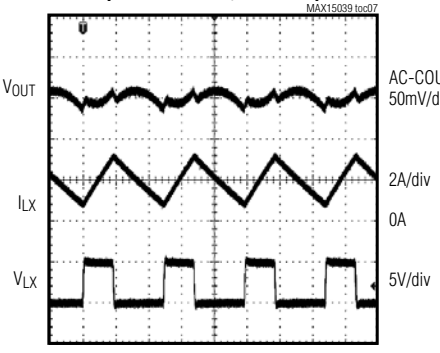
Typical Operating Characteristics (continued)

(Typical values are V_{IN} = V_{EN} = 5V, V_{OUT} = 1.8V, R_{FREQ} = 49.9kΩ, I_{OUT} = 6A, T_A = +25°C, circuit of Figure 1, unless otherwise noted.)

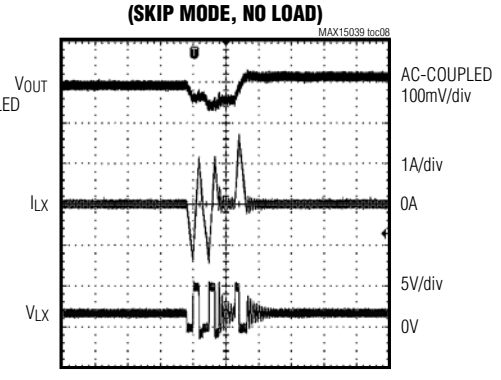
LOAD TRANSIENT



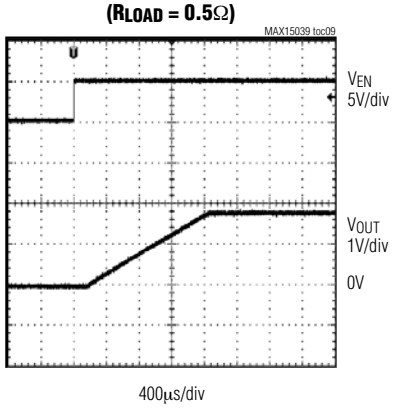
SWITCHING WAVEFORMS (FORCED PWM, 2A LOAD)



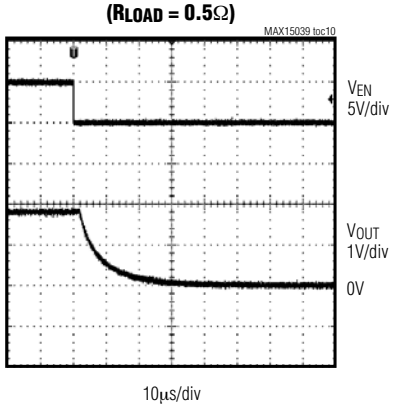
SWITCHING WAVEFORMS (SKIP MODE, NO LOAD)



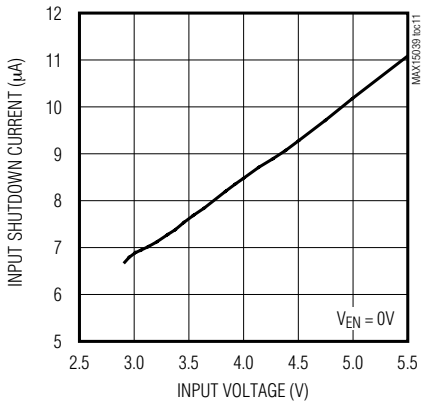
SOFT-START WAVEFORM (R_{LOAD} = 0.5Ω)



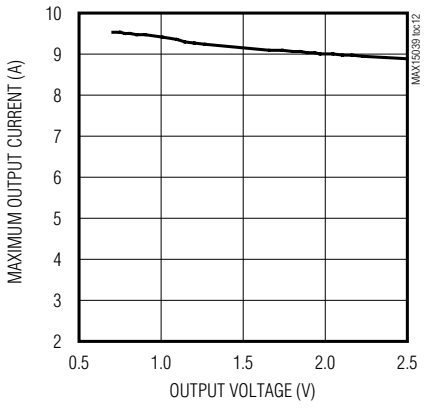
SHUTDOWN WAVEFORM (R_{LOAD} = 0.5Ω)



INPUT SHUTDOWN CURRENT vs. INPUT VOLTAGE



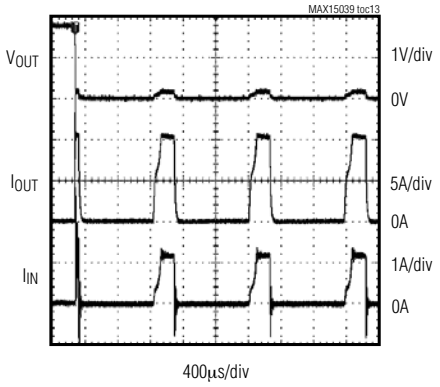
MAXIMUM OUTPUT CURRENT vs. OUTPUT VOLTAGE



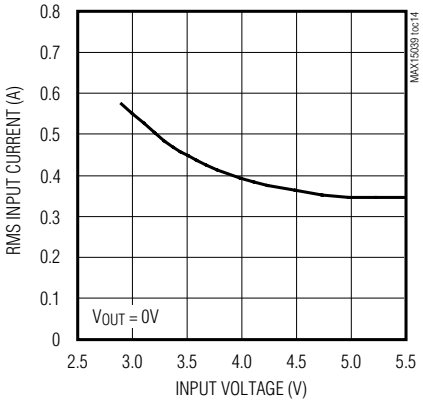
Typical Operating Characteristics (continued)

(Typical values are V_{IN} = V_{EN} = 5V, V_{OUT} = 1.8V, R_{FREQ} = 49.9kΩ, I_{OUT} = 6A, T_A = +25°C, circuit of Figure 1, unless otherwise noted.)

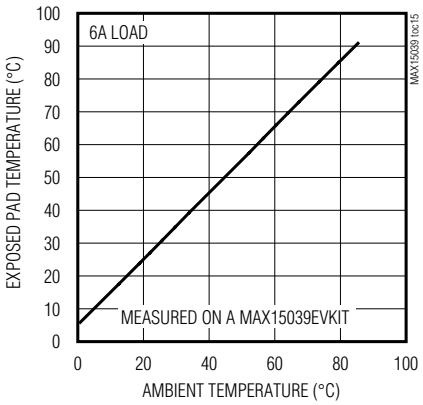
HICCUP CURRENT LIMIT



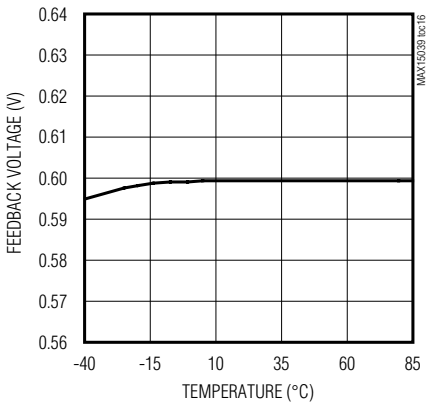
RMS INPUT CURRENT DURING SHORT CIRCUIT vs. INPUT VOLTAGE



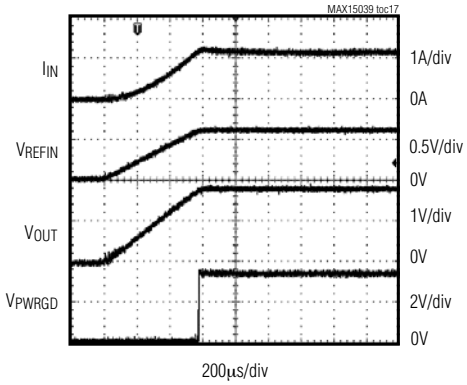
EXPOSED PAD TEMPERATURE vs. AMBIENT TEMPERATURE



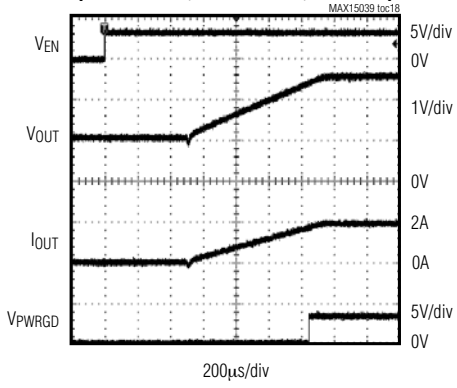
FEEDBACK VOLTAGE vs. TEMPERATURE



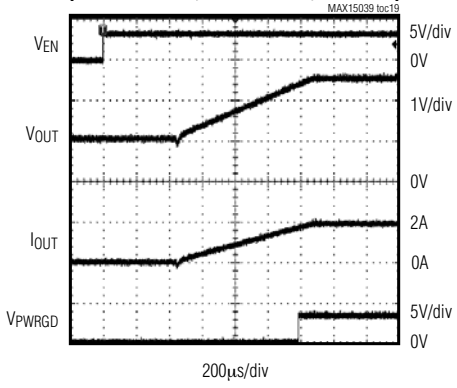
SOFT-START WITH REFIN



STARTING INTO PREBIASED OUTPUT (MODE = V_{DD}, V_{OUT} = 2.5V, 2A LOAD)



STARTING INTO PREBIASED OUTPUT (MODE = V_{DD}/2, V_{OUT} = 2.5V, 2A LOAD)

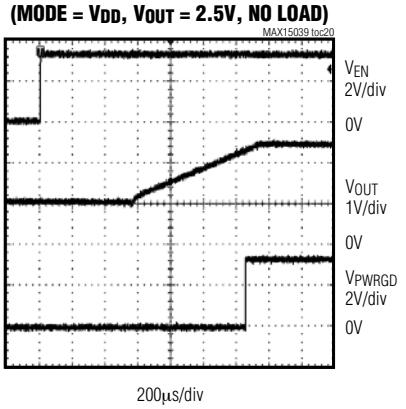


6A, 2MHz Step-Down Regulator with Integrated Switches

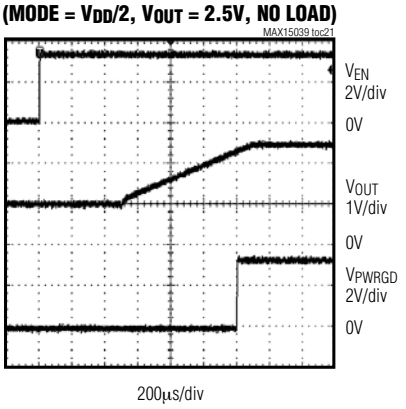
Typical Operating Characteristics (continued)

(Typical values are V_{IN} = V_{EN} = 5V, V_{OUT} = 1.8V, R_{FREQ} = 49.9kΩ, I_{OUT} = 6A, T_A = +25°C, circuit of Figure 1, unless otherwise noted.)

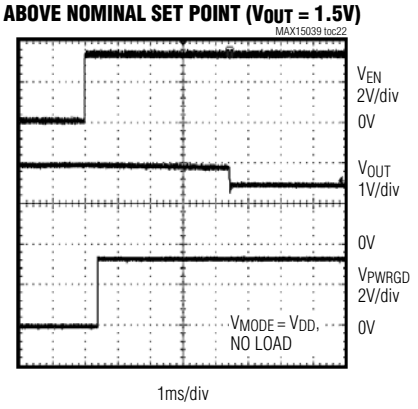
STARTING INTO PREBIASED OUTPUT (MODE = V_{DD}, V_{OUT} = 2.5V, NO LOAD)



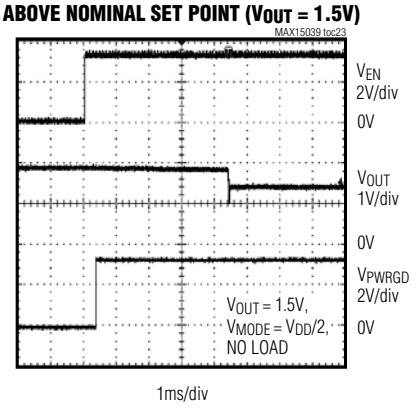
STARTING INTO PREBIASED OUTPUT (MODE = V_{DD}/2, V_{OUT} = 2.5V, NO LOAD)



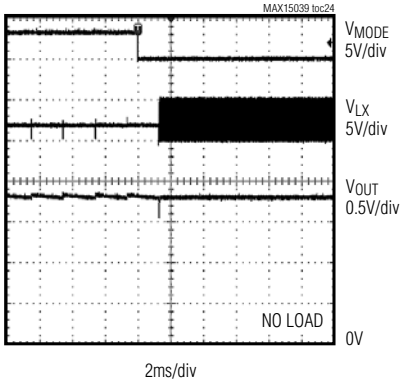
STARTING INTO PREBIASED OUTPUT ABOVE NOMINAL SET POINT (V_{OUT} = 1.5V)



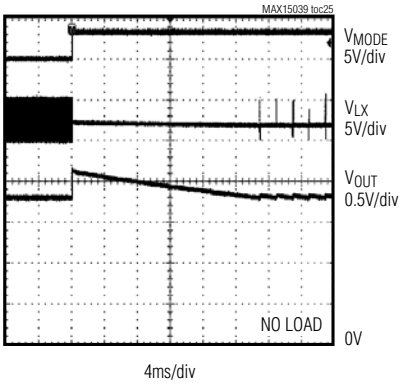
STARTING INTO PREBIASED OUTPUT ABOVE NOMINAL SET POINT (V_{OUT} = 1.5V)



TRANSITION FROM SKIP MODE TO FORCED PWM MODE



TRANSITION FROM FORCED PWM MODE TO SKIP MODE

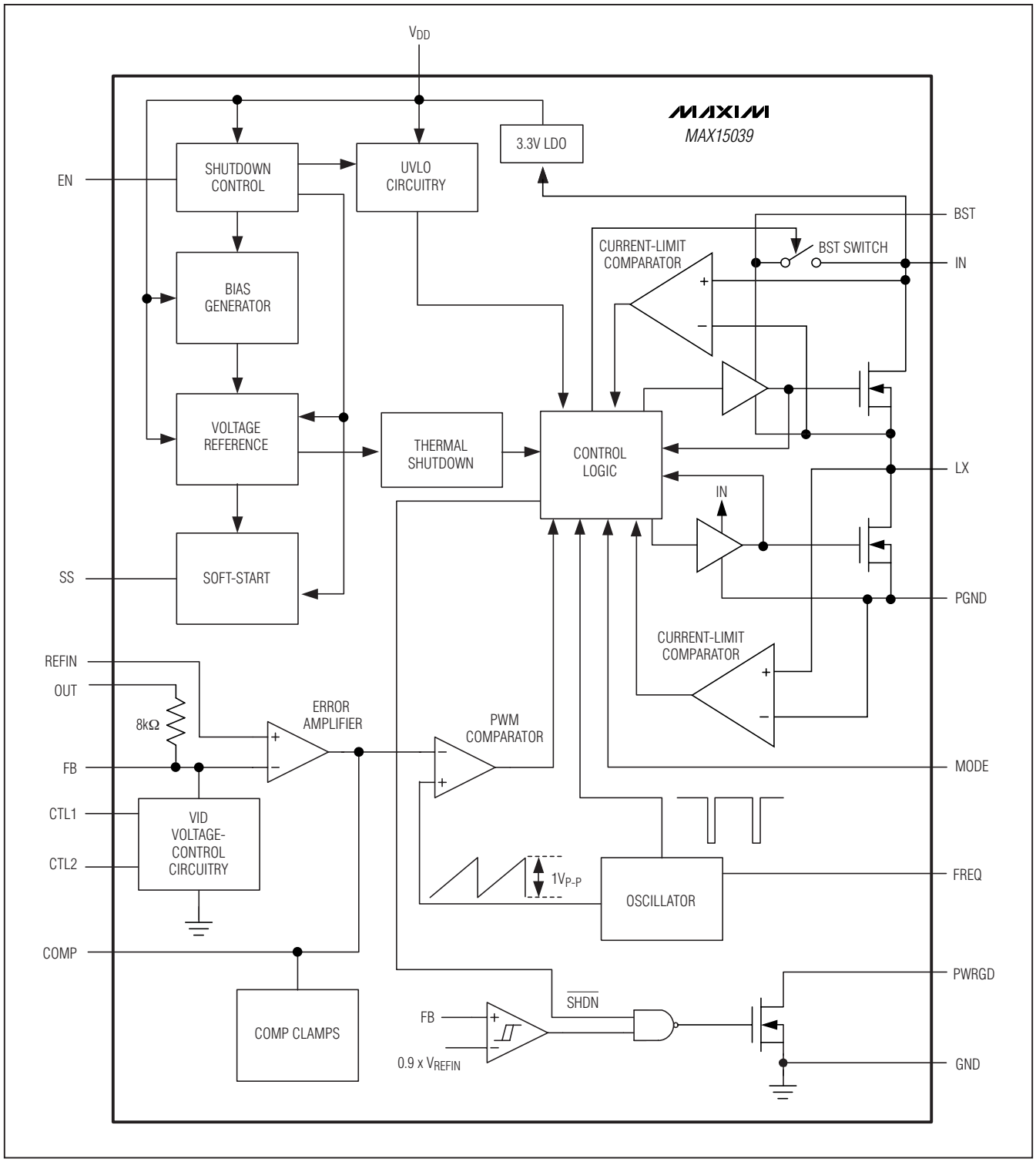


Pin Description

PIN	NAME	FUNCTION
1	MODE	Functional Mode Selection Input. See the *MODE Selection* section for more information.
2	V_{DD}	3.3V LDO Output. Supply input for the internal analog core. Connect a low-ESR, ceramic capacitor with a minimum value of 2.2µF from V_{DD} to GND.
3	CTL1	Preset Output-Voltage Selection Inputs. CTL1 and CTL2 set the output voltage to one of nine preset voltages. See Table 1 and the *Programming the Output Voltage (CTL1, CTL2)* section for preset voltages.
4	CTL2	
5	REFIN	External Reference Input. Connect REFIN to SS to use the internal 0.6V reference. Connecting REFIN to an external voltage forces FB to regulate to the voltage applied to REFIN. REFIN is internally pulled to GND when the IC is in shutdown/hiccup mode.
6	SS	Soft-Start Input. Connect a capacitor from SS to GND to set the startup time. Use a capacitor with a 1nF minimum value. See the *Soft-Start and REFIN* section for details on setting the soft-start time.
7	GND	Analog Ground Connection. Connect GND and PGND together at one point near the input bypass capacitor return terminal.
8	COMP	Voltage Error-Amplifier Output. Connect the necessary compensation network from COMP to FB and OUT. COMP is internally pulled to GND when the IC is in shutdown/hiccup mode.
9	FB	Feedback Input. Connect FB to the center tap of an external resistive divider from the output to GND to set the output voltage from 0.6V to 90% of V_{IN}. Connect FB through an RC network to the output when using CTL1 and CTL2 to select any of nine preset voltages.
10	OUT	Output-Voltage Sense. Connect to the converter output. Leave OUT unconnected when an external resistive divider is used.
11	FREQ	Oscillator Frequency Select. Connect a precision resistor from FREQ to GND to select the switching frequency. See the *Frequency Select (FREQ)* section.
12	PWRGD	Open-Drain, Power-Good Output. PWRGD is high impedance when V_{FB} rises above 92.5% (typ) of V_{REFIN} and V_{REFIN} is above 0.54V. PWRGD is internally pulled low when V_{FB} falls below 90% (typ) of V_{REFIN} or V_{REFIN} is below 0.54V. PWRGD is internally pulled low when the IC is in shutdown mode, V_{DD} is below the internal UVLO threshold, or the IC is in thermal shutdown.
13	BST	High-Side MOSFET Driver Supply. Internally connected to IN through a pMOS switch. Bypass BST to LX with a 0.1µF capacitor.
14, 15, 16	LX	Inductor Connection. All LX pins are internally shorted together. Connect all LX pins to the switched side of the inductor. LX is high impedance when the IC is in shutdown mode.
17–20	PGND	Power Ground. Connect all PGND pins externally to the power ground plane. Connect all PGND pins together near the IC.
21, 22, 23	IN	Input Power Supply. Input supply range is from 2.9V to 5.5V. Bypass IN to PGND with a 22µF ceramic capacitor.
24	EN	Enable Input. Logic input to enable/disable the MAX15039.
—	EP	Exposed Pad. Solder EP to a large contiguous copper plane connected to PGND to optimize thermal performance. Do not use EP as a ground connection for the device.

6A, 2MHz Step-Down Regulator with Integrated Switches

Block Diagram



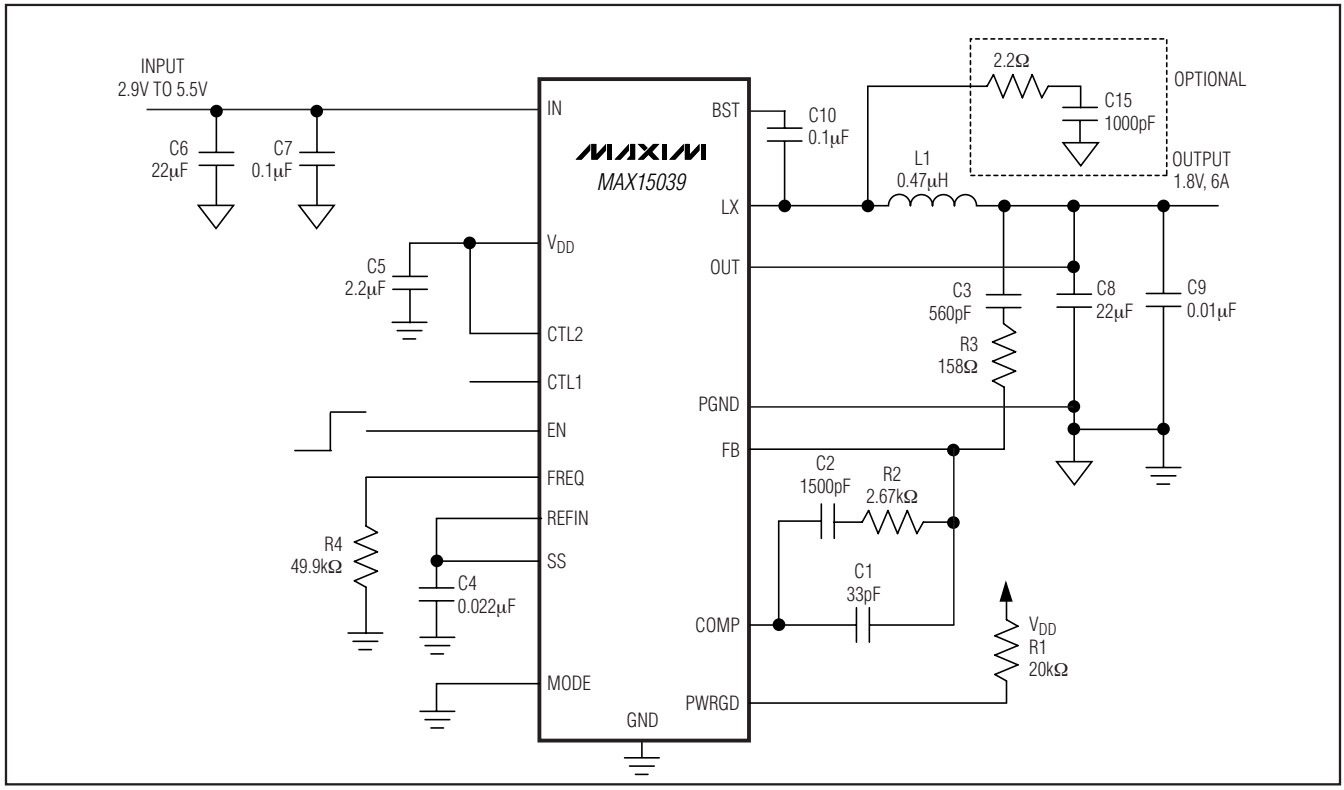


Figure 1. Typical Application Circuit: 1MHz, All-Ceramic-Capacitor Design with V_{IN} = 2.9V to 5.5V and V_{OUT} = 1.8V

Detailed Description

The MAX15039 high-efficiency, voltage-mode switching regulator delivers up to 6A of output current. The MAX15039 provides output voltages from 0.6V to 0.9 x V_{IN} from 2.9V to 5.5V input supplies, making it ideal for on-board point-of-load applications. The output-voltage accuracy is better than ±1% over load, line, and temperature.

The MAX15039 features a wide switching frequency range, allowing the user to achieve all-ceramic-capacitor designs and fast transient responses (see Figure 1). The high operating frequency minimizes the size of external components. The MAX15039 is available in a small (4mm x 4mm), lead-free, 24-pin thin QFN package. The REFIN function makes the MAX15039 an ideal candidate for DDR and tracking power supplies. Using internal low-$R_{DS(ON)}$ (20mΩ for the low-side n-channel MOSFET and 26mΩ for the high-side n-channel MOSFET) maintains high efficiency at both heavy-load and high-switching frequencies.

The MAX15039 employs voltage-mode control architecture with a high bandwidth (28MHz) error amplifier. The voltage-mode control architecture allows up to 2MHz switching frequency, reducing board area. The op amp voltage-error amplifier works with type III compensation to fully utilize the bandwidth of the high-frequency switching to obtain fast transient response. Adjustable soft-start time provides flexibilities to minimize input startup inrush current. An open-drain, power-good (PWRGD) output goes high when V_{FB} reaches 92.5% of V_{REFIN} and V_{REFIN} is greater than 0.54V.

The MAX15039 provides an option for three modes of operation: regular PWM, PWM mode with monotonic startup into prebiased output, or skip mode with monotonic startup into prebiased output.

6A, 2MHz Step-Down Regulator with Integrated Switches

Controller Function

The controller logic block is the central processor that determines the duty cycle of the high-side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current-limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator and generates the driver signals for both high-side and low-side MOSFETs. The break-before-make logic and the timing for charging the bootstrap capacitors are calculated by the controller logic block. The error signal from the voltage-error amplifier is compared with the ramp signal generated by the oscillator at the PWM comparator and, thus, the required PWM signal is produced. The high-side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the V_{COMP} signal or the current-limit threshold is exceeded. The low-side switch is then turned on for the remainder of the oscillator cycle.

Current Limit

The internal, high-side MOSFET has a typical 11A peak current-limit threshold. When current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. The synchronous rectifier remains on until the inductor current falls below the low-side current limit. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. The MAX15039 uses a hiccup mode to prevent overheating during short-circuit output conditions.

During current limit, if V_{FB} drops below 70% of V_{REFIN} and stays below this level for 12µs or more, the MAX15039 enters hiccup mode. The high-side MOSFET and the synchronous rectifier are turned off and both COMP and REFIN are internally pulled low. If REFIN and SS are connected together, both are pulled low. The part remains in this state for 896 clock cycles and then attempts to restart for 112 clock cycles. If the fault causing current limit has cleared, the part resumes normal operation. Otherwise, the part reenters hiccup mode again.

Soft-Start and REFIN

The MAX15039 utilizes an adjustable soft-start function to limit inrush current during startup. An 8µA (typ) current source charges an external capacitor connected to SS. The soft-start time is adjusted by the value of the external capacitor from SS to GND. The required capacitance value is determined as:

$$C = \frac{8\mu A \times t_{SS}}{0.6V}$$

where t_{SS} is the required soft-start time in seconds. The MAX15039 also features an external reference input (REFIN). The IC regulates FB to the voltage applied to REFIN. The internal soft-start is not available when using an external reference. A method of soft-start when using an external reference is shown in Figure 2. Connect REFIN to SS to use the internal 0.6V reference. Use a capacitor of 1nF minimum value at SS.

Undervoltage Lockout (UVLO)

The UVLO circuitry inhibits switching when V_{DD} is below 2.55V (typ). Once V_{DD} rises above 2.6V (typ), UVLO clears and the soft-start function activates. A 50mV hysteresis is built in for glitch immunity.

BST

The gate-drive voltage for the high-side, n-channel switch is generated by a flying-capacitor boost circuit. The capacitor between BST and LX is charged from the V_{IN} supply while the low-side MOSFET is on. When the low-side MOSFET is switched off, the voltage of the capacitor is stacked above LX to provide the necessary turn-on voltage for the high-side internal MOSFET.

Frequency Select (FREQ)

The switching frequency is resistor programmable from 500kHz to 2MHz. Set the switching frequency of the IC with a resistor (R_{FREQ}) connected from FREQ to GND. R_{FREQ} is calculated as:

$$R_{FREQ} = \frac{50k\Omega}{0.95\mu s} \times \left(\frac{1}{f_S} - 0.05\mu s\right)$$

where f_S is the desired switching frequency in Hertz.

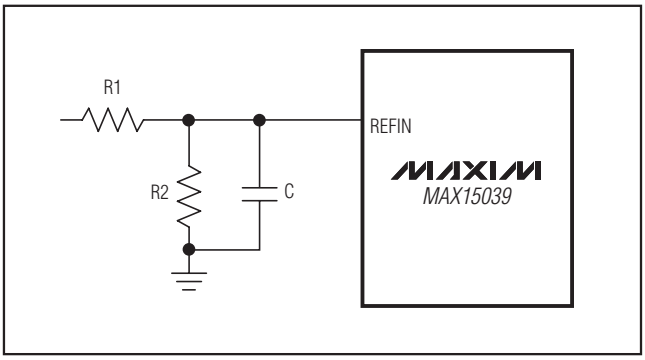


Figure 2. Typical Soft-Start Implementation with External Reference

Power-Good Output (PWRGD)

PWRGD is an open-drain output that goes high impedance when V_{FB} is above 0.925 x V_{REFIN} and V_{REFIN} is above 0.54V for at least 48 clock cycles. PWRGD pulls low when V_{FB} is below 90% of V_{REFIN} or V_{REFIN} is below 0.54V for at least 48 clock cycles. PWRGD is low when the IC is in shutdown mode, V_{DD} is below the internal UVLO threshold, or the IC is in thermal shutdown mode.

Programming the Output Voltage (CTL1, CTL2)

As shown in Table 1, the output voltage is pin programmable by the logic states of CTL1 and CTL2. CTL1 and CTL2 are trilevel inputs: V_{DD}, unconnected, and GND. An 8.06kΩ resistor must be connected between OUT and FB when CTL1 and CTL2 are connected to GND. The logic states of CTL1 and CTL2 should be programmed only before power-up. Once the part is enabled, CTL1 and CTL2 should not be changed. If the output voltage needs to be reprogrammed, cycle power or EN and reprogram before enabling. The output voltage can be programmed continuously from 0.6V to 90% of V_{IN} by using a resistor-divider network from V_{OUT} to FB to GND as shown in Figure 3a. CTL1 and CTL2 must be connected to GND.

Shutdown Mode

Drive EN to GND to shut down the IC and reduce quiescent current to 10µA (typ). During shutdown, the LX is high impedance. Drive EN high to enable the MAX15039.

Thermal Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J = +165°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, causing a pulsed output during continuous overload conditions. The soft-start sequence begins after recovery from a thermal-shutdown condition.

Applications Information

IN and V_{DD} Decoupling

To decrease the noise effects due to the high switching frequency and maximize the output accuracy of the MAX15039, decouple IN with a 22µF capacitor from IN to PGND. Also, decouple V_{DD} with a 2.2µF low-ESR ceramic capacitor from V_{DD} to GND. Place these capacitors as close as possible to the IC.

Table 1. CTL1 and CTL2 Output Voltage Selection

CTL1	CTL2	V_{OUT} (V)	V_{OUT} WHEN USING EXTERNAL REFIN (V)
GND	GND	0.6* or 0.6 < V_{OUT} ≤ 0.9 x V_{IN}**	V_{REFIN}* or V_{REFIN} < V_{OUT} ≤ 0.9 x V_{IN}**
V_{DD}	V_{DD}	0.7	V_{REFIN} x (7/6)
GND	Unconnected	0.8	V_{REFIN} x (4/3)
GND	V_{DD}	1.0	V_{REFIN} x (5/3)
Unconnected	GND	1.2	V_{REFIN} x 2
Unconnected	Unconnected	1.5	V_{REFIN} x 2.5
Unconnected	V_{DD}	1.8	V_{REFIN} x 3
V_{DD}	GND	2.0	V_{REFIN} x (10/3)
V_{DD}	Unconnected	2.5	V_{REFIN} x (25/6)

**Install an 8.06kΩ resistor at R3 and do not install a resistor at R4.*
***Install R3 and R4 following the equation in the* Compensation Design *section (see Figure 3a).*

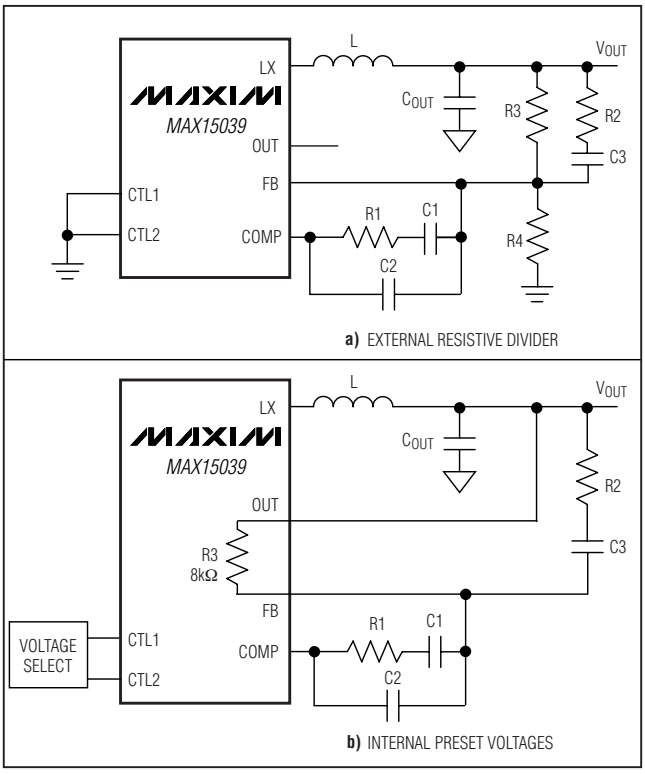


Figure 3. Type III Compensation Network

6A, 2MHz Step-Down Regulator with Integrated Switches

Inductor Selection

Choose an inductor with the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_S \times V_{IN} \times LIR \times I_{OUT(MAX)}}$$

where LIR is the ratio of the inductor ripple current to full load current at the minimum duty cycle. Choose LIR between 20% to 40% for best performance and stability.

Use an inductor with the lowest possible DC resistance that fits in the allotted dimensions. Powdered iron ferrite core types are often the best choice for performance. With any core material, the core must be large enough not to saturate at the current limit of the MAX15039.

Output-Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Estimate the output-voltage ripple due to the output capacitance, ESR, and ESL:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times C_{OUT} \times f_S}$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL$$

or:

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{OFF}} \times ESL$$

or whichever is larger.

The peak-to-peak inductor current (I_{P-P}) is:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Use these equations for initial output-capacitor selection. Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output-voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output-voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

Load-transient response depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to its predetermined value. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, preventing the output from deviating further from its regulating value. See the *Compensation Design* section for more details.

Input-Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. The total input capacitance must be equal or greater than the value given by the following equation to keep the input-ripple voltage within specification and minimize the high-frequency ripple current being fed back to the input source:

$$C_{IN\_MIN} = \frac{D \times T_S \times I_{OUT}}{V_{IN\text{-}RIPPLE}}$$

where $V_{IN\text{-}RIPPLE}$ is the maximum allowed input ripple voltage across the input capacitors and is recommended to be less than 2% of the minimum input voltage. D is the duty cycle (V_{OUT}/V_{IN}) and T_S is the switching period ($1/f_S$).

The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source, but are instead shunted through the input capacitor. The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{RIPPLE} is the input RMS ripple current.

Compensation Design

The power transfer function consists of one double pole and one zero. The double pole is introduced by the inductor L and the output capacitor C_O. The ESR of the output capacitor determines the zero. The double pole and zero frequencies are given as follows:

$$f_{P1\_LC} = f_{P2\_LC} = \frac{1}{2\pi \times \sqrt{L \times C_O \times \left(\frac{R_O + ESR}{R_O + R_L}\right)}}$$

$$f_{Z\_ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

where R_L is equal to the sum of the output inductor's DCR (DC resistance) and the internal switch resistance, $R_{DS(ON)}$. A typical value for $R_{DS(ON)}$ is 20mΩ (low-side MOSFET) and 26mΩ (high-side MOSFET). R_O is the output load resistance, which is equal to the rated output voltage divided by the rated output current. ESR is the total equivalent series resistance of the output capacitor. If there is more than one output capacitor of the same type in parallel, the value of the ESR in the above equation is equal to that of the ESR of a single output capacitor divided by the total number of output capacitors.

The high switching frequency range of the MAX15039 allows the use of ceramic output capacitors. Since the ESR of ceramic capacitors is typically very low, the frequency of the associated transfer function zero is higher than the unity-gain crossover frequency, f_C, and the zero cannot be used to compensate for the double pole created by the output filtering inductor and capacitor. The double pole produces a gain drop of 40dB/decade and a phase shift of 180°. The compensation network error amplifier must compensate for this gain drop and phase shift to achieve a stable high-bandwidth closed-loop system. Therefore, use type III compensation as shown in Figures 3 and 4. Type III compensation possesses three poles and two zeros with the first pole, f_{P1_EA}, located at zero frequency (DC). Locations of other poles and zeros of the type III compensation are given by:

$$f_{Z1\_EA} = \frac{1}{2\pi \times R1 \times C1}$$

$$f_{Z2\_EA} = \frac{1}{2\pi \times R3 \times C3}$$

$$f_{P3\_EA} = \frac{1}{2\pi \times R1 \times C2}$$

$$f_{P2\_EA} = \frac{1}{2\pi \times R2 \times C3}$$

The above equations are based on the assumptions that C1 >> C2 and R3 >> R2 are true in most applications. Placements of these poles and zeros are determined by the frequencies of the double pole and ESR zero of the power transfer function. It is also a function of the desired close-loop bandwidth. The following section outlines the step-by-step design procedure to calculate the required compensation components for the MAX15039. When the output voltage of the MAX15039 is programmed to a preset voltage, R3 is internal to the IC and R4 does not exist (Figure 3b).

When externally programming the MAX15039 (Figure 3a), the output voltage is determined by:

$$R4 = \frac{0.6 \times R3}{(V_{OUT} - 0.6)} \text{ (for } V_{OUT} > 0.6V\text{)}$$

or:

$$R4 = \frac{(V_{REFIN} \times R3)}{(V_{OUT} - V_{REFIN})}$$

if using an external V_{REFIN}, and $V_{OUT} > V_{REFIN}$.

For a 0.6V output, or for $V_{OUT} = V_{REFIN}$, connect an 8.06kΩ resistor from FB to V_{OUT}. The zero-cross frequency of the close-loop, f_C, should be between 10% and 20% of the switching frequency, f_S. A higher zero-cross frequency results in faster transient response. Once f_C is chosen, C1 is calculated from the following equation:

$$C1 = \frac{1.5625 \times \frac{V_{IN}}{V_{P-P}}}{2 \times \pi \times R3 \times (1 + \frac{R_L}{R_O}) \times f_C}$$

where V_{P-P} is the ramp peak-to-peak voltage (1V typ).

Due to the underdamped nature of the output LC double pole, set the two zero frequencies of the type III compensation less than the LC double-pole frequency to provide adequate phase boost. Set the two zero frequencies to 80% of the LC double-pole frequency. Hence:

$$R1 = \frac{1}{0.8 \times C1} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

$$C3 = \frac{1}{0.8 \times R3} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}}$$

6A, 2MHz Step-Down Regulator with Integrated Switches

$$R2 = \frac{C_O \times ESR}{C3}$$

Set the third compensation pole at 1/2 of the switching frequency. Calculate C2 as follows:

$$C2 = \frac{1}{\pi \times R1 \times f_S}$$

The above equations provide application compensation when the zero-cross frequency is significantly higher than the double-pole frequency. When the zero-cross frequency is near the double-pole frequency, the actual zero-cross frequency is higher than the calculated frequency. In this case, lowering the value of R1 reduces the zero-cross frequency. Also, set the third pole of the type III compensation close to the switching frequency if the zero-cross frequency is above 200kHz to boost the phase margin. The recommended range for R3 is 2kΩ to 10kΩ. Note that the loop compensation remains unchanged if only R4's resistance is altered to set different outputs.

MODE Selection

The MAX15039 features a mode selection input (MODE) that users can select a functional mode for the device (see Table 2).

Forced-PWM Mode

Connect MODE to GND to select forced-PWM mode. In forced-PWM mode, the MAX15039 operates at a constant switching frequency (set by the resistor at FREQ terminal) with no pulse skipping. PWM operation starts after a brief settling time when EN goes high. The low-side switch turns on first, charging the bootstrap capacitor to provide the gate-drive voltage for the high-side switch. The low-side switch turns off either at the end of the clock period or once the low-side switch sinks 1.35A current (typ), whichever occurs first. If the low-side switch is turned off before the end of the clock period, the high-side switch is turned on for the remaining part of the time interval until the inductor current reaches 0.9A, or the end of clock cycle is encountered.

Starting from the first PWM activity, the sink current threshold is increased through an internal 4-step DAC to reach the current limit of 11A after 128 clock periods. This is done to help a smooth recovery of the regulated voltage even in case of accidental prebiased output in spite of the initial forced-PWM mode selection.

Table 2. Mode Selection

MODE CONNECTION	OPERATION MODE
GND	Forced PWM
Unconnected or $V_{DD}/2$	Forced PWM. Soft-start up into a prebiased output (monotonic startup).
V_{DD}	Skip Mode. Soft-start into a prebiased output (monotonic startup).

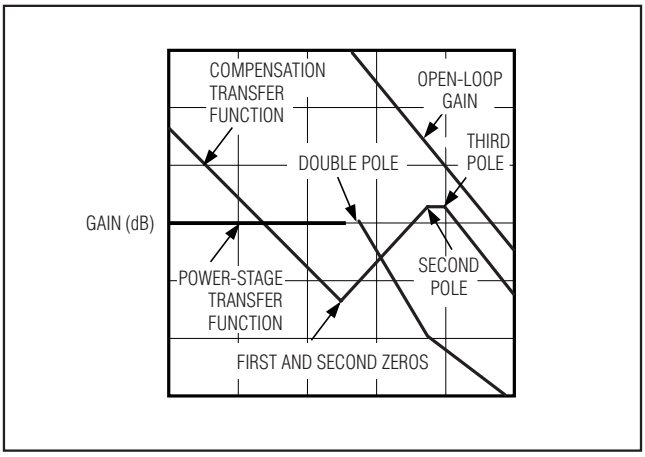


Figure 4. Type III Compensation Illustration

Soft-Starting Into a Prebiased Output Mode (Monotonic Startup)

When MODE is left unconnected or biased to $V_{DD}/2$, the MAX15039 soft-starts into a prebiased output without discharging the output capacitor. This type of operation is also termed monotonic startup. See the Starting Into Prebiased Output waveforms in the *Typical Operating Characteristics* section for an example.

In monotonic startup mode, both low-side and high-side switches remain off to avoid discharging the prebiased output. PWM operation starts when the FB voltage crosses the SS voltage. As in forced-PWM mode, the PWM activity starts with the low-side switch turning on first to build the bootstrap capacitor charge.

The MAX15039 is also able to start into prebiased with the output above the nominal set point without abruptly discharging the output, thanks to the sink current control of the low-side switch through a 4-step DAC in 128 clock cycles. Monotonic startup mode automatically switches to forced-PWM mode 4096 clock cycles delay after the voltage at FB increases above 92.5% of V_{REFIN}. The additional delay prevents an early transition from monotonic startup to forced-PWM mode during soft-start when a prolonged time constant external REFIN voltage is applied.

The maximum allowed soft-start time is 2ms when an external reference is applied at REFIN in the case of starting up into prebiased output.

Skip Mode

Connect MODE to V_{DD} to select skip mode. In skip mode, the MAX15039 switches only as necessary to maintain the output at light loads (not capable of sinking current from the output), but still operates with fixed-frequency (set by the resistor at FREQ terminal) PWM at medium and heavy loads. This maximizes light-load efficiency and reduces the input quiescent current.

In case of prolonged high-side idle activity (beyond eight clock cycles), the low-side switch is turned on briefly to rebuild the charge lost in the bootstrap capacitor before the next on-cycle of the high-side switch.

In skip mode, the low-side switch is turned off when the inductor current decreases to 0.2A (typ) to ensure no reverse current flowing from the output capacitor and the best conversion efficiency/minimum supply current.

The high-side switch minimum on-time is controlled to guarantee that 0.9A current is reached to avoid high frequency bursts at no load conditions and that might cause a rapid increase of the supply current caused by additional switching losses.

Even if skip mode is selected at the device turn-on, the monotonic startup mode is internally selected during soft-start. The transition to skip mode is automatically achieved 4096 clock cycles after the voltage at FB increases above 92.5% of V_{REFIN}.

Changing from skip mode to forced-PWM mode and vice-versa can be done at any time. The output capacitor should be large enough to limit the output-voltage overshoot/undershoot due to the settling times to reach different duty-cycle set points corresponding to forced-PWM mode and skip mode at light loads.

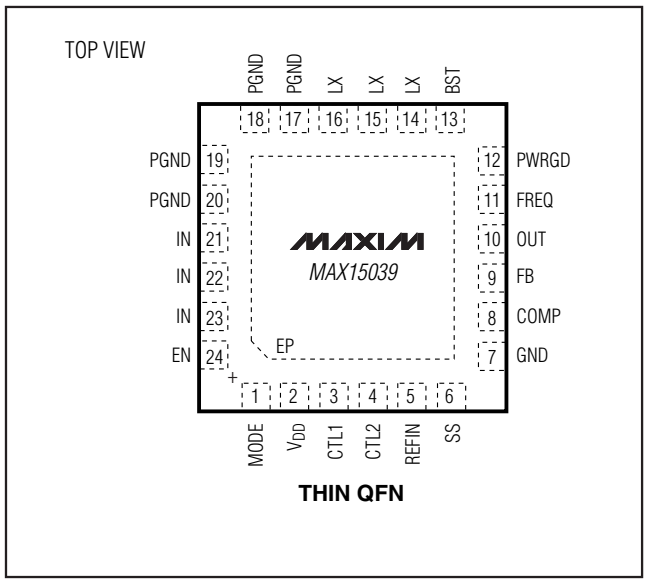
PCB Layout Considerations and Thermal Performance

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX15039 EV kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
2) Place capacitors on V_{DD}, IN, and SS as close as possible to the IC and its corresponding pin using direct traces. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the IC.
6) Route high-speed switching nodes, such as LX, away from sensitive analog areas (FB, COMP).

6A, 2MHz Step-Down Regulator with Integrated Switches

Pin Configuration



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444-4	21-0139	90-0022

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/08	Initial release	—
1	12/09	Updated the *Typical Operating Characteristics*.	5
2	5/10	Updated the *Electrical Characteristics*, Table 1, and the *Compensation Design* section.	3, 13, 15
3	12/10	Corrected error in C1 equation	15