ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND) Supply Voltage (VCC)	+6V
Control Input Voltage (RE, DE, SLR,	
H/F, TXP, RXP)	0.3V to +6V
Driver Input Voltage (DI)	
Driver Output Voltage (Z, Y, A, B)	8V to +13V
Receiver Input Voltage (A, B)	8V to +13V
Receiver Input Voltage	
Full Duplex (A, B)	
Receiver Output Voltage (RO)0.3V to	$(V_{CC} + 0.3V)$
Driver Output Current	±250mA

Continuous Power Dissipation ($T_A = +7$	70°C)	
8-Pin SO (derate 5.88mW/°C above +	-70°C)	471mW
8-Pin Plastic DIP (derate 9.09mW/°C	above +70°C)	727mW
14-Pin SO (derate 8.33mW/°C above		
14-Pin Plastic DIP (derate 10.0mW/°C	above +70°C)	800mW
Operating Temperature Ranges		
MAX1308_EC	0°C t	io +75°C
MAX1308_EE	40°C t	io +85°C
MAX1308_EA	40°C to	+125°C
Junction Temperature		+150°C
Storage Temperature Range	65°C to	+150°C
Lead Temperature (soldering, 10s)		+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = +5.0V \pm 10\%, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = +5.0V \text{ and } T_A = +25^{\circ}C.)$ (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN T	YP N	1AX	UNITS	
DRIVER	•			•			
V _{CC} Supply-Voltage Range	Vcc			4.5		5.5	V
		$R_L = 100\Omega$ (RS-422), Figure 1		3	\	/cc	
Differential Driver Output	V _{OD}	$R_L = 54\Omega$ (RS-485), Figure 1		2	\	/cc	V
		No load			\	/cc	
Change in Magnitude of Differential Output Voltage	ΔV _{OD}	$R_L = 100\Omega$ or 54Ω , Figure 1 (I	Note 2)		(0.2	V
Driver Common-Mode Output Voltage	Voc	$R_L = 100\Omega$ or 54Ω , Figure 1		VC	c/2	3	V
Change in Magnitude of Common-Mode Voltage	ΔV _{OC}	$R_L = 100\Omega$ or 54Ω , Figure 1 (I	Note 2)		(0.2	V
Input-High Voltage	VIH	DE, DI, $\overline{\text{RE}}$, TXP, RXP, H/ $\overline{\text{F}}$		3			V
Input-Low Voltage	V _{IL}	DE, DI, RE, TXP, RXP, HF			(8.0	V
Input Hysteresis	V _H YS	DE, DI, \overline{RE} , TXP, RXP, H/ \overline{F}		1	100		mV
Input Current	l _{IN1}	DE, DI, RE				±1	μΑ
Input Impedance First Transition		DE		1		10	kΩ
Input Current	I _{IN2}	TXP, RXP, H/F internal pulldov	wn	10		40	μΑ
SRL Input-High Voltage				V _{CC} - 0.4			V
SRL Input-Middle Voltage				V _{CC} x 0.3	Vcc	x 0.7	V
SRL Input-Low Voltage					(0.4	V
SI Israel Comment		SRL = V _{CC}				75	
SRL Input Current		SRL = GND		-75			μΑ
Output Leakage (Y and Z)	lo	DE = GND,	$V_{IN} = +12V$		-	125	μΑ
Full Duplex	Io	V _{CC} = GND or V _{CC}	$V_{IN} = -7V$	-100			μΛ

DC ELECTRICAL CHARACTERISTICS (continued)

 $(V_{CC} = +5.0V \pm 10\%, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = +5.0V \text{ and } T_A = +25^{\circ}\text{C.}$) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
		0 ≤ V _{OUT} ≤ +12V (Note 3)		40		250	
		$-7V \le V_{OUT} \le V_{CC}$ (Note 3)	-250		-40		
Driver Short-Circuit Output Current	I _{OSD}	$0 \le V_{OUT} \le +12V$, $+85^{\circ}C \le T_{A}$ (Note 3)	≤+125°C	40		270	mA
		$-7V \le V_{OUT} \le V_{CC}$, $+85^{\circ}C \le T_{A}$ (Note 3)	\ ≤ +125°C	-270		-40	
Driver Short-Circuit Foldback	loope	$(V_{CC} - 1V) \le V_{OUT} \le +12V$ (No	te 3)	20			mA
Output Current	losdf	$-7V \le V_{OUT} \le +1V \text{ (Note 3)}$				-20	IIIA
Thermal-Shutdown Threshold	T _{TS}				175		°C
Thermal-Shutdown Hysteresis	T _{TSH}				15		°C
Input Current (A and B)	IA D	DE = GND,	$V_{IN} = +12V$			125	μΑ
Input Current (A and B)	I _{A, B}	V _{CC} = GND or V _{CC}	$V_{IN} = -7V$	-100			μΑ
RECEIVER	•						
Receiver Differential Threshold Voltage	V _T H	$-7V \le V_{CM} \le +12V$		-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	$V_A + V_B = 0$			15		mV
RO Output-High Voltage	V _{OH}	I _O = -1mA		V _{CC} - 0.6	3		V
RO Output-Low Voltage	V _{OL}	$I_O = 1mA$				0.4	V
Three-State Output Current at Receiver	lozr	0 ≤ V _O ≤ V _{CC}				± 1	μΑ
Receiver Input Resistance	R _{IN}	$-7V \le V_{CM} \le +12V$		96			kΩ
Receiver Output Short-Circuit Current	IOSR	0V ≤ V _{RO} ≤ V _{CC}				±110	mA
SUPPLY CURRENT							
		No load, $\overline{RE} = 0$, DE = V_{CC}			1.2	1.8	
Supply Current	Icc	No load, $\overline{RE} = V_{CC}$, $DE = V_{CC}$			1.2	1.8	mA
		No load, $\overline{RE} = 0$, DE = 0			1.2	1.8	
Supply Current in Shutdown Mode	ISHDN	$\overline{RE} = V_{CC}$, DE = GND			2.8	10	μΑ
ESD PROTECTION	-						
		Human Body Model	<u> </u>		±15		kV
ESD Protection for Y, Z, A, and B		Contact Discharge IEC 61000-4-2			±6		kV

DRIVER SWITCHING CHARACTERISTICS MAX13080E/MAX13081E/MAX13082E/MAX13089E WITH SRL = UNCONNECTED (250kbps)

 $(V_{CC} = +5.0V \pm 10\%, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = +5.0V \text{ and } T_A = +25^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Brancosties Delev	tDPLH	0 50 5 0 540 5			1800	
Driver Propagation Delay	tdphl	C_L = 50pF, R_L = 54 Ω , Figures 2 and 3	350		1800	ns
Driver Differential Output Rise or Fall Time	t _R , t _F	C_L = 50pF, R_L = 54 Ω , Figures 2 and 3	400		1900	ns
Differential Driver Output Skew Itdplh - tdphll	tdskew	C_L = 50pF, R_L = 54 Ω , Figures 2 and 3			250	ns
Maximum Data Rate			250			kbps
Driver Enable to Output High	tDZH	Figure 4			2500	ns
Driver Enable to Output Low	t _{DZL}	Figure 5			2500	ns
Driver Disable Time from Low	t _{DLZ}	Figure 5			100	ns
Driver Disable Time from High	tDHZ	Figure 4			100	ns
Driver Enable from Shutdown to Output High	tDZH(SHDN)	Figure 4			5500	ns
Driver Enable from Shutdown to Output Low	t _{DZL} (SHDN)	Figure 5			5500	ns
Time to Shutdown	tshdn		50	340	700	ns

RECEIVER SWITCHING CHARACTERISTICS MAX13080E/MAX13081E/MAX13082E/MAX13089E WITH SRL = UNCONNECTED (250kbps)

 $(V_{CC} = +5.0V \pm 10\%, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = +5.0V \text{ and } T_A = +25^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Propagation Delay	trplh	C _L = 15pF, Figures 6 and 7			200	ns
neceiver Fropagation Delay	trphl	CL = 15pr, Figures 6 and 7			200	115
Receiver Output Skew ItRPLH - tRPHLI	trskew	C _L = 15pF, Figures 6 and 7			30	ns
Maximum Data Rate			250			kbps
Receiver Enable to Output Low	trzl	Figure 8			50	ns
Receiver Enable to Output High	trzh	Figure 8			50	ns
Receiver Disable Time from Low	t _{RLZ}	Figure 8			50	ns
Receiver Disable Time from High	tRHZ	Figure 8			50	ns
Receiver Enable from Shutdown to Output High	tRZH(SHDN)	Figure 8			5500	ns
Receiver Enable from Shutdown to Output Low	tRZL(SHDN)	Figure 8			5500	ns
Time to Shutdown	tshdn		50	340	700	ns

· _____ /I/X/N

DRIVER SWITCHING CHARACTERISTICS MAX13083E/MAX13084E/MAX13085E/MAX13089E WITH SRL = V_{CC} (500kbps)

 $(V_{CC} = +5.0V \pm 10\%, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = +5.0V \text{ and } T_A = +25^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	tDPLH	$ C_L = 50$ pF, $R_L = 54\Omega$, Figures 2 and 3			1000	20
Driver Propagation Delay	tDPHL				1000	ns
Driver Differential Output Rise or Fall Time	t _R , t _F	C_L = 50pF, R_L = 54 Ω , Figures 2 and 3	250		900	ns
Differential Driver Output Skew Itdplh - tdphll	tDSKEW	C_L = 50pF, R_L = 54 Ω , Figures 2 and 3			140	ns
Maximum Data Rate			500			kbps
Driver Enable to Output High	tdzh	Figure 4			2500	ns
Driver Enable to Output Low	tDZL	Figure 5			2500	ns
Driver Disable Time from Low	t _{DLZ}	Figure 5			100	ns
Driver Disable Time from High	tDHZ	Figure 4			100	ns
Driver Enable from Shutdown to Output High	tDZH(SHDN)	Figure 4			5500	ns
Driver Enable from Shutdown to Output Low	tDZL(SHDN)	Figure 5			5500	ns
Time to Shutdown	tshdn		50	340	700	ns

RECEIVER SWITCHING CHARACTERISTICS MAX13083E/MAX13084E/MAX13085E/MAX13089E WITH SRL = V_{CC} (500kbps)

 $(V_{CC} = +5.0V \pm 10\%, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = +5.0V \text{ and } T_A = +25^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Propagation Delay	trplh	C _L = 15pF, Figures 6 and 7			200	no
neceiver Fropagation Delay	trphl	CL = 15pr, Figures 6 and 7			200	ns
Receiver Output Skew ltrplh - trphl	trskew	C _L = 15pF, Figures 6 and 7			30	ns
Maximum Data Rate			500			kbps
Receiver Enable to Output Low	trzl	Figure 8			50	ns
Receiver Enable to Output High	trzh	Figure 8			50	ns
Receiver Disable Time from Low	t _{RLZ}	Figure 8			50	ns
Receiver Disable Time from High	trhz	Figure 8			50	ns
Receiver Enable from Shutdown to Output High	[†] RZH(SHDN)	Figure 8			5500	ns
Receiver Enable from Shutdown to Output Low	tRZL(SHDN)	Figure 8			5500	ns
Time to Shutdown	tshdn		50	340	700	ns

DRIVER SWITCHING CHARACTERISTICS MAX13086E/MAX13087E/MAX13088E/MAX13089E WITH SRL = GND (16Mbps)

 $(V_{CC} = +5.0V \pm 10\%, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted. Typical values are at } V_{CC} = +5.0V \text{ and } T_A = +25^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	tDPLH	$C_L = 50$ pF, $R_L = 54\Omega$, Figures 2 and 3			50	no
Driver Propagation Delay	tDPHL				50	ns
Driver Differential Output Rise or Fall Time	t _R , t _F	C_L = 50pF, R_L = 54 Ω , Figures 2 and 3			15	ns
Differential Driver Output Skew Itdplh - tdphll	tdskew	C_L = 50pF, R_L = 54 Ω , Figures 2 and 3			8	ns
Maximum Data Rate			16			Mbps
Driver Enable to Output High	tdzh	Figure 4			150	ns
Driver Enable to Output Low	t _{DZL}	Figure 5			150	ns
Driver Disable Time from Low	t _{DLZ}	Figure 5			100	ns
Driver Disable Time from High	tDHZ	Figure 4			100	ns
Driver Enable from Shutdown to Output High	tDZH(SHDN)	Figure 4			2200	ns
Driver Enable from Shutdown to Output Low	t _{DZL} (SHDN)	Figure 5			2200	ns
Time to Shutdown	tshdn		50	340	700	ns

RECEIVER SWITCHING CHARACTERISTICS MAX13086E/MAX13087E/MAX13088E/MAX13089E WITH SRL = GND (16Mbps)

 $(V_{CC} = +5.0V \pm 10\%, T_A = T_{MIN} \text{ to } T_{MAX}, \text{ unless otherwise noted.}$ Typical values are at $V_{CC} = +5.0V \text{ and } T_A = +25^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Desciver Proposition Delay	trplh	Cr = 15pE Figures 6 and 7		50	80	20
Receiver Propagation Delay	trphl	C _L = 15pF, Figures 6 and 7		50	80	ns
Receiver Output Skew trplh - trphl	trskew	C _L = 15pF, Figures 6 and 7			13	ns
Maximum Data Rate			16			Mbps
Receiver Enable to Output Low	trzl	Figure 8			50	ns
Receiver Enable to Output High	trzh	Figure 8			50	ns
Receiver Disable Time from Low	tRLZ	Figure 8			50	ns
Receiver Disable Time from High	trhz	Figure 8			50	ns
Receiver Enable from Shutdown to Output High	[†] RZH(SHDN)	Figure 8			2200	ns
Receiver Enable from Shutdown to Output Low	[†] RZL(SHDN)	Figure 8			2200	ns
Time to Shutdown	tshdn		50	340	700	ns

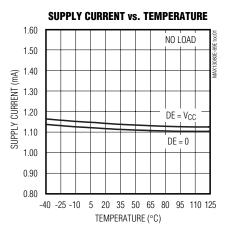
Note 1: All currents into the device are positive. All currents out of the device are negative. All voltages are referred to device ground, unless otherwise noted.

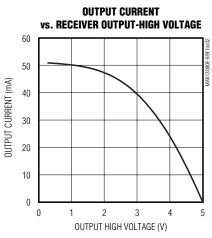
Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when the DI input changes state.

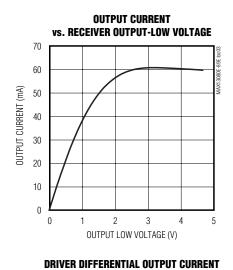
Note 3: The short-circuit output current applies to peak current just prior to foldback current limiting. The short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

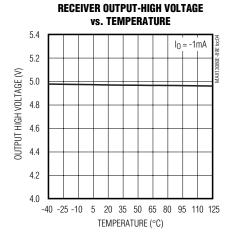
Typical Operating Characteristics

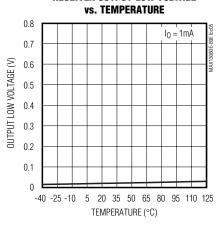
 $(V_{CC} = +5.0V, T_A = +25^{\circ}C, unless otherwise noted.)$



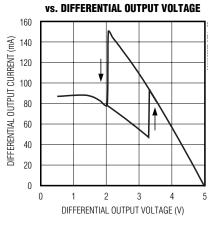


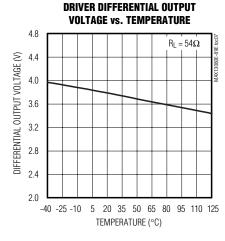


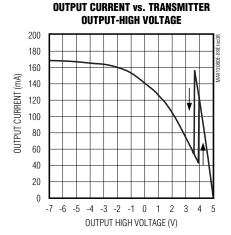


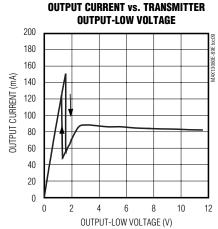


RECEIVER OUTPUT-LOW VOLTAGE



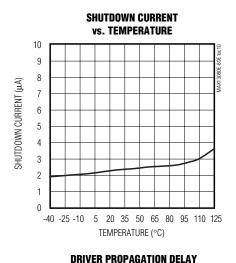


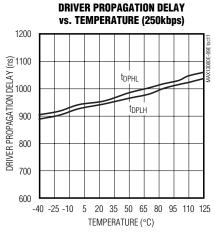


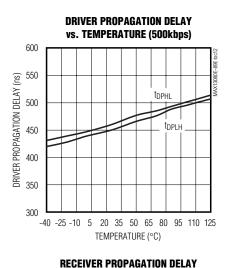


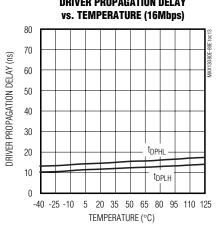
_Typical Operating Characteristics (continued)

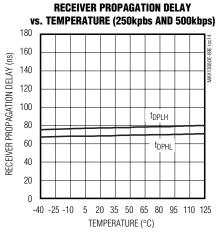
($V_{CC} = +5.0V$, $T_A = +25$ °C, unless otherwise noted.)

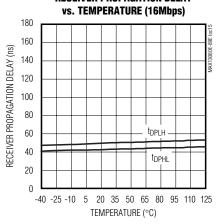


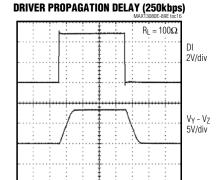




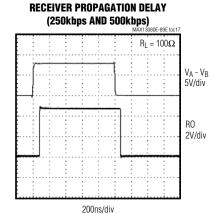






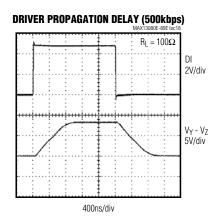


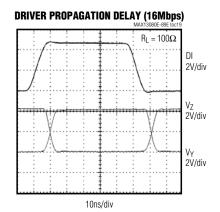
2µs/div

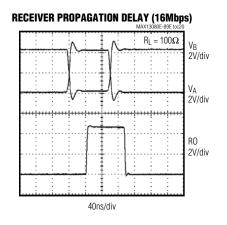


Typical Operating Characteristics (continued)

 $(V_{CC} = +5.0V, T_A = +25^{\circ}C, unless otherwise noted.)$







Test Circuits and Waveforms

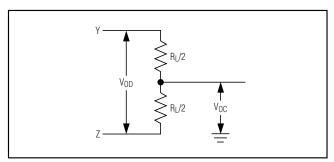


Figure 1. Driver DC Test Load

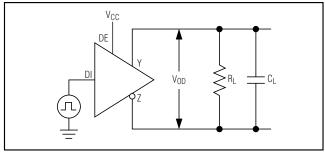


Figure 2. Driver Timing Test Circuit

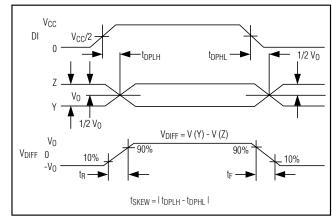


Figure 3. Driver Propagation Delays

Test Circuits and Waveforms (continued)

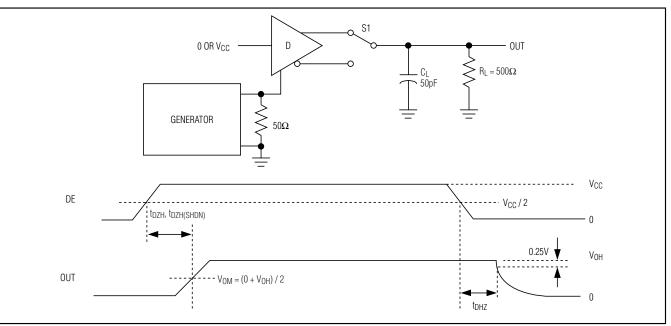


Figure 4. Driver Enable and Disable Times (tDHZ, tDZH, tDZH(SHDN))

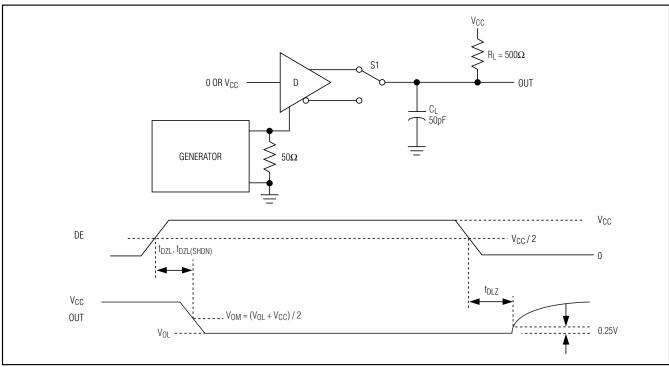


Figure 5. Driver Enable and Disable Times (tDZL, tDLZ, tDLZ(SHDN))

10 ______/N/XI/VI

Test Circuits and Waveforms (continued)

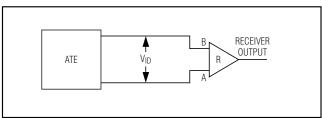


Figure 6. Receiver Propagation Delay Test Circuit

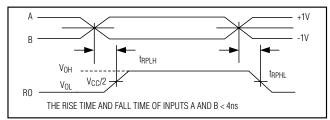


Figure 7. Receiver Propagation Delays

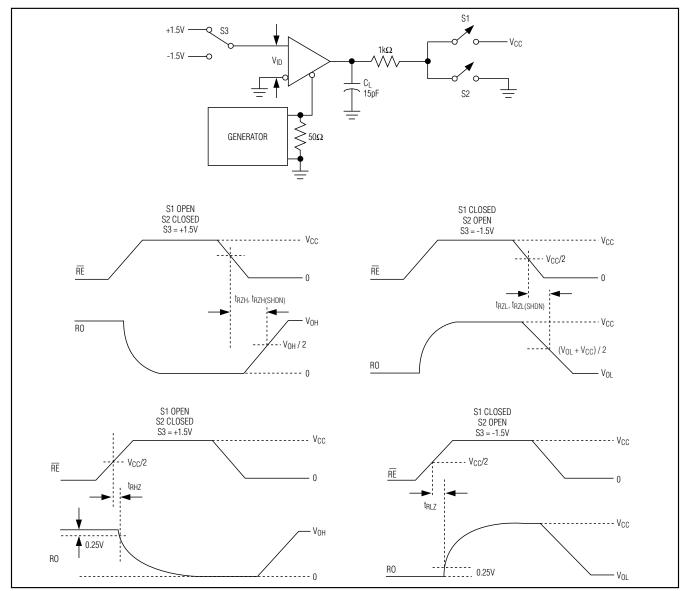


Figure 8. Receiver Enable and Disable Times

Pin Description

	PIN					
MAX13083E	X13080E MAX13081E MAX13082E X13083E MAX13084E MAX13085E MAX13088 X13086E MAX13087E MAX13088E		3089E	NAME	FUNCTION	
FULL-D DEV	OUPLEX	HALF- DUPLEX DEVICES	FULL- DUPLEX MODE	PLEX DUPLEX		
1, 8, 13	_	_	_	_	N.C.	No Connect. Not internally connected, can be connected to GND.
_	_	_	1	1	H/F	Half-/Full-Duplex Select Input. Connect H/F to V _{CC} for half-duplex mode; connect H/F to GND or leave unconnected for full-duplex mode.
2	2	1	2	2	RO	Receiver Output. When \overline{RE} is low and if $(A - B) \ge -50 \text{mV}$, RO is high; if $(A - B) \le -200 \text{mV}$, RO is low.
3		2	3	3	RE	Receiver Output Enable. Drive \overline{RE} low to enable RO; RO is high impedance when \overline{RE} is high. Drive \overline{RE} high and DE low to enter low-power shutdown mode. \overline{RE} is a hot-swap input (see the <i>Hot-Swap Capability</i> section for details).
4	_	3	4	4	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive RE high and DE low to enter low-power shutdown mode. DE is a hot-swap input (see the Hot-Swap Capability section for details).
5	3	4	5	5	DI	Driver Input. With DE high, a low on DI forces noninverting output low and inverting output high. Similarly, a high on DI forces noninverting output high and inverting output low.
_	_	_	6	6	SRL	Slew-Rate Limit Selector Input. Connect SRL to ground for 16Mbps communication rate; connect SRL to V _{CC} for 500kbps communication rate. Leave SRL unconnected for 250kbps communication rate.
6, 7	4	5	7	7	GND	Ground
_	_	_	8	8	TXP	Transmitter Phase. Connect TXP to ground or leave TXP floating for normal transmitter phase/polarity. Connect TXP to V _{CC} to invert the transmitter phase/polarity.
9	5		9		Υ	Noninverting Driver Output
_	_	_		9	Υ	Noninverting Driver Output and Noninverting Receiver Input*
10	6	_	10	_	Z	Inverting Driver Output
_	_	_	_	10	Z	Inverting Driver Output and Inverting Receiver Input*
11	7	_	11	_	В	Inverting Receiver Input
_	_	_	_	11	В	Receiver Input Resistors*
_	_	7	_	_	В	Inverting Receiver Input and Inverting Driver Output

Pin Description (continued)

		PIN				
MAX13083E	MAX13081E MAX13084E MAX13087E		MAX13089E		NAME	FUNCTION
_	JLL-DUPLEX DEVICES HALF-DUPLEX DEVICES		FULL- DUPLEX MODE	OUPLEX DUPLEX		
12	8	_	12	12 —		Noninverting Receiver Input
_	_	_	_	12	Α	Receiver Input Resistors*
_	_	6	_	_	А	Noninverting Receiver Input and Noninverting Driver Output
_	_	_	13	13	RXP	Receiver Phase. Connect RXP to GND or leave RXP unconnected for normal transmitter phase/polarity. Connect RXP to VCC to invert receiver phase/polarity.
14	1	8	14	14	V _{CC}	Positive Supply V_{CC} = +5.0V ±10%. Bypass V_{CC} to GND with a 0.1µF capacitor.

^{*}MAX13089E only. In half-duplex mode, the driver outputs serve as receiver inputs. The full-duplex receiver inputs (A and B) still have a 1/8-unit load (96 $k\Omega$), but are not connected to the receiver.

_Function Tables

13

MAX13080E/MAX13083E/MAX13086E

TRANSMITTING						
	INPUTS	OUTPUTS				
RE	DE	DI	Z	Υ		
Х	1	1	0	1		
Х	1	0	1	0		
0	0	Х	High-Z	High-Z		
1	0	Х	Shuto	down		
		RECEIVING				
	INPUTS		OUT	PUT		
RE	DE	A, B	RO			
0	Χ	≥ -50mV	1			
0	Χ	≤ -200mV	0			
0	Х	Open/ shorted	1			
1	1	Χ	High-Z			
1	0	Х	Shuto	down		

MAX13081E/MAX13084E/MAX13086E/ MAX13087E

TRANSMITTING				
INPUT	OUTPUTS			
DI	Z	Υ		
1	0	1		
0	1	0		
RECEIVING				
INPUTS	OUT	PUT		
A, B	R	0		
≥ -50mV	≥ -50mV 1			
≤ -200mV	≤ -200mV 0			
Open/shorted		1		

Function Tables (continued)

MAX13082E/MAX13085E/MAX13088E

TRANSMITTING						
INPUTS OUTPUTS						
RE	DE	DI	B/Z	A/Y		
Х	1	1	0	1		
Х	1	0	1	0		
0	0	Х	High-Z	High-Z		
1	0	Х	Shutdown			

RECEIVING						
	INPUTS OUTPUTS					
RE	DE	A-B	RO			
0	Χ	≥ -50mV	1			
0	Χ	≤ -200mV	0			
0	X	Open/ shorted	1			
1	1	Х	High-Z			
1	0	Χ	Shutdown			

MAX13089E

TRANSMITTING							
	INPUTS OUTPUTS						
TXP	RE	DE	DI	Z	Υ		
0	X	1	1	0	1		
0	X	1	0	1	0		
1	X	1	1	1	0		
1	Х	1	0	0	1		
Х	0	0	Х	High-Z	High-Z		
Х	1 0 X Shutdown						

			RECEIVIN	 G		
		INP	UTS			OUTPUTS
H/F	RXP	RE	DE	A, B	Y, Z	RO
0	0	0	Х	> -50mV	X	1
0	0	0	Х	< -200mV	X	0
0	1	0	X	> -50mV	Х	0
0	1	0	Х	< -200mV	X	1
1	0	0	0	X	> -50mV	1
1	0	0	0	X	< -200mV	0
1	1	0	0	X	> -50mV	0
1	1	0	0	X	< -200mV	1
0	0	0	X	Open/shorted	X	1
1	0	0	0	X	Open/shorted	1
0	1	0	Х	Open/shorted	X	0
1	1	0	0	X	Open/shorted	0
X	X	1	1	X	X	High-Z
Χ	Х	1	0	Х	X	Shutdown

X = Don't care; shutdown mode, driver, and receiver outputs are high impedance.

14 _______/N/1XI/VI

Detailed Description

The MAX13080E-MAX13089E high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the Fail-Safe section). The MAX13080E/MAX13082E/MAX13083E/MAX13085E/ MAX13086E/MAX13088E/MAX13089E also feature a hotswap capability allowing line insertion without erroneous data transfer (see the Hot Swap Capability section). The MAX13080E/MAX13081E/MAX13082E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 250kbps. The MAX13083E/MAX13084E/MAX13085E also offer slewrate limits allowing transmit speeds up to 500kbps. The MAX13086E/MAX13087E/MAX13088Es' driver slew rates are not limited, making transmit speeds up to 16Mbps possible. The MAX13089E's slew rate is selectable between 250kbps, 500kbps, and 16Mbps by driving a selector pin with a three-state driver.

The MAX13082E/MAX13085E/MAX13088E are half-duplex transceivers, while the MAX13080E/MAX13081E/MAX13083E/MAX13084E/MAX13086E/MAX13087E are full-duplex transceivers. The MAX13089E is selectable between half- and full-duplex communication by driving a selector pin (H/\overline{F}) high or low, respectively.

All devices operate from a single +5.0V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

Receiver Input Filtering

The receivers of the MAX13080E-MAX13085E, and the MAX13089E when operating in 250kbps or 500kbps mode, incorporate input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases by 25% due to this filtering.

Fail-Safe

The MAX13080E family guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic-high. If (A - B) is less

than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the MAX13080E family, this results in a logic-high with a 50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

Hot-Swap Capability (Except MAX13081E/MAX13084E/MAX13087E)

Hot-Swap Inputs

When circuit boards are inserted into a hot or powered backplane, differential disturbances to the data bus can lead to data errors. Upon initial circuit board insertion, the data communication processor undergoes its own power-up sequence. During this period, the processor's logic-output drivers are high impedance and are unable to drive the DE and $\overline{\text{RE}}$ inputs of these devices to a defined logic level. Leakage currents up to $\pm 10 \mu A$ from the high-impedance state of the processor's logic drivers could cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to the enable inputs. Without the hot-swap capability, these factors could improperly enable the transceiver's driver or receiver.

When V_{CC} rises, an internal pulldown circuit holds DE low and \overline{RE} high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

Hot-Swap Input Circuitry

The enable inputs feature hot-swap capability. At the input there are two NMOS devices. M1 and M2 (Figure 9). When V_{CC} ramps from zero, an internal 7µs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 1.5mA current sink, and M1, a 500µA current sink, pull DE to GND through a $5k\Omega$ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 7µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever VCC drops below 1V, the hot-swap input is reset.

For \overline{RE} there is a complementary circuit employing two PMOS devices pulling \overline{RE} to VCC.

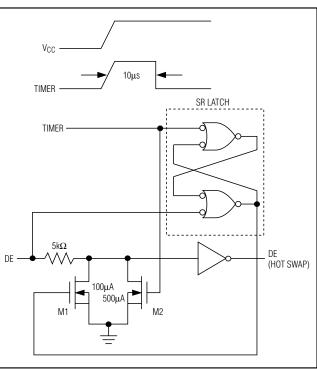


Figure 9. Simplified Structure of the Driver Enable Pin (DE)

MAX13089E Programming

The MAX13089E has several programmable operating modes. Transmitter rise and fall times are programmable, resulting in maximum data rates of 250kbps, 500kbps, and 16Mbps. To select the desired data rate, drive SRL to one of three possible states by using a three-state driver: $V_{\rm CC}$, GND, or unconnected. For 250kbps operation, set the three-state device in high-impedance mode or leave SRL unconnected. For 500kbps operation, drive SRL high or connect it to V_{CC}. For 16Mbps operation, drive SRL low or connect it to GND. SRL can be changed during operation without interrupting data communications.

Occasionally, twisted-pair lines are connected backward from normal orientation. The MAX13089E has two pins that invert the phase of the driver and the receiver to correct this problem. For normal operation, drive TXP and RXP low, connect them to ground, or leave them unconnected (internal pulldown). To invert the driver phase, drive TXP high or connect it to V $_{\rm CC}$. To invert the receiver phase, drive RXP high or connect it to V $_{\rm CC}$. Note that the receiver threshold is positive when RXP is high.

The MAX13089E can operate in full- or half-duplex mode. Drive H/F low, leave it unconnected (internal pulldown), or connect it to GND for full-duplex opera-

tion. Drive H/F high for half-duplex operation. In full-duplex mode, the pin configuration of the driver and receiver is the same as that of a MAX13080E. In half-duplex mode, the receiver inputs are internally connected to the driver outputs through a resistor-divider. This effectively changes the function of the device's outputs. Y becomes the noninverting driver output and receiver input, Z becomes the inverting driver output and receiver input. In half-duplex mode, A and B are still connected to ground through an internal resistor-divider but they are not internally connected to the receiver.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX13080E family of devices have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX13080E–MAX13089E keep working without latchup or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX13080E–MAX13089E are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±6kV using the Contact Discharge method specified in IEC 61000-4-2

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 10a shows the Human Body Model, and Figure 10b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a $1.5 \mathrm{k}\Omega$ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX13080E family of devices helps you design equipment to meet IEC 61000-4-2, without the need for additional ESD-protection components.

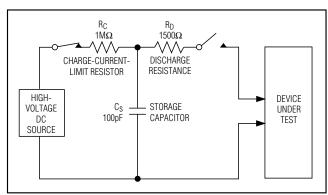


Figure 10a. Human Body ESD Test Model

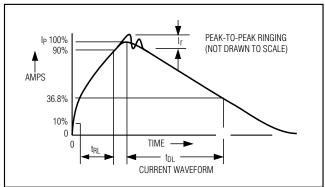


Figure 10b. Human Body Current Waveform

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 10c shows the IEC 61000-4-2 model, and Figure 10d shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

Machine Model

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly. Of course, all pins require this protection, not just RS-485 inputs and outputs.

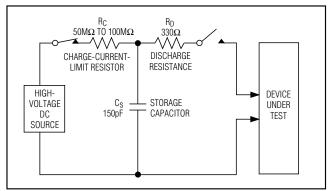


Figure 10c. IEC 61000-4-2 ESD Test Model

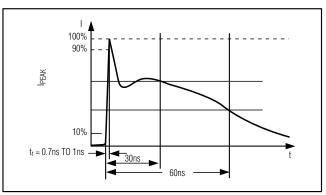


Figure 10d. IEC 61000-4-2 ESD Generator Current Waveform

_Applications Information

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is $12k\Omega$ (1-unit load), and the standard driver can drive up to 32-unit loads. The MAX13080E family of transceivers has a 1/8-unit load receiver input impedance ($96k\Omega$), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices, as well as other RS-485 transceivers with a total of 32-unit loads or fewer, can be connected to the line.

Reduced EMI and Reflections

The MAX13080E/MAX13081E/MAX13082E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 250kbps. The MAX13083E/MAX13084E/MAX13085E offer higher driver output slew-rate limits, allowing transmit speeds up to 500kbps. The MAX13089E with SRL = VCC or unconnected are slew-rate limited. With SRL unconnected, the MAX13089E error-free data transmission is up to 250kbps. With SRL connected to VCC, the data transmit speeds up to 500kbps.

Low-Power Shutdown Mode (Except MAX13081E/MAX13084E/MAX13087E)

Low-power shutdown mode is initiated by bringing both RE high and DE low. In shutdown, the devices typically draw only 2.8µA of supply current.

RE and DE can be driven simultaneously; the devices are guaranteed not to enter shutdown if RE is high and DE is low for less than 50ns. If the inputs are in this state for at least 700ns, the devices are guaranteed to enter shutdown.

Enable times tzH and tzL (see the *Switching Characteristics* section) assume the devices were not in a low-power shutdown state. Enable times tzH(SHDN) and tzL(SHDN) assume the devices were in shutdown state. It takes drivers and receivers longer to become enabled from low-power shutdown mode (tzH(SHDN), tzL(SHDN)) than from driver/receiver-disable mode (tzH, tzL).

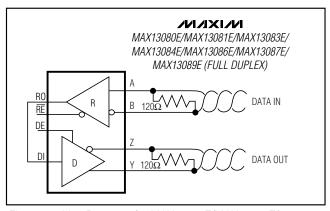


Figure 11. Line Repeater for MAX13080E/MAX13081E/ MAX13083E/MAX13084E/MAX13086E/MAX13087E/MAX13089E in Full-Duplex Mode

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics*). The second, a thermal-shut-down circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +175°C (typ).

Line Length

The RS-485/RS-422 standard covers line lengths up to 4000ft. For line lengths greater than 4000ft, use the repeater application shown in Figure 11.

Typical Applications

The MAX13082E/MAX13085E/MAX13088E/MAX13089E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 12 and 13 show typical network applications circuits.

To minimize reflections, terminate the line at both ends in its characteristic impedance, and keep stub lengths off the main line as short as possible. The slew-rate-limited MAX13082E/MAX13085E and the two modes of the MAX13089E are more tolerant of imperfect termination.

Chip Information

TRANSISTOR COUNT: 1228

PROCESS: BiCMOS

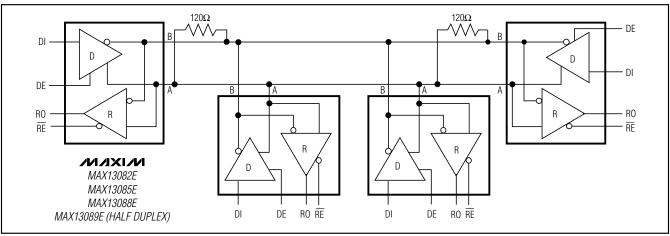


Figure 12. Typical Half-Duplex RS-485 Network

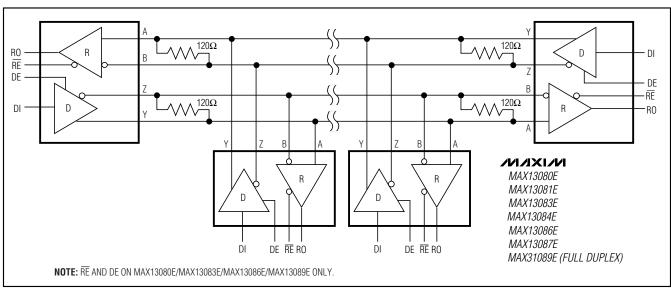
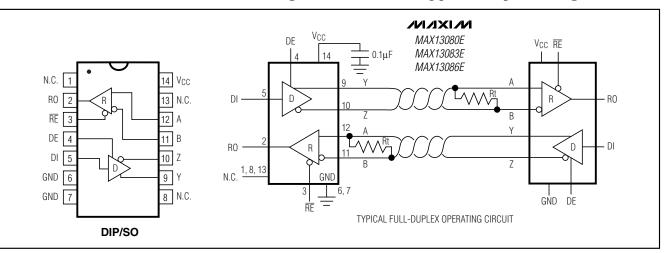


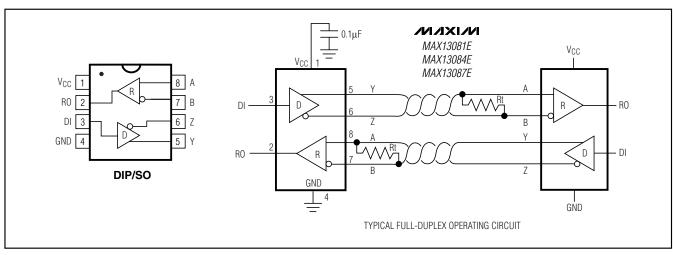
Figure 13. Typical Full-Duplex RS-485 Network

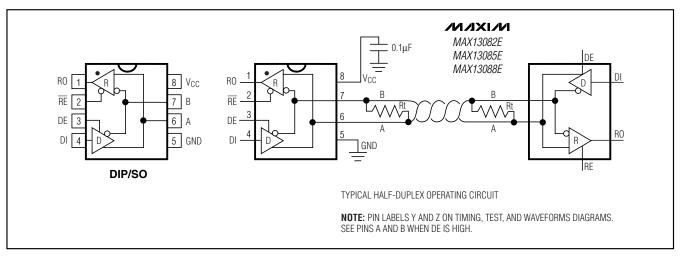
Selector Guide

PART	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	TRANSCEIVERS ON BUS	PINS
MAX13080E	Full	0.250	Yes	Yes	Yes	256	14
MAX13081E	Full	0.250	Yes	No	No	256	8
MAX13082E	Half	0.250	Yes	Yes	Yes	256	8
MAX13083E	Full	0.5	Yes	Yes	Yes	256	14
MAX13084E	Full	0.5	Yes	No	No	256	8
MAX13085E	Half	0.5	Yes	Yes	Yes	256	8
MAX13086E	Full	16	No	Yes	Yes	256	14
MAX13087E	Full	16	No	No	No	256	8
MAX13088E	Half	16	No	Yes	Yes	256	8
MAX13089E	Selectable	Selectable	Selectable	Yes	Yes	256	14

Pin Configurations and Typical Operating Circuits

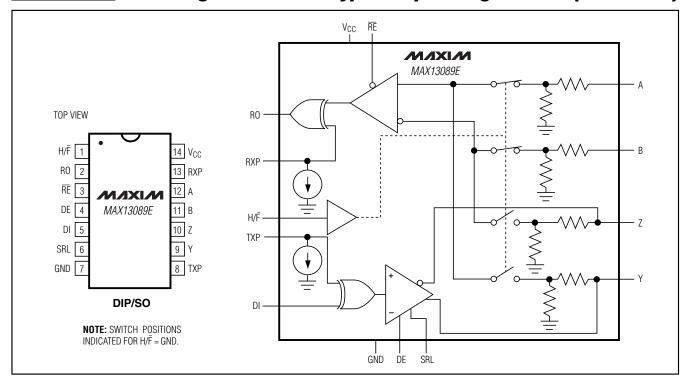






20 _______/VIXI/M

Pin Configurations and Typical Operating Circuits (continued)



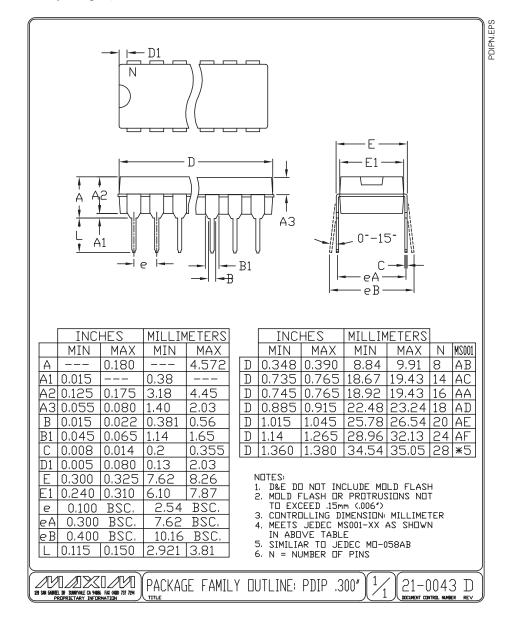
Ordering Information (continued)

PART	TEMP RANGE	PIN- PACKAGE	PKG CODE
MAX13081ECPA	0°C to +70°C	8 PDIP	P8-2
MAX13081ECSA	0°C to +70°C	8 SO	S8-4
MAX13081EEPA	-40°C to +85°C	8 PDIP	P8-2
MAX13081EESA	-40°C to +85°C	8 SO	S8-4
MAX13081EAPA	-40°C to +125°C	8 PDIP	P8-2
MAX13081EASA	-40°C to +125°C	8 SO	S8-4
MAX13082ECPA	0°C to +70°C	8 PDIP	P8-2
MAX13082ECSA	0°C to +70°C	8 SO	S8-4
MAX13082EEPA	-40°C to +85°C	8 PDIP	P8-2
MAX13082EESA	-40°C to +85°C	8 SO	S8-4
MAX13082EAPA	-40°C to +125°C	8 PDIP	P8-2
MAX13082EASA	-40°C to +125°C	8 SO	S8-4
MAX13083ECPD	0°C to +70°C	14 PDIP	P14-3
MAX13083ECSD	0°C to +70°C	14 SO	S14-2
MAX13083EEPD	-40°C to +85°C	14 PDIP	P14-3
MAX13083EESD	-40°C to +85°C	14 SO	S14-2
MAX13083EAPD	-40°C to +125°C	14 PDIP	P14-3
MAX13083EASD	-40°C to +125°C	14 SO	S14-2
MAX13084ECPA	0°C to +70°C	8 PDIP	P8-2
MAX13084ECSA	0°C to +70°C	8 SO	S8-4
MAX13084EEPA	-40°C to +85°C	8 PDIP	P8-2
MAX13084EESA	-40°C to +85°C	8 SO	S8-4
MAX13084EAPA	-40°C to +125°C	8 PDIP	P8-2
MAX13084EASA	-40°C to +125°C	8 SO	S8-4
MAX13085ECPA	0°C to +70°C	8 PDIP	P8-2
MAX13085ECSA	0°C to +70°C	8 SO	S8-4
MAX13085EEPA	-40°C to +85°C	8 PDIP	P8-2
MAX13085EESA	-40°C to +85°C	8 SO	S8-4
MAX13085EAPA	-40°C to +125°C	8 PDIP	P8-2
MAX13085EASA	-40°C to +125°C	8 SO	S8-4

PART	TEMP RANGE	PIN- PACKAGE	PKG CODE
MAX13086ECPD	0°C to +70°C	14 PDIP	P14-3
MAX13086ECSD	0°C to +70°C	14 SO	S14-2
MAX13086EEPD	-40°C to +85°C	14 PDIP	P14-3
MAX13086EESD	-40°C to +85°C	14 SO	S14-2
MAX13086EAPD	-40°C to +125°C	14 PDIP	P14-3
MAX13086EASD	-40°C to +125°C	14 SO	S14-2
MAX13087ECPA	0°C to +70°C	8 PDIP	P8-2
MAX13087ECSA	0°C to +70°C	8 SO	S8-4
MAX13087EEPA	-40°C to +85°C	8 PDIP	P8-2
MAX13087EESA	-40°C to +85°C	8 SO	S8-4
MAX13087EAPA	-40°C to +125°C	8 PDIP	P8-2
MAX13087EASA	-40°C to +125°C	8 SO	S8-4
MAX13088ECPA	0°C to +70°C	8 PDIP	P8-2
MAX13088ECSA	0°C to +70°C	8 SO	S8-4
MAX13088EEPA	-40°C to +85°C	8 PDIP	P8-2
MAX13088EESA	-40°C to +85°C	8 SO	S8-4
MAX13088EAPA	-40°C to +125°C	8 PDIP	P8-2
MAX13088EASA	-40°C to +125°C	8 SO	S8-4
MAX13089ECPD	0°C to +70°C	14 PDIP	P14-3
MAX13089ECSD	0°C to +70°C	14 SO	S14-2
MAX13089EEPD	-40°C to +85°C	14 PDIP	P14-3
MAX13089EESD	-40°C to +85°C	14 SO	S14-2
MAX13089EAPD	-40°C to +125°C	14 PDIP	P14-3
MAX13089EASD	-40°C to +125°C	14 SO	S14-2

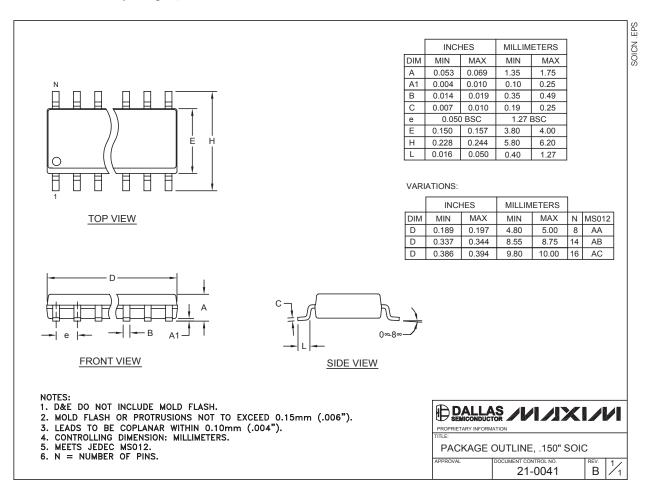
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600