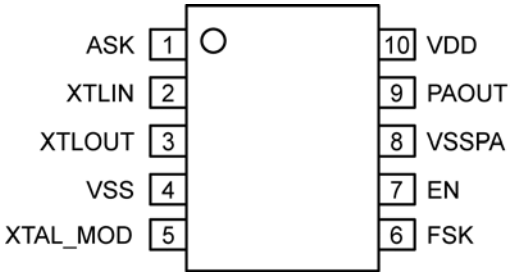
Pin Configuration



10-Pin MSOP (YMM)

Pin Description

Pin Number	Pin Name	Pin Function
1	ASK	ASK Data Input and PA Enable. When EN is set to a logic-level HIGH and ASK is set to a logic-level HIGH, the power amplifier (PA) is enabled. A logic-level LOW on ASK disables the power amplifier. Apply a data stream less than 50Kbps (Manchester Encoded, 50% duty-cycle) for ASK modulation. To transmit with FSK modulation, both EN and ASK need to be set to a logic-level HIGH, while the FSK pin is modulated.
2	XTLIN	Reference Oscillator Input Connection. Connect a crystal between XTLIN and XTLOUT. Connect a load capacitor from XTLIN to ground, based on the recommendations of the crystal manufacturer.
3	XTLOUT	Reference Oscillator Output Connection. Connect a crystal between XTLIN and XTLOUT. Connect a load capacitor from XTLOUT to ground, based on the recommendations of the crystal manufacturer.
4	VSS	Ground.
5	XTAL_MOD	FSK Crystal Pulling Switch Connection. For FSK modulation, connect a capacitor between the XTAL_MOD pin and XTLOUT. For ASK-only operation, this pin can be left unconnected.
6	FSK	FSK Data Input. A logic-level LOW opens the FSK crystal pulling switch, providing high impedance (>1MΩ) between the XTAL_MOD pin and VSS (ground). A logic-level HIGH closes the switch, providing low impedance (15Ω) between XTAL_MOD and VSS (ground). This parallels the crystal pulling capacitor, C_{FSK}, with the crystal load capacitor, C_{LOAD}, and pulls the reference frequency to achieve FSK modulation. For ASK-only operation, pulling this pin low is recommended.
7	EN	Enable/Shutdown Input. A logic-level LOW disables the entire device, placing it in a low-power shutdown mode. A logic-level HIGH enables the crystal oscillator, PLL, voltage-controlled oscillator (VCO), and control blocks, if the supply voltage is above the undervoltage lockout (UVLO) voltage. The power amplifier is enabled when a logic-level HIGH is applied to EN and ASK.
8	VSSPA	Power Amplifier Ground.
9	PAOUT	Open Collector of Power Amplifier Output. Pull the PA_OUT pin to VDD through an inductor to properly bias the output stage. Add a pull-up resistor in series to reduce bias current and to achieve lower output power and lower supply current operation. A matching network is required to match the output to desired load (PCB antenna, wire antenna, or 50Ω load) to achieve best output power, supply current, and spectral performance. See the “Applications Information” section for recommended power supply bypassing.
10	VDD	Power Supply for Crystal Oscillator, Phase-Locked Loop, Voltage-Controlled Oscillator, and Control Blocks. See the “Applications Information” section for recommended power supply bypassing.

Absolute Maximum Ratings[1]

Supply Voltage (V_{VDD}) .....+4.3V
Voltage on PAOUT (V_{PAOUT}).....+7.2V
Logic Inputs (V_{ASK}, V_{FSK}, V_{EN})..... V_{VSS} – 0.3 to V_{VDD} + 0.3V
Storage Temperature Range .....–65°C to + 150°C
Lead Temperature (soldering, 10s).....+260°C
ESD Rating.....Note 3

Operating Ratings[2]

Supply Voltage (V_{VDD}, V_{PAOUT})……+1.8V to +3.6V
Input Voltage (V_{ASK}, V_{FSK}, V_{EN}).....0V to V_{VDD}
Junction Temperature (T_J) .....–40°C to +125°C
Transmitter Frequency Range (f_{RF})..... 300MHz to 450MHz
Thermal Resistance, (θ_{JA})……130°C/W

Electrical Characteristics[4]

V_{VDD} = 3.0V, T_A = +25°C, f_{REFOSC} = 9.84375MHz for 315MHz, f_{REFOSC} = 13.560MHz for 433.92MHz, ASK = EN = VDD. MICRF/MAQRF112 50Ω Evaluation Board. Bold values indicate T_A = –40°C to +125°C unless otherwise noted. 1Kbps data rate, 50% duty cycle, pulse width = 500µs.

Parameter	Condition		Min	Typ	Max	Units
Power Supply						
Standby Supply Current	V_{VDD} = 3.6V, V_{EN} = 0V			0.05	**3**	µA
Mark Supply Current	f_{RF} = 315MHz	V_{VDD} = V_{ASK} = 3.0V		11.5		mA
		V_{VDD} = V_{ASK} = 3.6V		12.1	**14.5**	mA
	f_{RF} = 433.92MHz	V_{VDD} = V_{ASK} = 3.0V		11.6		mA
		V_{VDD} = V_{ASK} = 3.6V		12.1	**15.0**	mA
SPACE Supply Current	f_{RF} = 315MHz	V_{VDD} = 3.0V, V_{ASK} = 0V		2.4		mA
		V_{VDD} = 3.6V, V_{ASK} = 0V		2.5	**3.5**	mA
	f_{RF} = 433.92MHz	V_{VDD} = 3.0V, V_{ASK} = 0V		2.7		mA
		V_{VDD} = 3.6V, V_{ASK} = 0V		2.8	**3.8**	mA
ASK Modulated Supply Current	f_{RF} = 315MHz	V_{VDD} = 3.0V, V_{ASK} = 1kHz		6.9		mA
	f_{RF} = 433.92MHz	V_{VDD} = 3.0V, V_{ASK} = 1kHz		7.2		mA
RF Output Section and Modulation Limits						
Output Power Level	V_{ASK} = 3.0V	f_{RF} = 315MHz	**5**	10		dBm
		f_{RF} = 433.92MHz	**6**	10		dBm
Harmonic Output	f_{RF} = 315MHz	$f_{HARMONIC}$ = 630MHz		–53		dBc
		$f_{HARMONIC}$ = 945MHz		–53		dBc
	f_{RF} = 433.92MHz	$f_{HARMONIC}$ = 867.84MHz		–51		dBc
		$f_{HARMONIC}$ = 1301.76MHz		–65		dBc
Extinction Ratio for ASK	f_{RF} = 315MHz			80		dBc
	f_{RF} = 433.92MHz			90		dBc
FSK Modulation						
Maximum Data Rate	Manchester Encoded (50% Duty Cycle)[4]			10		Kbps
Maximum Frequency Deviation	Crystal = HC49/US, load capacitor = 10pF[4]			±25		kHz
XTAL_MOD to VSS Impedance, RDSon	FSK = VSS		**1**			MΩ
	FSK = VDD			15	**35**	Ω
ASK Modulation						
Maximum Data Rate	Manchester Encoded (50% Duty Cycle)			50		kbps

Parameter	Condition		Min	Typ	Max	Units
Occupied Bandwidth	f_{RF} = 315MHz[5]			630		kHz
	f_{RF} = 433.92MHz[5]			670		kHz
VCO Section						
Single Side-Band Phase Noise	f_{RF} = 315MHz	f_{OFFSET} = 100kHz		–76		dBc/Hz
		f_{OFFSET} = 1000kHz		–79		dBc/Hz
	f_{RF} = 433.92MHz	f_{OFFSET} = 100kHz		–72		dBc/Hz
		f_{OFFSET} = 1000kHz		–81		dBc/Hz
Reference Oscillator Section						
XTLIN, XTLOUT, XTLMOD	Pin capacitance			2		pF
Oscillator Start-Up Time	Crystal: HC49S, Note 4			400		µs
Digital/Control Section						
Digital Input Threshold Voltage (EN, ASK, and FSK)	High (V_{IH})		**0.8V_{DD}**			V
	Low (V_{IL})				**0.2V_{DD}**	V
Digital Input Current (EN, ASK, and FSK)	High (I_{IH}), V_{DD} = 3.6V			0.05	**1**	µA
	Low (I_{IL}), V_{DD} = 3.6V			0.05	**1**	µA
Supply Undervoltage Lock Out (UVLO)				1.6		V

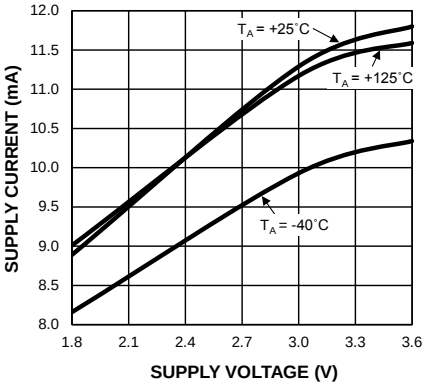
Notes:

1. Exceeding the absolute maximum ratings can damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
4. Dependent on crystal.
5. RBW = 100kHz, OBW measured at –20dBc.
6. Data rate = 50kbps, pulse width = 10µs, pulse repetition time = 20µs.

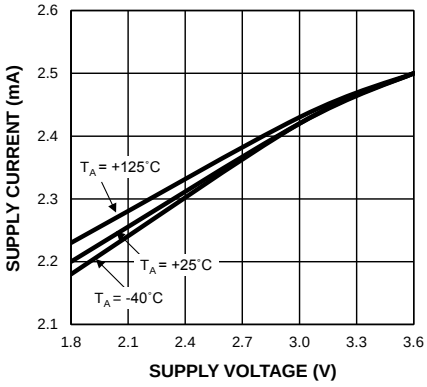
Typical Characteristics

(MAQRF112, 50Ω Evaluation Board, V_{VDD} = 3.0V, V_{ASK} = V_{EN} = VDD, T_A = +25°C unless otherwise noted)

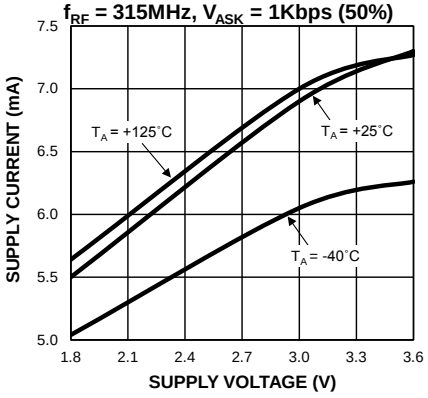
Supply Current vs. Supply Voltage
f_{RF} = 315MHz, V_{ASK} = VDD



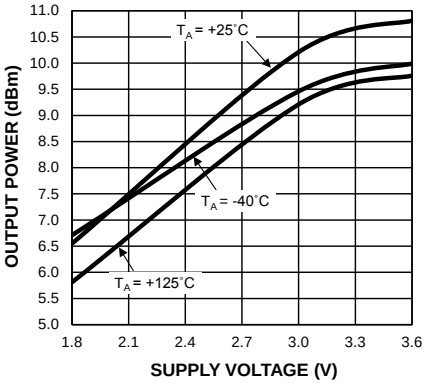
Supply Current vs. Supply Voltage
f_{RF} = 315MHz, V_{ASK} = GND



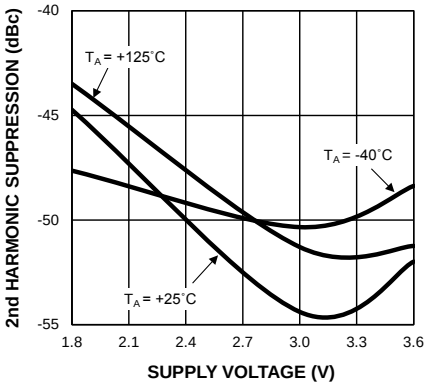
ASK Modulated
Supply Current vs. Supply Voltage
f_{RF} = 315MHz, V_{ASK} = 1Kbps (50%)



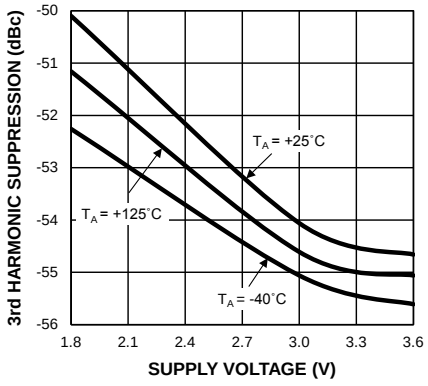
Output Power vs. Supply Voltage
f_{RF} = 315MHz, V_{ASK} = VDD



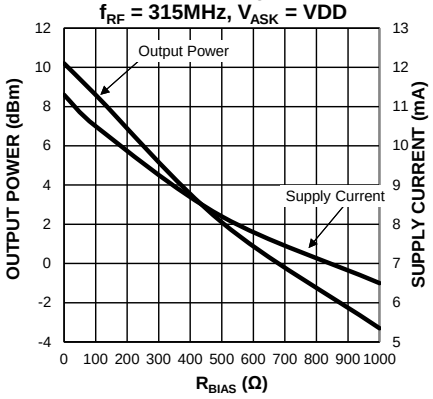
2nd Harmonic vs. Supply Voltage
f_{RF} = 315MHz, V_{ASK} = VDD



3rd Harmonic vs. Supply Voltage
f_{RF} = 315MHz, V_{ASK} = VDD

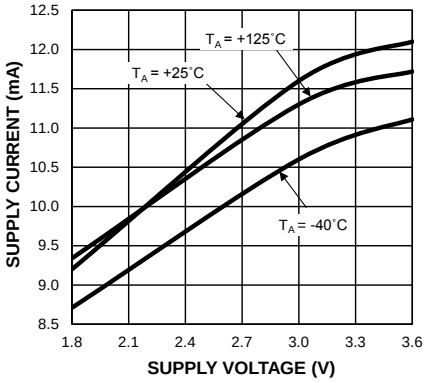


Output Power and Supply Current
vs. R_{BIAS}
f_{RF} = 315MHz, V_{ASK} = VDD

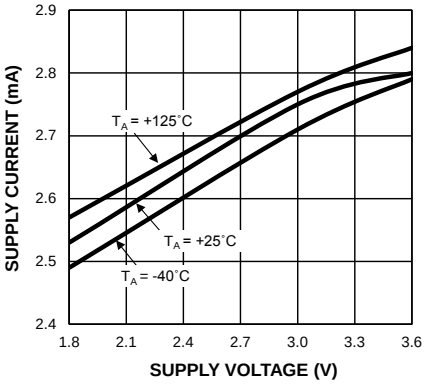


Typical Characteristics (Continued)

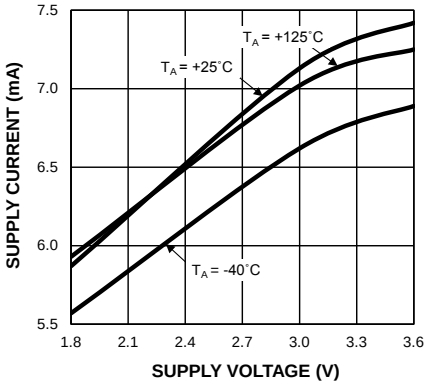
Supply Current vs. Supply Voltage
f_{RF} = 433.92MHz, V_{ASK} = VDD



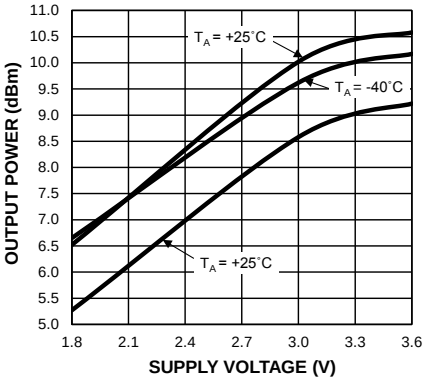
Supply Current vs. Supply Voltage
f_{RF} = 433.92MHz, V_{ASK} = GND



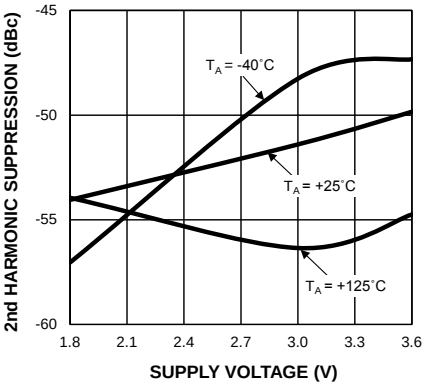
Supply Current vs. Supply Voltage
f_{RF} = 433MHz, V_{ASK} = 1Kbps (50%)



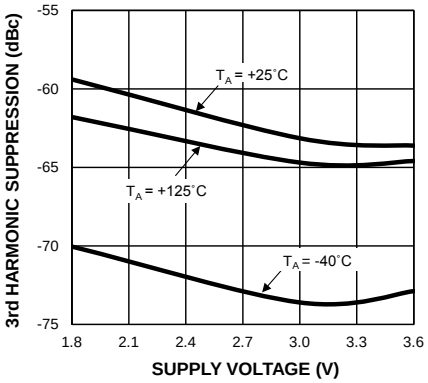
Output Power vs. Supply Voltage
f_{RF} = 433.92MHz, V_{ASK} = VDD



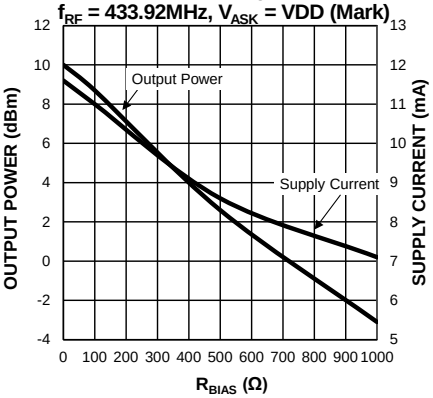
2nd Harmonic vs. Supply Voltage
f_{RF} = 433MHz, V_{ASK} = VDD



3rd Harmonic vs. Supply Voltage
f_{RF} = 433.92MHz, V_{ASK} = VDD



Output Power and Supply Current
vs. R_{BIAS}
f_{RF} = 433.92MHz, V_{ASK} = VDD (Mark)



Functional Diagram

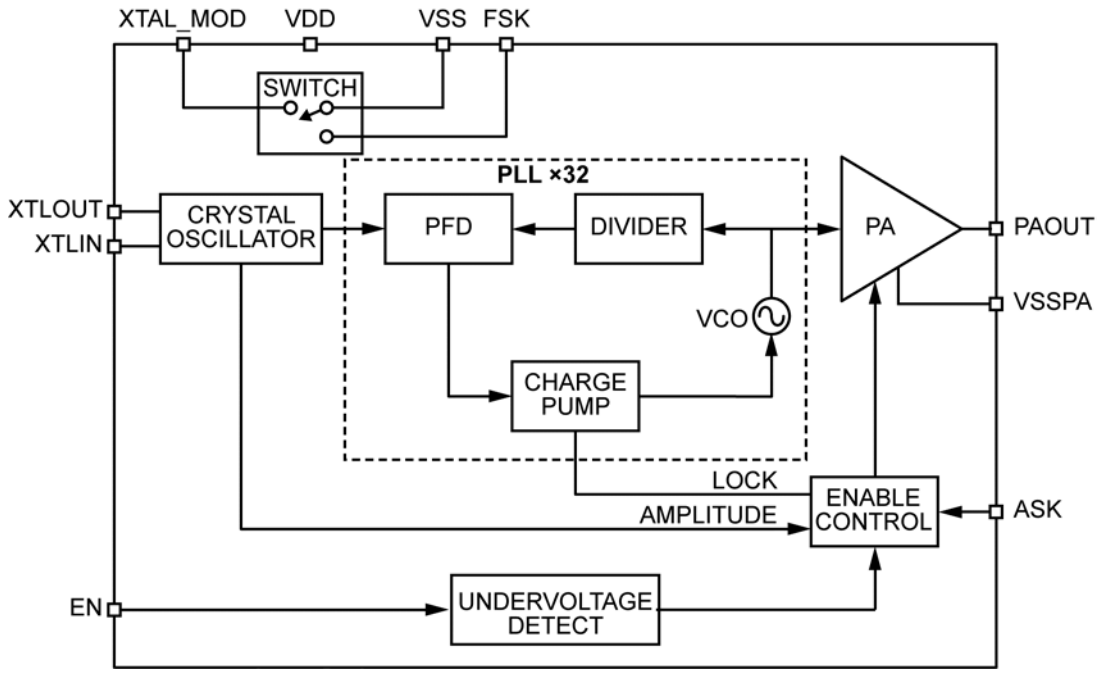


Figure 1. Functional Block Diagram MAQRF112

Functional Description

The MAQRF112 is a 1.8V to 3.6V, 300MHz to 450MHz, +10dBm ASK/FSK transmitter. It has an integrated crystal oscillator, phase-locked loop (PLL), voltage-controlled oscillator (VCO), power amplifier (PA), undervoltage lockout (UVLO) and three logic-level inputs for ASK modulation/PA enable, FSK modulation, and on/off control. The device requires only a crystal, crystal loading capacitors, supply bypassing capacitors, and a few output matching components to match the PA to the load (loop antenna, 50Ω load, or whip antenna).

The device achieves ASK modulation using on and off modulation of the power amplifier. FSK modulation is achieved by pulling the crystal oscillator when an on-chip switch shunts an additional capacitance across the crystal.

The MAQRF112 is enabled or placed into a low-power shutdown mode through the logic-level EN input. An undervoltage lockout disables the PA until the power supply has reached a valid operating range. The only external components required are a crystal, antenna matching components, and power supply bypassing. Figure 1 shows the block diagram of the MAQRF112.

Phase-Locked Loop (PLL) Synthesizer

The PLL of the MAQRF112 integrates a VCO, a “Divide-by-32” frequency divider, a phase-frequency detector (PFD), a charge pump, and a loop -filter. The VCO tunes from 300MHz to 450MHz and drives both the PA and the divider. The divider divides the VCO frequency by 32, and the PFD compares the divided frequency against the reference frequency generated by the crystal oscillator. Any phase difference between these signals generates a current into the loop filter, which closes the loop with the VCO providing a precise, low phase-noise VCO, with quick start-up time. The PLL also includes an internal Lock indicator which will keep the PA disabled until the PLL has locked.

Crystal Oscillator

The crystal oscillator provides a precision reference frequency to the PLL. The MAQRF112 uses a Pierce oscillator, which is operated in parallel resonant mode. It is designed to accept fundamental mode crystals, which operate from 9.375MHz to 14.0625MHz, to accommodate the "Divide-by-32" divider of the PLL. The crystal frequency is:

$$f_{XTAL} = f_{RF} \div 32 \qquad \text{Eq. 1}$$

Most applications require an initial frequency tolerance of <±30ppm at T_A = +25°C and an overtemperature stability of ±25ppm to ±50ppm, but that can vary depending on the desired operating temperature range and performance required versus crystal cost. The MAQRF112 Pierce oscillator can work with values of equivalent series resistance (ESR) in the range of 5Ω to 300Ω.

ASK Crystal Oscillator Operation

Figure 2 shows a reference oscillator circuit configuration for ASK operation. The crystal is placed between the XTLIN (pin 2) and XTLOUT (pin 3). Table 1 shows corresponding ESR values to crystal parameter values. C_{PAR} is the parallel capacitance determined from internal crystal substrate contacts and board parasitic capacitance.

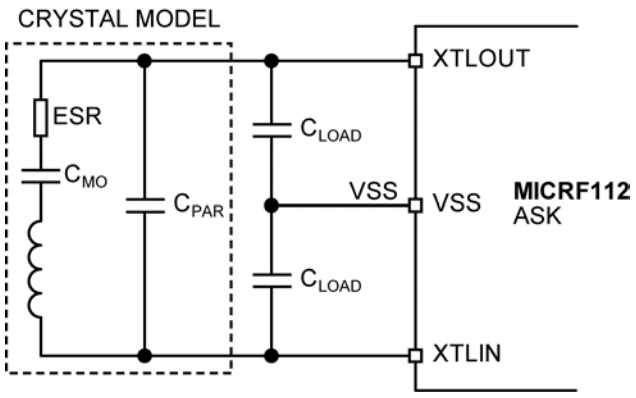


Figure 2. Reference Oscillator ASK Operation

ESR (Ω)	C_{PAR} (pF)	C_{MO} (fF)	C_{LOAD} (pF)
20	1 to 10	10 to 40	10 to 70
300	1 to 5	10 to 40	10 to 30

Table 1. Recommended Crystal Oscillator Values

Referring to Figure 2, Equation 2 is an example of C_{L1} and C_{L2} calculation for a crystal load capacitance, C_{LOAD} = 10pF. The load capacitance seen by the crystal is calculated as follows:

$$C_{LOAD} = \frac{1}{\frac{1}{C_{L1}} + \frac{1}{C_{L2}}} + C_{STRAY} \qquad \text{Eq. 2}$$

Therefore, the calculation of C_{L1} and C_{L2} for a specified C_{LOAD} of 10 pF is as follows:

C_{STRAY} = 1.5pF (stray pin and PCB capacitance)

$C_{L1} = C_{L2} = (C_{LOAD} - C_{STRAY}) \times 2$

$C_{L1} = C_{L2}$ = 18pF

The final value of C_{L1} and C_{L2} may need to be optimized on the bench because of board stray parasitics.

Capacitors, C_{L1} and C_{L2}, are placed from XTLIN to ground and from XTLOUT to ground. When specifying a crystal to a crystal manufacturer, the load capacitance, C_{LOAD}, must be specified as part of the manufacturing crystal design.

For ASK-only operation, connect the FSK pin to VSS and leave XTAL_MOD unconnected.

FSK Operation

Figure 3 shows the reference oscillator circuit configuration for FSK operation. To operate the MAQRF112 device in FSK mode, one additional capacitor, C_{FSK}, is needed between the XTLOUT pin and the XTAL_MOD pin. Crystal parameters for FSK operation are the same as for ASK operation except:

- When the ESR of the crystal is at 20Ω, $C_{FSK} + C_{LOAD}$ must not exceed 70pF.
- When the ESR of the crystal is at 300Ω, $C_{FSK} + C_{LOAD}$ must not exceed 30pF.

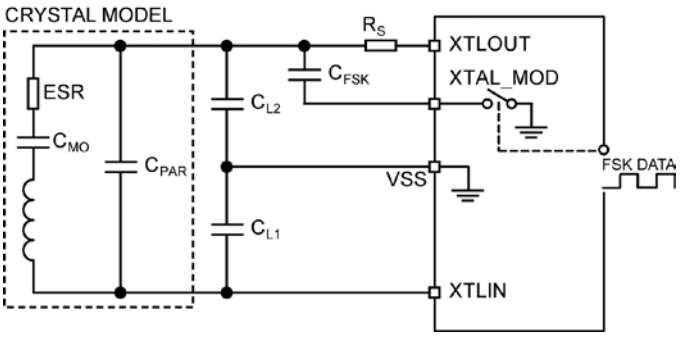


Figure 3. Reference Oscillator FSK Operation

C_{L1}, C_{L2} and C_{FSK} Calculation

Referring to Figure 3, C_{L1}, C_{L2}, and C_{FSK} values depend on C_{LOAD}. Capacitor calculation is similar to ASK operation, with the addition of a shunt capacitor, C_{FSK}. Selection of C_{L1}, C_{L2}, and C_{FSK} determine RF center frequency, high-side, and low-side RF frequency. See Figure 4.

Use Equation 3 to calculate the FSK high-side frequency calculation.

$$C_{LOAD} = \frac{1}{\frac{1}{C_{L1}} + \frac{1}{C_{L2}}} + C_{STRAY} \qquad \text{Eq. 3}$$

Use Equation 4 to calculate the FSK low-side frequency calculation.

$$C_{LOAD} = \frac{1}{\frac{1}{C_{L1}} + \frac{1}{C_{L2} + C_{FSK}}} + C_{STRAY} \qquad \text{Eq. 4}$$

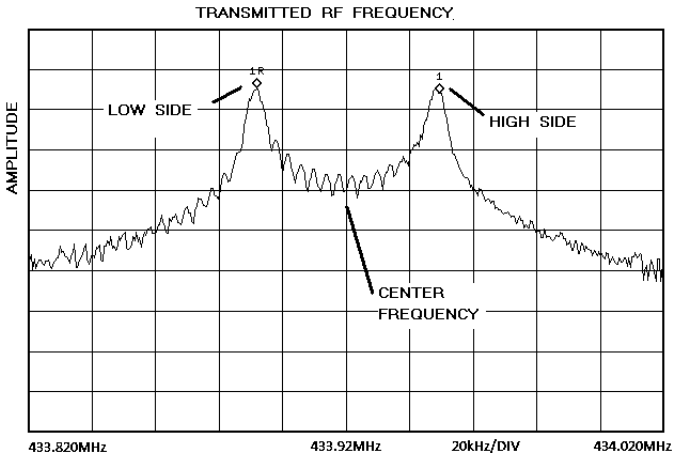


Figure 4. MAQRF112 Frequency Deviation

FSK modulation is achieved by pulling the crystal at the desired data rate. Pulling the crystal frequency is done by shunting C_{FSK} with C_{L2}. A logic-level LOW on the FSK data input opens the internal switch, removing C_{FSK}, which pulls the reference oscillator high. A logic-level HIGH closes the switch, paralleling the crystal C_{FSK} with C_{L2}, which pulls the reference frequency low. See Figure 4. R_S is used to minimize crystal RF spurs when using a low-quality crystal. A typical value of R_S is 0Ω to 1000Ω and depends on the crystal chosen. Board-level optimization is required to optimize for frequency deviation and occupied bandwidth requirements.

Power Amplifier

The power amplifier serves two purposes: to buffer the VCO from external elements and to amplify the phase-locked signal. The power amplifier can produce +10dBm at 3V (typical). The PA output matching network to a 50Ω load or to a PCB antenna serves two purposes: to optimize PA output power and to minimize unwanted harmonics. Matching values are a function of operational frequency and load impedance seen by the MAQRF112. The “Application Information” section provides matching values for 315MHz and 433.92MHz.

Power Control Using an External Resistor

A resistor (R7 on the 50Ω evaluation board) is in series with the output RF choke and can be used to adjust the RF output power and supply current. This adjustment can also be used to lower the power to meet FCC compliance. See the “Output Power and Supply Current vs. R_{BIAS}” graphs in the “Typical Characteristics” section for examples of performance on the 50Ω evaluation boards. An evaluation board using a PCB antenna can have its radiated power lowered by adjusting this series resistor. The resistor value must be calibrated empirically, and will vary depending on the final product PCB layout and form factor.

Enable Control

The Enable control gates the ASK data to the PA. It allows transmission only when the lock, crystal amplitude, and undervoltage detect conditions are valid. An Enable and ASK logic-level HIGH places the PA in the Mark condition. An Enable logic-level LOW disables the power amplifier. An Enable logic-level HIGH and an ASK logic-level LOW places the PA in the Space condition. To transmit with FSK modulation, both the EN and ASK pins must be set to a logic-level HIGH while the FSK pin is digitally modulated with a logic-level signal.

ASK Input Control

An ASK logic-level data input modulates the RF carrier when the PA is enabled. Apply a data stream less than 50Kbps (Manchester Encoded, 50% duty-cycle) for ASK modulation. Tying the FSK pin low is recommended when ASK modulation is used.

Undervoltage Detect

The undervoltage detect block senses the operating voltage. If the operating voltage falls below 1.6V, the undervoltage detect block sends a signal to the enable control block to disable the PA.

Application Information

The MAQRF112 is ideal for driving a 50Ω load monopole or a PCB loop antenna. The following sections discuss PCB loop antenna and 50Ω output configurations.

Output Matching Network

Part of the function of the output network is to attenuate the second and third harmonics. When matching to a transmit frequency, take care not only to optimize for maximum output power but to attenuate unwanted harmonics. Proper matching to a PCB antenna or a 50Ω load optimizes current requirements.

Layout Issues

PCB layout is extremely important to achieve optimum performance and consistent manufacturing results. Be careful with the orientation of the components to ensure that they do not couple or decouple the RF signal. PCB trace length should be short, to minimize parasitic inductance (1in ~ 20nH). For example, depending on inductance values, a 0.5in trace can change the inductance by as much as 10%. To reduce parasitic inductance, the use of wide traces and a ground plane under signal traces is recommended. Use vias with low inductance values for components requiring a connection to ground.

Crystal PCB Layout

Crystal PCB board layout affects the calculated frequency deviation. It is recommended that the crystal be located close to the XTLIN and XTLOUT pins to minimize trace lengths. Trace thickness should be no greater than 20mil.

Antenna Layout

The antenna trace layout affects directivity. No ground plane should be under the antenna trace. For consistent performance, do not place components inside the loop of the antenna. Gerbers for a suggested layout are available on the Micrel website at: www.micrel.com.

ASK PCB Loop Antenna Application Circuit

Figure 5 is an example of an ASK circuit configuration using a PCB loop antenna. Table 2 lists modified values for both 315MHz and 433.92MHz configurations, including crystal values for 315MHz and 433.92MHz operation. Values are dependent on PCB board layout. Refer to the Micrel website for a reference design and PCB Gerber files.

Frequency (MHz)	L1 (nH)	C5 (pF)	L4 (nH)	C7 (pF)	Y1 (MHz)
315	470	10	150	4.7	9.84375
433.92	680	10	82	3.9	13.5600

Table 2. PCB Antenna Matching Network

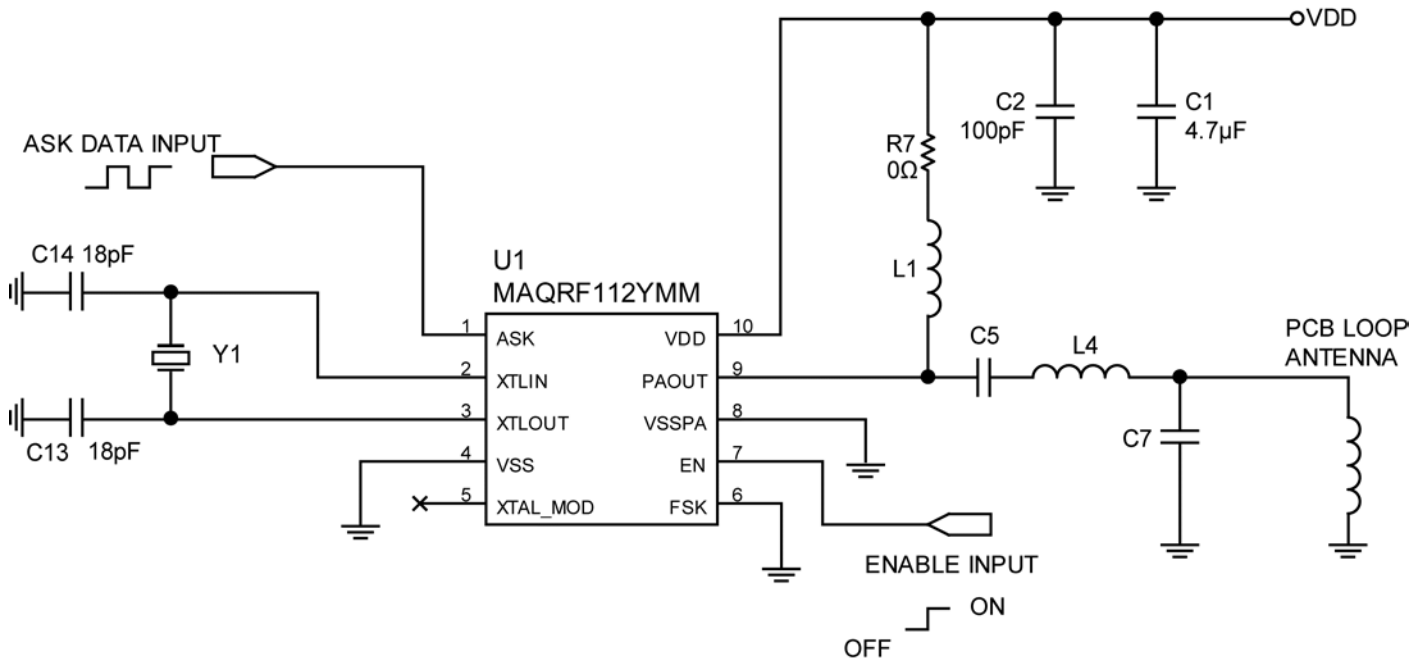


Figure 5. MAQRF112 ASK Application Circuit with PCB Loop Antenna

FSK PCB Loop Antenna Application Circuit

Figure 6 is an example of a FSK circuit configuration using a PCB loop antenna. Table 3 lists modified values for both 315MHz and 433.92MHz configurations, including crystal values for 315MHz and 433.92MHz operation. Antenna matching values are dependent on PCB board layout. Refer to the Micrel website for a reference design and PCB Gerber files. Table 4 lists crystal capacitor load values for a frequency deviation of ±25kHz. For crystal capacitor calculations, refer to the "FSK Operation" section.

Frequency (MHz)	L1 (nH)	C5 (pF)	L4 (nH)	C7 (pF)	Y1 (MHz)
315	470	10	150	4.7	9.84375(1)
433.92	680	10	82	3.9	13.5600(2)

Table 3. PCB Antenna Matching Network

Notes:

1. Y1 = Abracon ABLS-9.84375MHz-10-R50-K4Q for 315MHz
2. Y1 = Abracon ABLS-13.5600MHz-10-R50-K4Q for 433.92MHz

Center Frequency (MHz)	C14 (pF)	C13 (pF)	C8 (pF)	Frequency Deviation (kHz)
315	15	10	22	±25
433.92	18	6.8	15	±25

Table 4. Crystal Capacitor Values for FSK Operation

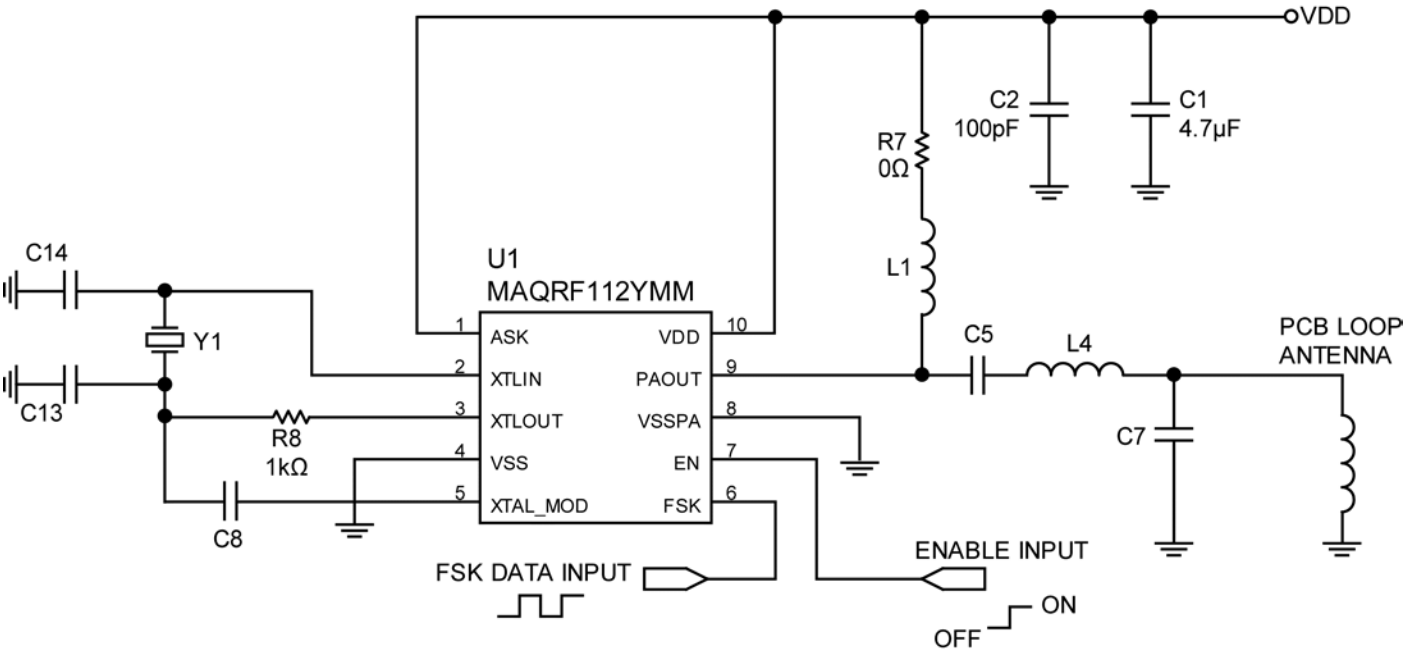


Figure 6. MAQRF112 FSK Application Circuit with PCB Loop Antenna

ASK 50Ω Load Application Circuit

Figure 7 is an example of an ASK circuit configuration used to drive a 50Ω load. Table 5 lists modified values for both 315MHz and 433.92MHz configurations, including crystal values for 315MHz and 433.92MHz operation. The matching network values are dependent on PCB board layout. Refer to the Micrel website for a reference design and the PCB Gerber files

Frequency (MHz)	L1 (nH)	C5 (pF)	L2 (nH)	C7 (pF)	C11 (pF)	Y1 (MHz)
315	470	8.2	82	8.2	2.2	9.84375
433.92	470	2.2	82	6.8	1.2	13.5600

Table 5. 50Ω Load Matching Network

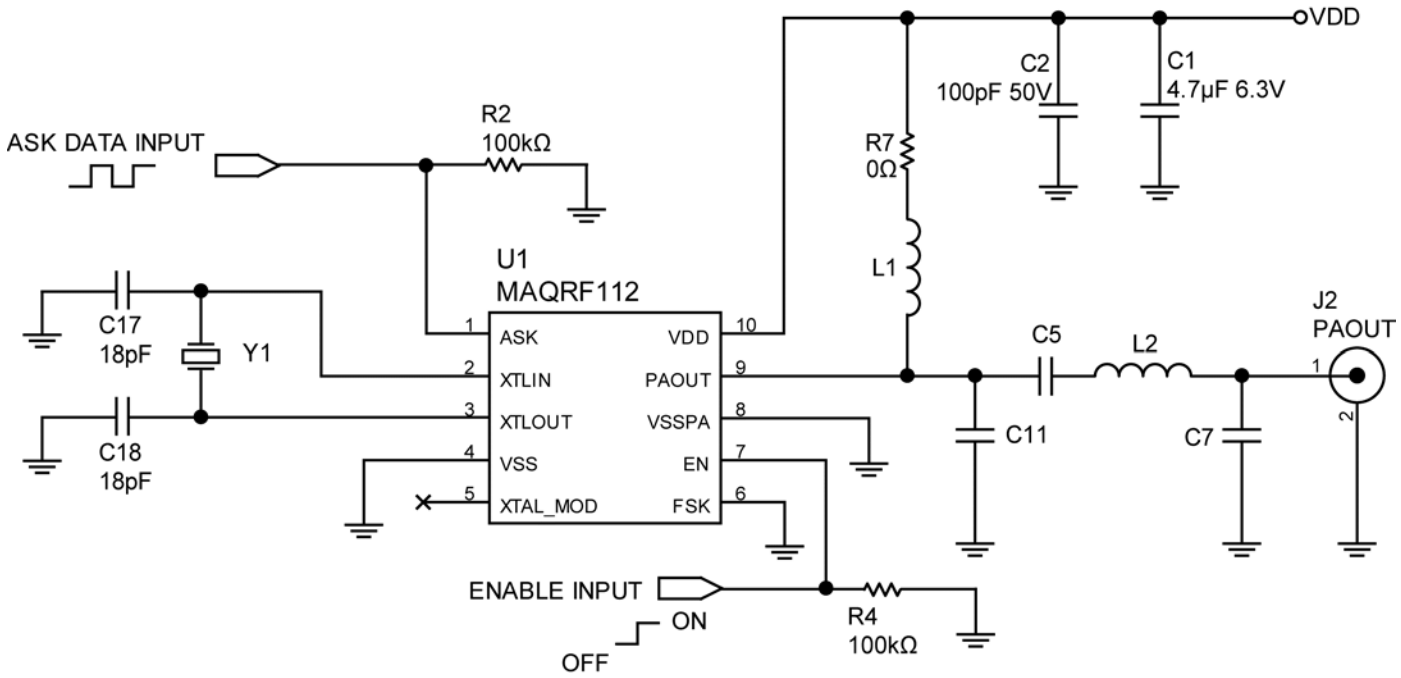


Figure 7. MAQRF112 ASK 50Ω Evaluation Board

FSK- 50Ω Load Application Circuit

Figure 8 is an example of a FSK circuit configuration used to drive a 50Ω load. Table 6 lists modified values for both 315MHz and 433.92MHz configurations, including crystal values for 315MHz and 433.92MHz operation. The matching network values are dependent on PCB board layout. Refer to the Micrel website for a reference design and PCB Gerber files. Table 7 lists crystal capacitor load values for a frequency deviation of ±25 kHz. For crystal capacitor calculations, refer to the "FSK Operation" section.

Frequency (MHz)	L1 (nH)	C5 (pF)	L2 (nH)	C7 (pF)	C11 (pF)	Y1 (MHz)
315	470	8.2	82	8.2	2.2	9.84375(1)
433.92	470	2.2	82	6.8	1.2	13.5600(2)

Table 6. 50Ω Load Matching Network

Notes:

1. Y1 = Abracon ABLS-9.84375MHz-10-R50-K4Q for 315MHz
2. Y1 = Abracon ABLS-13.5600MHz-10-R50-K4Q for 433.92MHz

Center Frequency (MHz)	C17 (pF)	C18 (pF)	C9 (pF)	Frequency Deviation (kHz)
315	15	10	22	±25
433.92	18	6.8	15	±25

Table 7. 50Ω Load Matching Network

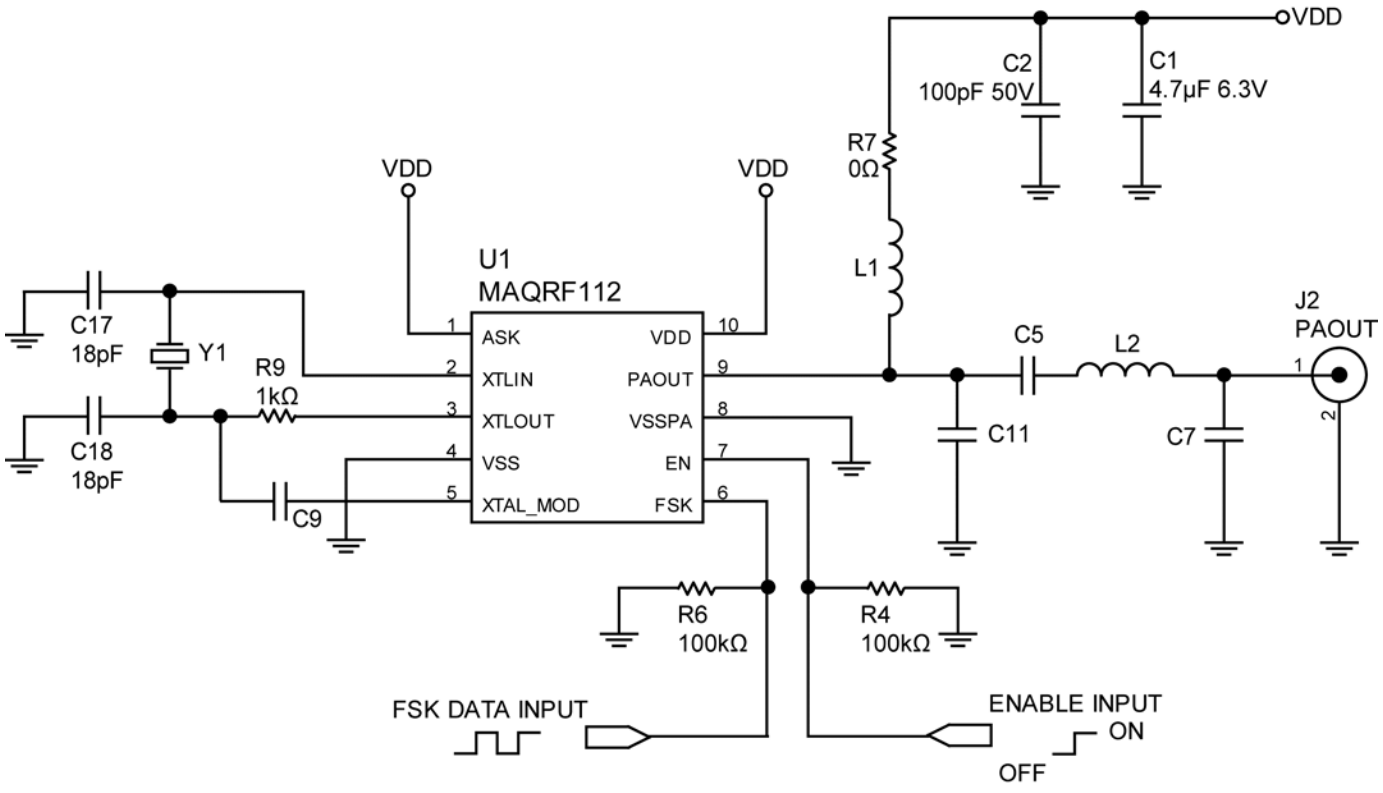
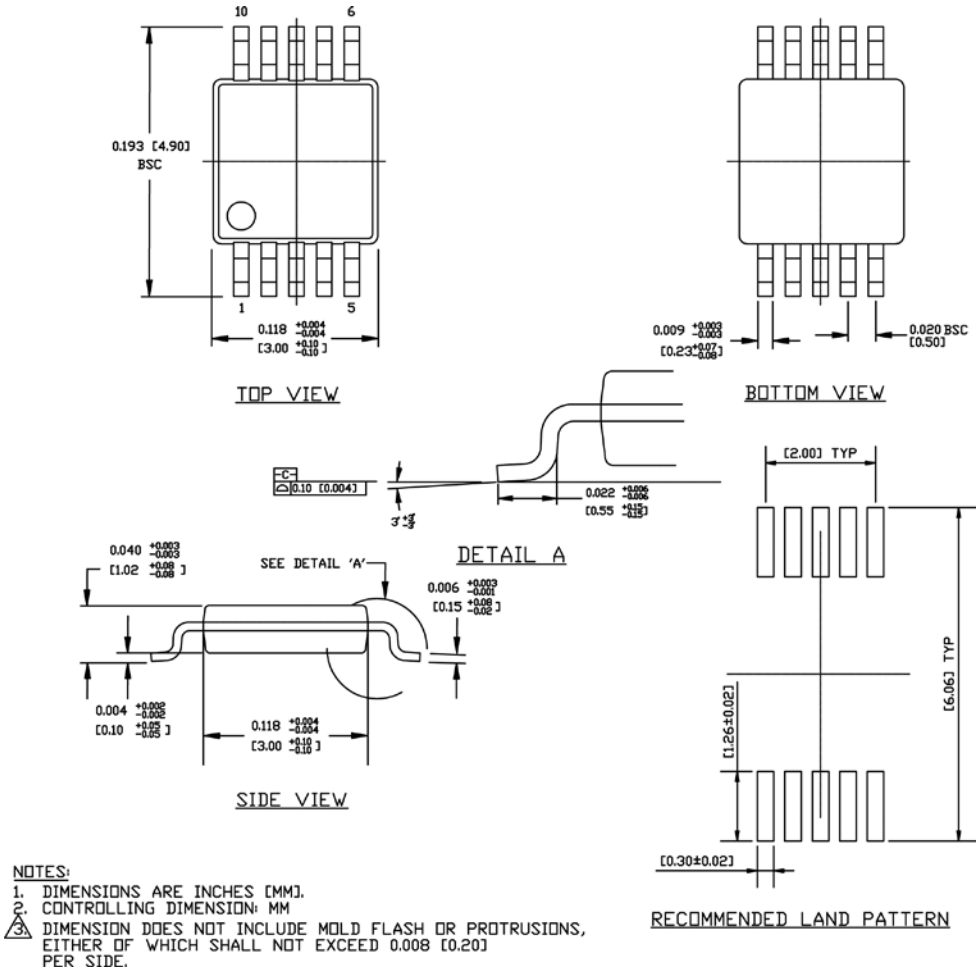


Figure 8. MAQRF112 FSK 50Ω Evaluation Board

Package Information(1)



10-Pin MSOP Package Type (YMM)

Note:

1. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com