Pin Configuration and Pinout

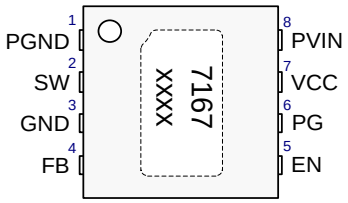


Figure 2 · **Pinout DFN 2mmx2mm 8L Top View**

Marking: First Line 7167

Second Line YWWA (Year/Work Week/Lot Code)

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-10°C to 85°C	RoHS Compliant, Pb-free	DFN 2mmx2mm 8L	LX7167CLD	Bulk / Tube
			LX7167CLD-TR	Tape and Reel

Pin Description

Pin Number	Pin Designator	Description
1	PGND	Ground pin for the power stage.
2	SW	Switch-node pin. Connect the output inductor between this pin and output capacitor. When the chip is DISABLED, the internal discharge resistor will be enabled to discharge the output capacitance. The current will flow into this pin.
3	GND	Ground pin.
4	FB	Voltage feedback pin. Connect to the output terminal through a resistor divider network to set the output voltage of the regulator to the desired value.
5	EN	Pull this pin higher than 1V will enable the controller. When pulled low, the IC will turn off and the Internal discharge FET will turn on to discharge the output capacitor through the SW pin.
6	PG	Power-good pin. This is an open-drain output and should be connected to a voltage rail with an external pull-up resistor. During the power on, this pin switches from LOW to HI state when FB voltage reaches above the power good threshold and the internal soft start has finished its operation. It will be pulled low when the FB falls below the power-good threshold minus the hysteresis. It will turn back on when the pull FB rises above the threshold.
7	VCC	Analog input voltage terminal. Connect this pin to VIN with a 10ohm resistor and connect a 1µF ceramic capacitor from VCC to GND.
8	PVIN	Input voltage terminal of the regulator. A minimum of 10µF, X5R type ceramic capacitor must be connected as close as possible from this pin to PGND plane to insure proper operation.
	Power PAD	For good thermal connection, this PAD must be connected using thermal VIAs to the GND plane and to the LAND pattern of the IC.

Block Diagram

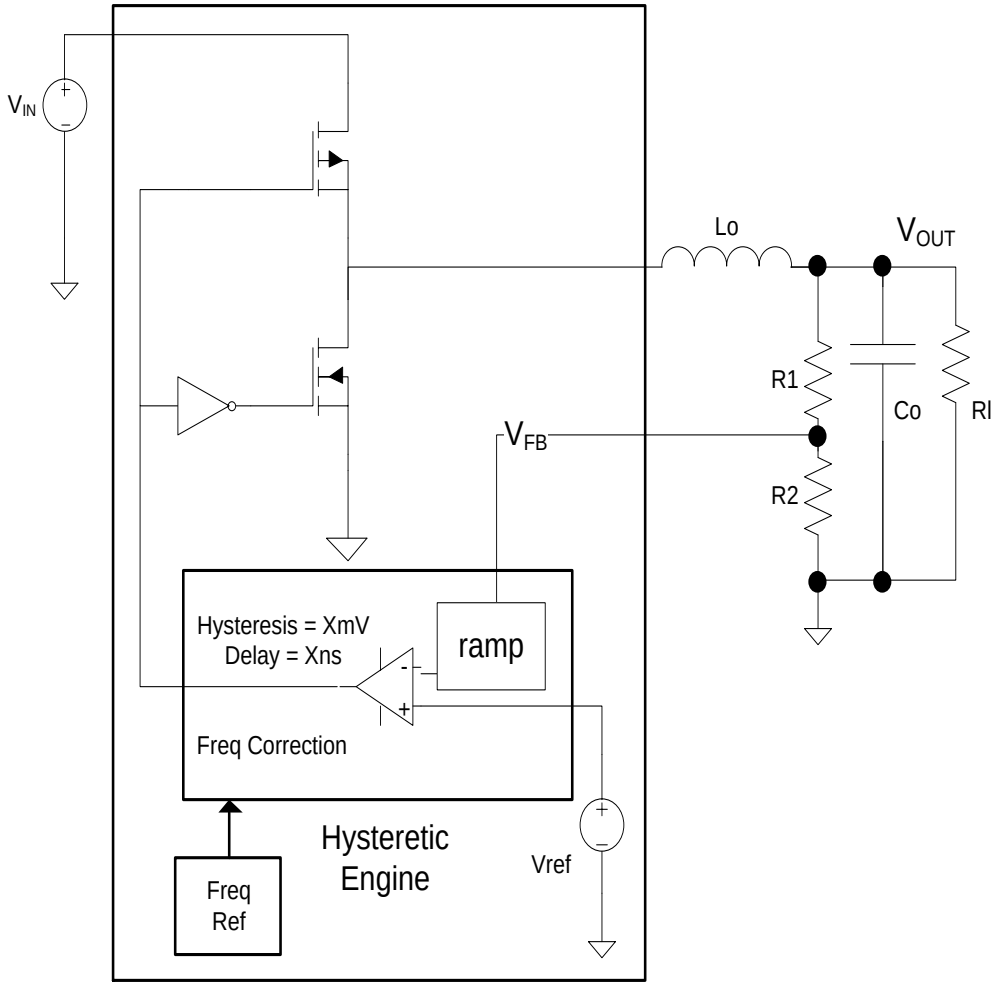


Figure 3 · **Simplified Block Diagram of LX7167**

Absolute Maximum Ratings

Parameter	Min	Max	Units
PVIN, EN, FB, PG to GND	-0.3	7	V
SW to GND	-0.3	7	V
SW to GND (Shorter than 50ns)	-2	7	V
Junction Temperature	0	150	°C
Storage Temperature	-65	150	°C
Peak Package Solder Reflow Temperature (40s, reflow)		260 (+0,-5)	°C

Note: Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability

Operating Ratings

Parameter	Min	Max	Units
VCC, PVIN	3	5.5	V
V_{OUT}	0.6	VIN – 0.5	V
Ambient Temperature	-10	85	°C
Output Current	0	2.4	A

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	75	°C/W

Note: The θ_{JA} number assumes no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Note: Unless otherwise specified, the following specifications apply over the operating ambient temperature of $-10°C \le T_A \le 85°C$ except where otherwise noted with the following test conditions: VCC = PVIN = 5V. Typical parameter refers to $T_J = 25°C$

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Operating Current						
I_Q	Input Current	$I_{LOAD} = 0$		350		µA
I_{SHDN}	Input Current at Shut Down	V_{EN} = GND		0.1	2	µA
PVIN Input UVLO						
PVIN	Under Voltage Lockout	PVIN rising		2.4	2.8	V
	UVLO Hysteresis			260		mV

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
FEEDBACK						
V_{REF}	Feedback Voltage	T_A = 25°C	0.594	0.600	0.606	V
		-10°C to 85°C	0.591		0.609	
I_{FB}	FB Pin Input Current				10	nA
	Line Regulation	PVIN from 3V to 5.5V		0.70		%
	Load Regulation	I_{LOAD} = 0 to 2A. Note 1		1.0		%/A
FB UVLO						
V_{FBUVLO}	FB UVLO Threshold			70		$\%V_{REF}$
OUTPUT DEVICE						
R_{DSON_H}	R_{DSON} of High Side			95	150	mΩ
R_{DSON_L}	R_{DSON} of Low Side			75	100	mΩ
I_L	Peak Current Limit		2.6	3.5	4.5	A
T_{SH}	Thermal Shutdown Threshold			150		°C
T_H	Thermal Shutdown Hysteresis			20		°C
PVIN OVP						
OVP_R	Rising Threshold			6.1		V
OVP_F	Falling Threshold		5.5			V
OSCILLATOR FREQUENCY						
f	Switching Frequency		2.6	3	3.4	MHz
SOFT START						
T_{SS}	Soft Start Time	From EN High to V_{OUT} reach regulation		500		µs
T_{HICCUP}	Hiccup Time	V_{FB} = 0.2V		1.2		ms
EN INPUT						
EN_{VIN}	Input High		1			V
EN_{VIL}	Input Low				0.4	V
EN_H	Hysteresis			0.1		V
EN_{II}	Input Bias			0.01	1	µA
PG (Power Good)						
V_{PG}	Power Good Transition High Threshold			83		%
V_{PGHY}	Hysteresis	Either V_{FB} rising or falling		40		mV
PG_{RDSON}	Power Good Internal FET R_{DSON}	VCC = 5V		100	300	Ω
	PG FET Leakage Current			0.01	1	µA
	PG internal Glitch Filter	Note 1		5		µs
OUTPUT DISCHARGE						
	Internal Discharge Resistor		80	200	1400	Ω

Note 1: Guaranteed by design, not tested during production.

Typical Performance Curves -- (Efficiency)

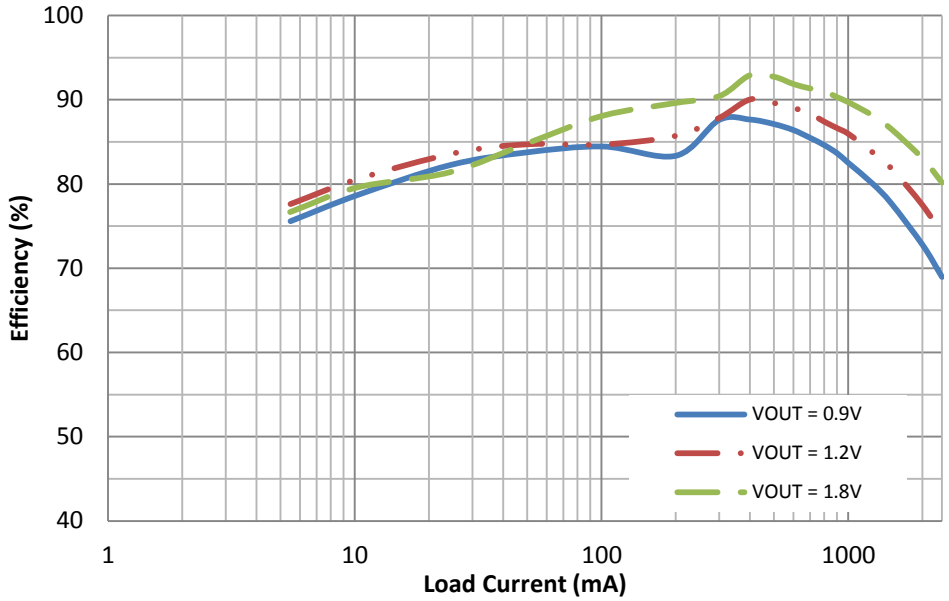


Figure 4 · **Efficiency vs. Output Current with 3.3V Input**

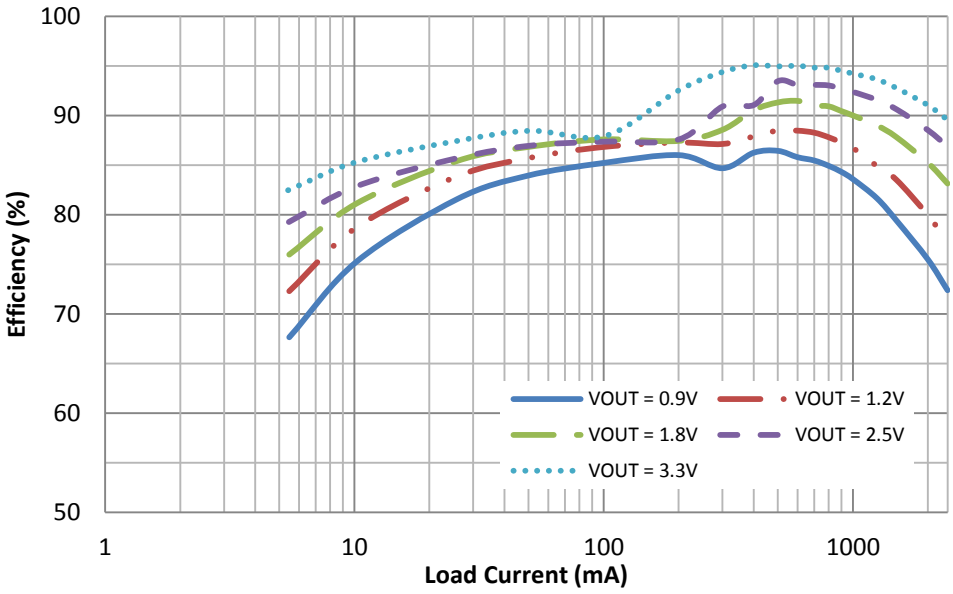


Figure 5 · **Efficiency vs. Output Current with 5V Input**

Typical Performance Curves -- (Step Load Response.)

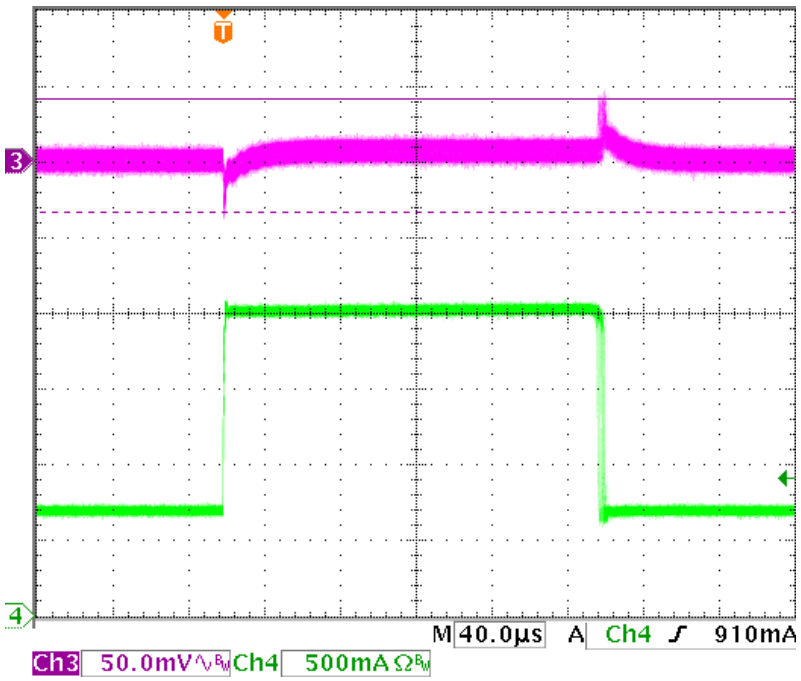


Figure 6 · **Step Response (V_{IN} = 5V, V_{OUT} = 3.3V, L = 0.47µH, C_{OUT} = 22µF)**

Theory of Operation / Application Information

Basic Operation

The operation of the controller consists of comparing the V_{FB} voltage to an internal reference. When the VFB voltage is lower than the V_{REF}, the upper switch turns on. When the VFB voltage is higher than V_{REF}, the upper switch turns off and the lower switch turns on. An internal ramp is used to stabilize the switching frequency and keep the V_{FB} immune to the output capacitor, C_O, value or parasitic components (i.e. esr, esl). In addition, a frequency control loop ensures the switching frequency is constant under continuous conduction mode of operation.

At light load, the converter automatically reduces the switching frequency to optimize efficiency while ensuring the ripple voltage is low.

Setting of the Output Voltage

The LX7167A develops a 0.6V reference voltage between the feedback pin, FB, and the signal ground. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

The output component values are recommended below.

VOUT	L	R1	R2	COUT	C9	
					5V input	3.3V input
1V	0.47µH & 0.68µH	66.5kΩ	100kΩ	22µF	10pF	
				2x22µF	15pF	
				4x22µF	22pF	
	1.0µH			22µF	15pF	12pF
				2x22µF	22pF	22pF
				4x22µF	27pF	27pF
1.8V	0.47µH & 0.68µH	100kΩ	49.9kΩ	22µF	10pF	
				2x22µF	15pF	
				4x22µF	22pF	
	1.0µH			22µF	15pF	
				2x22µF	22pF	
				4x22µF	27pF	
2.5V	0.47µH & 0.68µH	158kΩ	49.9kΩ	22µF	15pF	
				2x22µF	22pF	
				4x22µF	33pF	
	1.0µH			22µF	10pF	22pF
				2x22µF	15pF	27pF
				4x22µF	22pF	33pF
3.3V	0.47µH & 0.68µH	158kΩ	34.8kΩ	22µF	22pF	-
				2x22µF	33pF	-
				4x22µF	47pF	-
	1.0µH			22µF	22pF	-
				2x22µF	33pF	-
				4x22µF	47pF	-

Start Up

The reference (V_{REF}) is ramped up from zero voltage to 0.6V in 500µs. During this time, the PG is pulled low. When the reference reaches 0.6V, signaling the end of the soft start cycle, the PG pin will go high within 5µs.

Over Current Protection

The IC has the ability to protect against all types of short circuit protection. It has cycle by cycle short protection that turns off the upper MOSFET and ends the cycle when the current exceeds the OCP threshold, when this occurs, the off-time is at least 200ns before the upper FET is turned on again. After startup, if the FB pin drops below the Feedback UVLO threshold, the chip will go into a hiccup mode of operation. This helps to protect against a crowbar short circuit. The FB UVLO Alarm is not active during startup.

Hiccup Mode of Operation

Hiccup mode of operation will protect the IC during a short of the output. After startup, it will be triggered when the FB UVLO is exceeded.

Input Over Voltage Protection

The IC is protected against damage when the input voltage rapidly rises to the absolute maximum level. When the input voltage rises over the PVIN OVP rising threshold, the IC will turn off switching. It will resume switching when the input voltage drops below the PVIN OVP falling threshold with hysteresis.

Typical Application Diagram

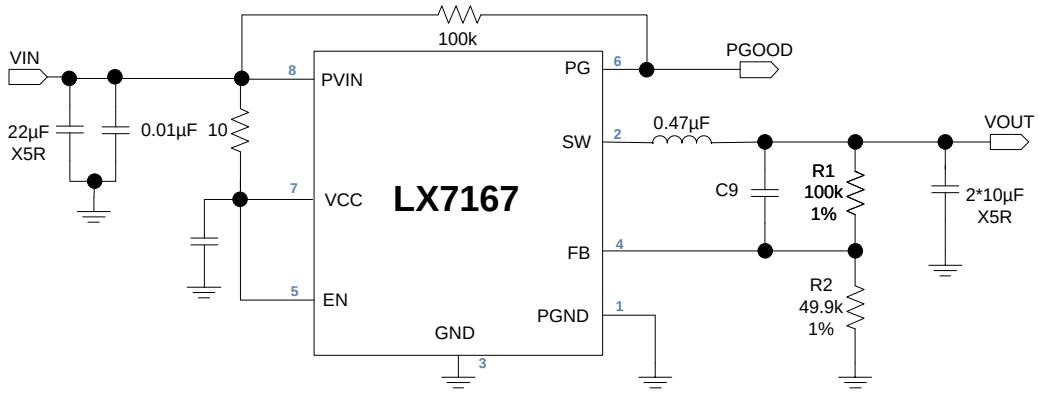
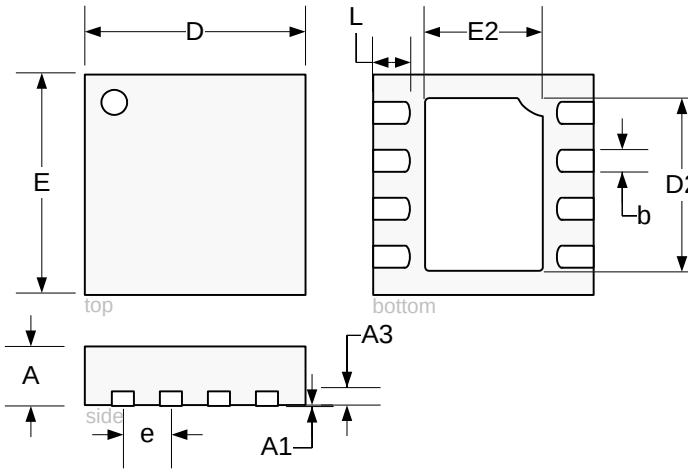


Figure 7 · **LX7167 Typical Application Diagram**

PACKAGE OUTLINE DIMENSIONS



Dim	MILLIMETERS		INCHES	
	MIN	**MAX**	**MIN**	**MAX**
A	0.70	0.80	0.0276	0.0315
A1	0	0.05	0	0.0020
A3	0.20 ref		0.0079 ref	
b	0.18	0.30	0.0071	0.0118
D	2.00 BSC		0.0787 BSC	
D2	1.55	1.80	0.0610	0.0709
e	0.50 BSC		0.0197 BSC	
E	2.00 BSC		0.0787 BSC	
E2	0.75	1.00	0.0295	0.0394
L	0.20	0.40	0.0079	0.0157

Figure 8 · **8 Pin Plastic DFN 2x2mm Dual Exposed Pad Package Dimensions**

Note: 1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006”) on any side. Lead dimension shall not include solder coverage.

Note: 2. Dimensions are in mm, inches are for reference only.

LAND PATTERN RECOMMENDATION

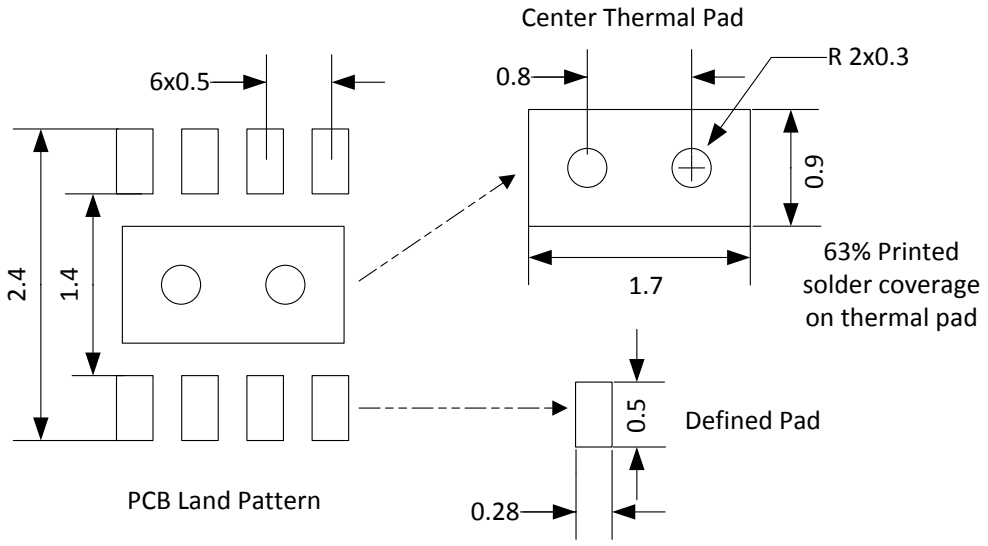


Figure 9 · **8 Pin Plastic DFN 2x2mm Dual Exposed Pad Package Footprint**

Disclaimer:
This PCB land pattern recommendation is based on information available to Microsemi by its suppliers. The actual land pattern to be used could be different depending on the materials and processes used in the PCB assembly, end user must account for this in their final layout. Microsemi makes no warranty or representation of performance based on this recommended land pattern.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1(949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.