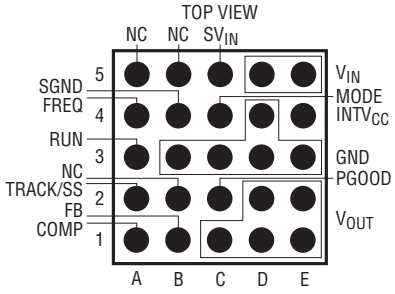
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SV_{IN} ..... –0.3V to 15V
V_{OUT} (Note 4) .....–0.3V to SV_{IN} or 6V
RUN .....–0.3V to $15V_{IN}$
$INTV_{CC}$ ..... –0.3V to 3.6V
PGOOD, MODE, TRACK/SS, FREQ .....–0.3V to $INTV_{CC}$
COMP, FB (Note 4) .....–0.3V to $INTV_{CC}$
Internal Operating Junction Temperature Range
(Notes 2, 5) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 245°C

PIN CONFIGURATION

(See Pin Functions, Pin Configuration Table)



BGA PACKAGE
25-LEAD (6.25mm × 6.25mm × 5.01mm)

T_{JMAX} = 125°C, θ_{JCtop} = 17°C/W, $\theta_{JCbottom}$ = 11°C/W,
$\theta_{JB} + \theta_{BA}$ = 22°C/W, θ_{JA} = 22°C/W,
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS
θ VALUES DETERMINED PER JESD51-12, WEIGHT = 0.5g

ORDER INFORMATION

http://www.linear.com/product/LTM4624#orderinfo

PART NUMBER	PAD OR BALL FINISH	PART MARKING* DEVICE	PART MARKING* FINISH CODE	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (See Note 2)
LTM4624EY#PBF	SAC305 (RoHS)	LTM4624Y	e1	BGA	3	–40°C to 125°C
LTM4624IY#PBF	SAC305 (RoHS)	LTM4624Y	e1	BGA	3	–40°C to 125°C
LTM4624IY	SnPb (63/37)	LTM4624Y	e0	BGA	3	–40°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Markings:
  www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures:
  www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings:
  www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = SV_{IN} = 12V per the typical application shown on the front page.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Section: per Channel							
V_{IN}	Input DC Voltage	SV_{IN} = V_{IN}	●	4		14	V
$V_{OUT(RANGE)}$	Output Voltage Range		●	0.6		5.5	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF, C_{OUT} = 100µF Ceramic, R_{FB} = 40.2k, MODE = $INTV_{CC}$, V_{IN} = 4V to 14V, I_{OUT} = 0A to 4A (Note 3) 0°C to 125°C –40°C to 125°C	 ●	 1.477 1.47	 1.50 1.50	 1.523 1.53	 V V
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising		1.1	1.2	1.3	V
$I_{Q(SVIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, MODE = $INTV_{CC}$ V_{IN} = 12V, V_{OUT} = 1.5V, MODE = GND Shutdown, RUN = 0, V_{IN} = 12V			6 2 11		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 4A			0.62		A
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V		0		4	A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = SV_{IN} = 12V per the typical application shown on the front page.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔV_{OUT} (Line)/V_{OUT}	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} = 4V to 14V, I_{OUT} = 0A	●		0.04	0.15	%/V
ΔV_{OUT} (Load)/V_{OUT}	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 4A	●		1	1.5	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			5		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			30		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF Ceramic, No Load, TRACK/SS = 0.01µF, V_{IN} = 12V, V_{OUT} = 1.5V			2.5		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			160		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 47µF Ceramic, V_{IN} = 12V, V_{OUT} = 1.5V			40		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V		5	7		A
V_{FB}	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V I_{OUT} = 0A, V_{OUT} = 1.5V, –40°C to 125°C	 ●	0.594 0.591	0.60 0.60	0.606 0.609	V V
I_{FB}	Current at FB Pin	(Note 4)				±30	nA
R_{FBHI}	Resistor Between V_{OUT} and FB Pins			60.05	60.40	60.75	kΩ
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V			2.5	4	µA
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout	V_{IN} Falling V_{IN} Hysteresis		2.4	2.6 350	2.8	V mV
$t_{ON(MIN)}$	Minimum On-Time	(Note 4)			40		ns
$t_{OFF(MIN)}$	Minimum Off-Time	(Note 4)			70		ns
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive		 –13 7	 –10 10	 –7 13	 % %
I_{PGOOD}	PGOOD Leakage					2	µA
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 1mA			0.02	0.1	V
V_{INTVCC}	Internal V_{CC} Voltage	SV_{IN} = 4V to 14V		3.2	3.3	3.4	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA			0.5		%
f_{OSC}	Oscillator Frequency				1		MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4624 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4624E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4624I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

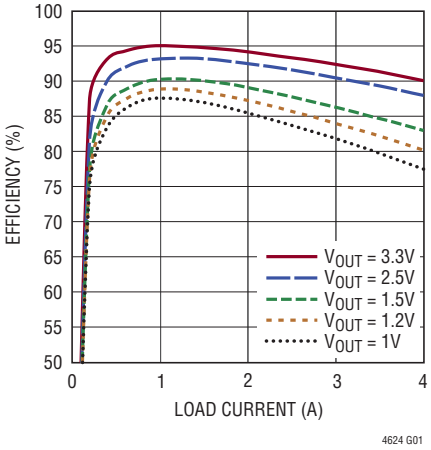
Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

Note 4: 100% tested at wafer level.

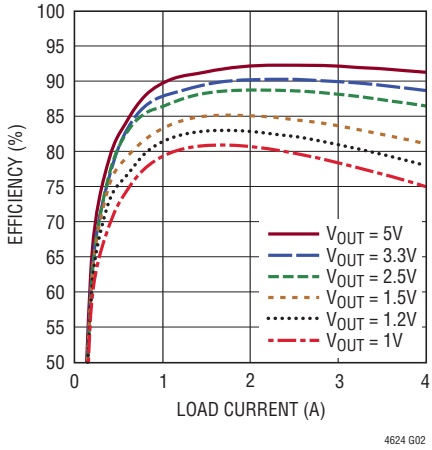
Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

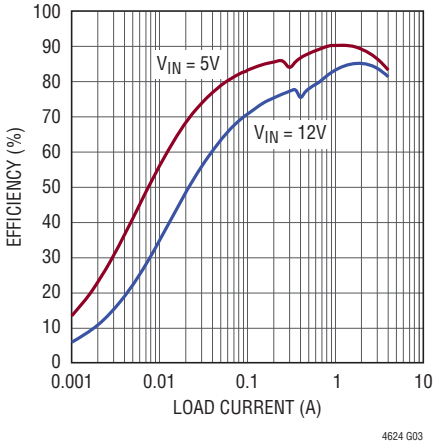
Efficiency vs Load Current with $5V_{IN}$



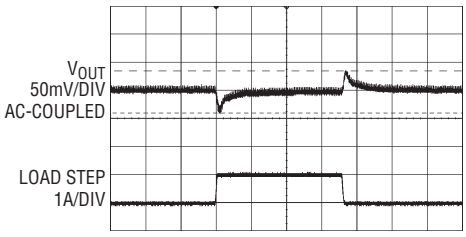
Efficiency vs Load Current with $12V_{IN}$



DCM Mode Efficiency, $V_{OUT} = 1.5V$

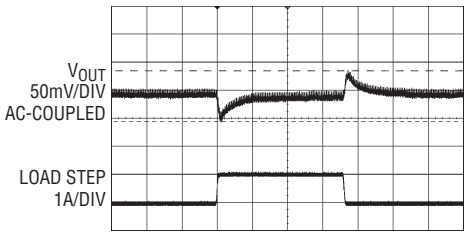


1V Output Transient Response



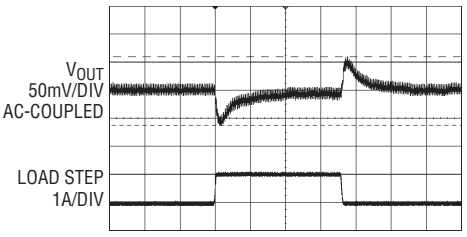
V_{IN} = 12V 20µs/DIV
V_{OUT} = 1V
I_{OUT} = 3A TO 4A, 1A/µs
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

1.5V Output Transient Response



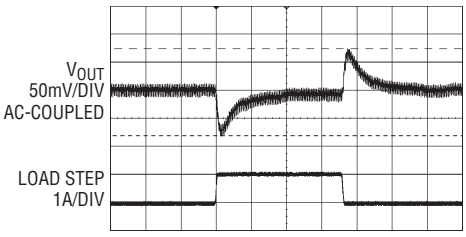
V_{IN} = 12V 20µs/DIV
V_{OUT} = 1.5V
I_{OUT} = 3A TO 4A, 1A/µs
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

2.5V Output Transient Response



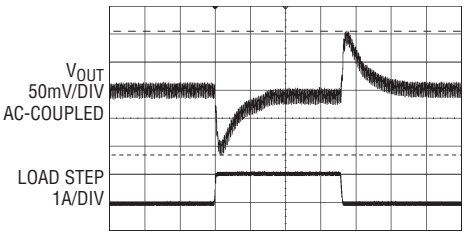
V_{IN} = 12V 20µs/DIV
V_{OUT} = 2.5V
I_{OUT} = 3A TO 4A, 1A/µs
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

3.3V Output Transient Response



V_{IN} = 12V 20µs/DIV
V_{OUT} = 3.3V
I_{OUT} = 3A TO 4A, 1A/µs
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

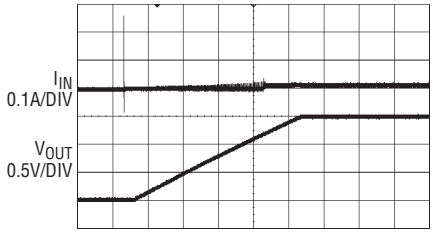
5V Output Transient Response



V_{IN} = 12V 20µs/DIV
V_{OUT} = 5V
I_{OUT} = 3A TO 4A, 1A/µs
OUTPUT CAPACITOR = 1 × 47µF CERAMIC

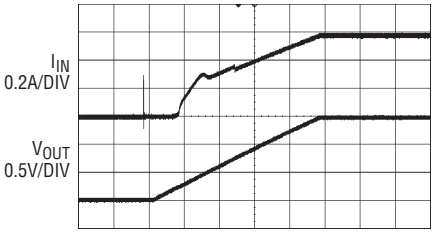
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up with No Load



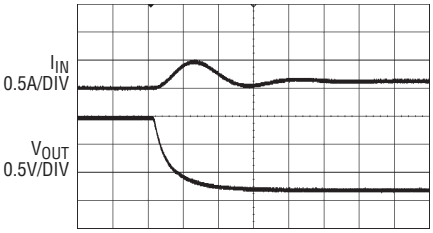
V_{OUT} = 1.5V
INPUT CAPACITOR = 150µF SANYO ELECTROLYTIC CAPACITOR (OPTIONAL) + 22µF CERAMIC CAPACITOR
OUTPUT CAPACITOR = 47µF CERAMIC CAPACITOR
SOFT-START CAPACITOR = 0.1µF

Start-Up with 4A Load



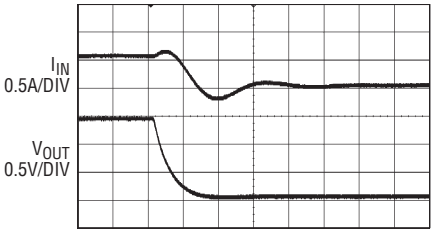
V_{OUT} = 1.5V
INPUT CAPACITOR = 150µF SANYO ELECTROLYTIC CAPACITOR (OPTIONAL) + 22µF CERAMIC CAPACITOR
OUTPUT CAPACITOR = 47µF CERAMIC CAPACITOR
SOFT-START CAPACITOR = 0.1µF

Short-Circuit with No Load



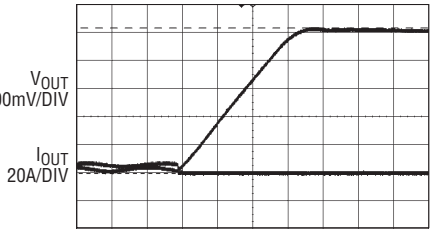
V_{OUT} = 1.5V
INPUT CAPACITOR = 150µF SANYO ELECTROLYTIC CAPACITOR (OPTIONAL) + 22µF CERAMIC CAPACITOR
OUTPUT CAPACITOR = 47µF CERAMIC CAPACITOR

Short-Circuit with 4A Load



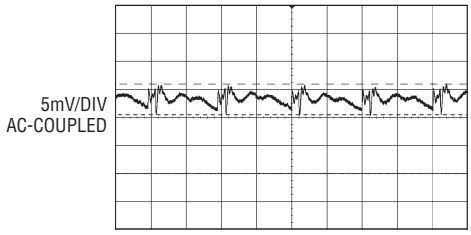
V_{OUT} = 1.5V
INPUT CAPACITOR = 150µF SANYO ELECTROLYTIC CAPACITOR (OPTIONAL) + 22µF CERAMIC CAPACITOR
OUTPUT CAPACITOR = 47µF CERAMIC CAPACITOR

Recovery to No Load from Short Circuit



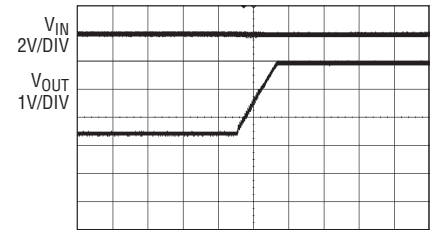
V_{OUT} = 1V
INPUT CAPACITOR = 22µF SANYO ELECTROLYTIC CAPACITOR (OPTIONAL) + 2× 22µF CERAMIC CAPACITOR
OUTPUT CAPACITOR = 2× 47µF CERAMIC CAPACITOR
SOFT-START CAPACITOR = 0.1µF

Output Ripple



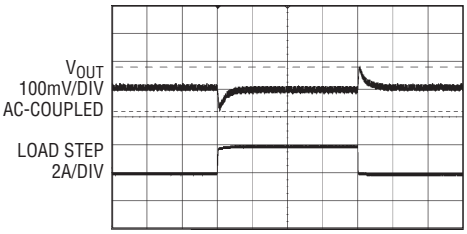
V_{OUT} = 1.5V
INPUT CAPACITOR = 22µF SANYO ELECTROLYTIC CAPACITOR (OPTIONAL) + 2× 22µF CERAMIC CAPACITOR
OUTPUT CAPACITOR = 2× 47µF CERAMIC CAPACITOR
SOFT-START CAPACITOR = 0.1µF

Start Into Pre-Bias Output



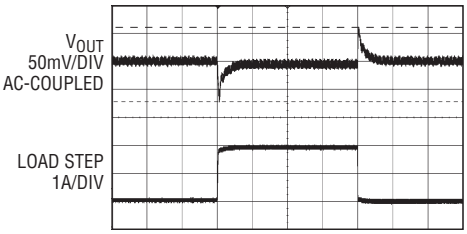
V_{OUT} = 5V
INPUT CAPACITOR = 22µF SANYO ELECTROLYTIC CAPACITOR (OPTIONAL) + 2× 22µF CERAMIC CAPACITOR
OUTPUT CAPACITOR = 2× 47µF CERAMIC CAPACITOR
SOFT-START CAPACITOR = 0.1µF

12V Input to 1.8V Output, 50% Load Transient Response



V_{OUT} = 1.8V
I_{OUT} = 2A TO 4A, 1A/µs
OUTPUT CAPACITOR = 1× 47µF CERAMIC

5V Input to 1.2V Output, 50% Load Transient Response



V_{OUT} = 1.2V
I_{OUT} = 2A TO 4A, 1A/µs
OUTPUT CAPACITOR = 1× 47µF CERAMIC

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

COMP (A1): Current Control Threshold and Error Amplifier Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.8V. Tie the COMP pins together for parallel operation. The device is internally compensated.

TRACK/SS (A2): Output Tracking and Soft-Start Input. Allows the user to control the rise time of the output voltage. Putting a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier, and servos the FB pin to match the TRACK/SS voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. There's an internal 2.5µA pull-up current from $INTV_{CC}$ on this pin, so putting a capacitor here provides a soft-start function.

RUN (A3): Run Control Input of the Switching Mode Regulator. Enables chip operation by tying RUN above 1.25V. Pulling it below 1.1V shuts down the part. Do not leave floating.

FREQ (A4): Frequency is set internally to 1MHz. An external resistor can be placed from this pin to SGND to increase frequency, or from this pin to $INTV_{CC}$ to reduce frequency. See the Applications Information section for frequency adjustment.

NC (A5, B2, B5): No Connect Pins. Pins are not connected internally. Float or ground these pins.

FB (B1): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between the FB and SGND pins. Tying the FB pins together allows for parallel operation. See the Applications Information section for details.

GND (B3, C3, D3-D4, E3): Power Ground Pins for Both Input and Output Returns.

SGND (B4): Signal Ground Connection. Tie to GND with minimum distance. Connect FREQ resistor, COMP component, MODE, TRACK/SS component, FB resistor to this pin as needed.

V_{OUT} (C1, D1-D2, E1-E2): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins.

PGOOD (C2): Output Power Good with Open-Drain Logic. PGOOD is pulled to ground when the voltage on the FB pin is not within ±10% of the internal 0.6V reference.

MODE (C4): Operation Mode Select. Tie this pin to $INTV_{CC}$ to force continuous synchronous operation at all output loads. Tying it to SGND enables discontinuous mode operation at light loads. Do not leave floating.

SV_{IN} (C5): Signal V_{IN}. Filtered input voltage to the on-chip 3.3V regulator. Tie this pin to the V_{IN} pin in most applications. Connect SV_{IN} to an external voltage supply of at least 4V which must also be greater than V_{OUT}.

V_{IN} (D5, E5): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

$INTV_{CC}$ (E4): Internal 3.3V Regulator Output. The internal power drivers and control circuits are powered from this voltage. This pin is internally decoupled to GND with a 1µF low ESR ceramic capacitor.

BLOCK DIAGRAM

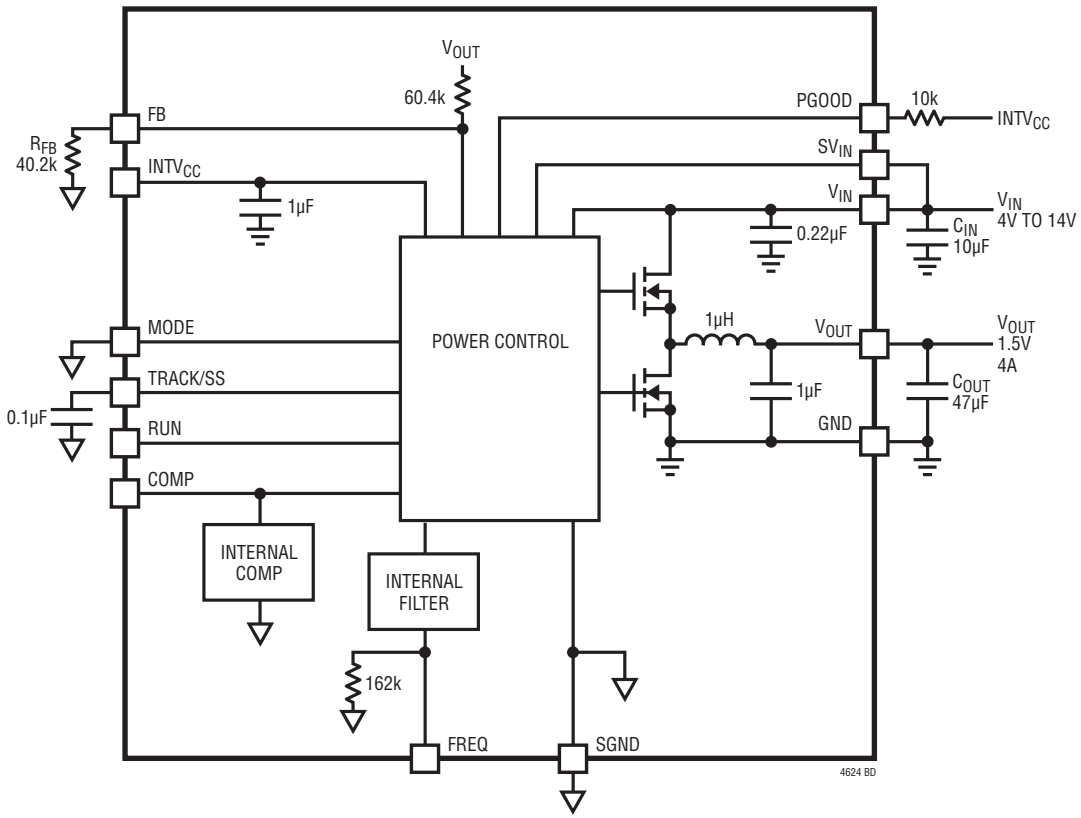


Figure 1. Simplified LTM4624 Block Diagram

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4V to 14V, V_{OUT} = 1.5V)	I_{OUT} = 4A	4.7	10		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4V to 14V, V_{OUT} = 1.5V)	I_{OUT} = 4A	22	47		µF

OPERATION

The LTM4624 is a standalone nonisolated switch mode DC/DC power supply. It can deliver up to 4A DC (5A peak) output current with few external input and output capacitors. This module provides precisely regulated output voltage adjustable between 0.6V to 5.5V via one external resistor over a 4V to 14V input voltage range. With an external bias supply, this module operates with an input voltage down to 2.375V. The typical application schematic is shown in Figure 20.

The LTM4624 contains an integrated constant on-time valley current mode regulator, power MOSFETs, inductor, and other supporting discrete components. The default switching frequency is 1MHz. For noise-sensitive applications, the switching frequency can be adjusted by external resistors. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4624 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limiting. Foldback current limiting is provided in an overcurrent condition indicated by a drop in V_{FB} reducing inductor valley current to approximately 40% of the original value. Internal output overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Continuous operation is forced during OV and UV conditions except during start-up when the TRACK pin is ramping up to 0.6V

Pulling the RUN pin below 1.1V forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, discontinuous mode (DCM) operation can be enabled to achieve higher efficiency compared to continuous mode (CCM) by pulling the MODE pin to SGND. The TRACK/SS pin is used for power supply tracking and soft-start programming. See the Applications Information section.

APPLICATIONS INFORMATION

The typical LTM4624 application circuit is shown in Figure 20. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. Refer to Table 6 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratios that can be achieved for a given input voltage due to the minimum off-time and minimum on-time limits of the regulator. The minimum off-time limit imposes a maximum duty cycle which can be calculated as:

$$D_{MAX} = 1 - (t_{OFF(MIN)} \bullet f_{SW})$$

where $t_{OFF(MIN)}$ is the minimum off-time, typically 70ns for LTM4624, and f_{SW} (Hz) is the switching frequency. Conversely the minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated as:

$$D_{MIN} = t_{ON(MIN)} \bullet f_{SW}$$

where $t_{ON(MIN)}$ is the minimum on-time, typically 40ns for LTM4624. In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. Note that additional thermal derating may be applied. See the Thermal Considerations and Output Current Derating section in this data sheet.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects the V_{OUT} and FB pins together. Adding a resistor, R_{FB}, from FB pin to SGND programs the output voltage:

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \bullet 60.4k$$

Table 1. R_{FB} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
R_{FB} (kΩ)	OPEN	90.9	60.4	40.2	30.1	19.1	13.3	8.25

Input Decoupling Capacitors

The LTM4624 module should be connected to a low AC impedance DC source. For the regulator, a 10µF input ceramic capacitor is required for RMS ripple current decoupling. Bulk input capacitance is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an aluminum electrolytic capacitor or polymer capacitor.

Without considering the inductor ripple current, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

where $\eta\%$ is the estimated efficiency of the power module.

Output Decoupling Capacitors

With an optimized high frequency, high bandwidth design, only a single low ESR output ceramic capacitor is required for the LTM4624 to achieve low output ripple voltage and very good transient response. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 6 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 1A and 2A load-step transient. The Linear Technology LTpowerCAD® design tool is available to download online for output ripple, stability and transient response analysis for further optimization.

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Discontinuous Current Mode (DCM)

In applications where low output ripple and high efficiency at intermediate current are desired, discontinuous current mode (DCM) should be used by connecting the MODE pin to SGND. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode.

Forced Continuous Current Mode (CCM)

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE pin to $INTV_{CC}$. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4624's output voltage is in regulation.

Operating Frequency

The operating frequency of the LTM4624 is optimized to achieve the compact package size and the minimum output ripple voltage while still keeping high efficiency. The default operating frequency is internally set to 1MHz. In most applications, no additional frequency adjusting is required.

If any operating frequency other than 1MHz is required by application, the operating frequency can be increased by adding a resistor, R_{FSET}, between the FREQ pin and SGND, as shown in Figure 21. The operating frequency can be calculated as:

$$f(Hz) = \frac{1.6e11}{162k \,||\, R_{FSET}(\Omega)}$$

The operating frequency can also be decreased by adding a resistor between the FREQ pin and $INTV_{CC}$, calculated as:

$$f(Hz) = 1MHz - \frac{2.8e11}{R_{FSET}(\Omega)}$$

The programmable operating frequency range is from 800kHz to 4MHz.

Soft-Start And Output Voltage Tracking

The TRACK/SS pin provides a means to either soft start the regulator or track it to a different power supply. A capacitor on the TRACK/SS pin will program the ramp rate of the output voltage. An internal 2.5µA current source will charge up the external soft-start capacitor towards $INTV_{CC}$ voltage. When the TRACK/SS voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated as:

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{2.5\mu A}$$

where C_{SS} is the capacitance on the TRACK/SS pin. Current foldback and forced continuous mode are disabled during the soft-start process.

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Output voltage tracking can also be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. Figure 2 and Figure 3 show an example waveform and schematic of ratiometric tracking where the slave regulator's output slew rate is proportional to the master's.

Since the slave regulator's TRACK/SS is connected to the master's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the slave output voltage when TRACK/SS voltage is below 0.6V, the slave

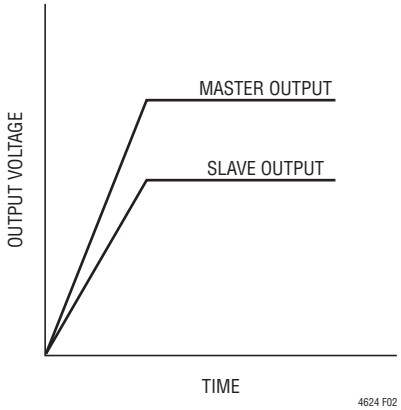

Figure 2. Output Ratiometric Tracking Waveform

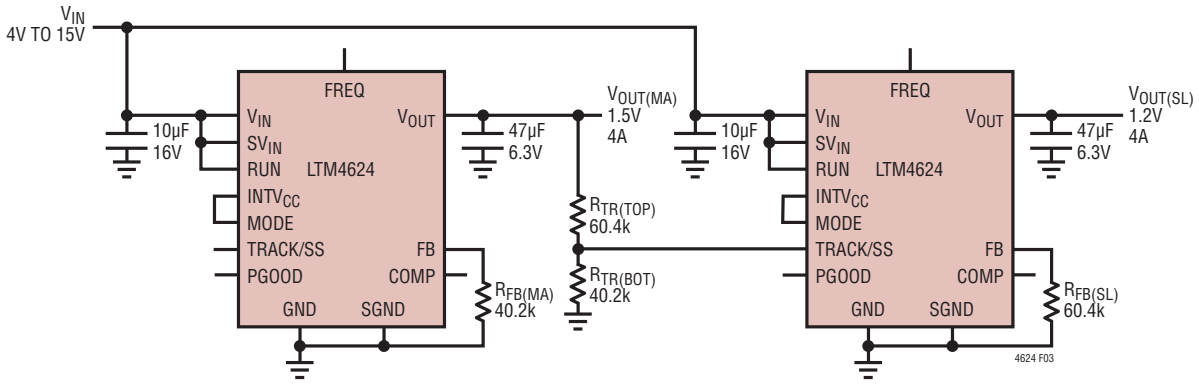

Figure 3. Example Schematic of Ratiometric Output Voltage Tracking

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output voltage and the master output voltage should satisfy the following equation during start-up:

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

The $R_{FB(SL)}$ is the feedback resistor and the $R_{TR(TOP)}$/$R_{TR(BOT)}$ is the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 3.

Following the previous equation, the ratio of the master's output slew rate (MR) to the slave's output slew rate (SR) is determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

For example, $V_{OUT(MA)}$=1.5V, MR = 1.5V/1ms and $V_{OUT(SL)}$ = 1.2V, SR = 1.2V/1ms as shown in Figure 5. From the equation, we could solve that $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 40.2k are a good combination for the ratiometric tracking.

The TRACK/SS pin will have the 2.5µA current source on when a resistive divider is used to implement tracking on the slave regulator. This will impose an offset on the TRACK/SS pin input. Smaller value resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK/SS pin offset to a negligible value.

The coincident output tracking can be recognized as a special ratiometric output tracking in which the master's output slew rate (MR) is the same as the slave's output slew rate (SR), waveform as shown in Figure 4.

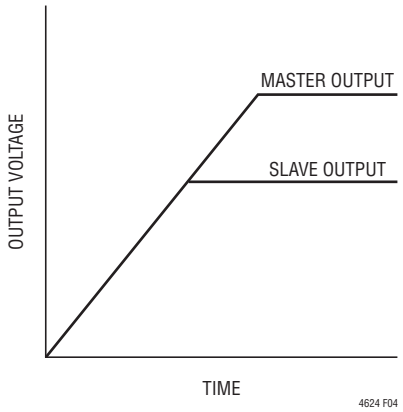

Figure 4. Output Coincident Tracking Waveform

From the equation, we could easily find that, in coincident tracking, the slave regulator's TRACK/SS pin resistor divider is always the same as its feedback divider:

$$\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

For example, $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 60.4k is a good combination for coincident tracking for a $V_{OUT(MA)}$ = 1.5V and $V_{OUT(SL)}$ = 1.2V application.

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin is pulled low when the output voltage exceeds a ±10% window around the regulation point. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTM4624's PGOOD falling edge includes a blanking delay of approximately 52 switching cycles.

Stability Compensation

The LTM4624's internal compensation loop is designed and optimized for use with low ESR ceramic output capacitors. Table 5 is provided for most application requirements. In case a bulk output capacitor is required for output ripple or dynamic transient spike reduction, an additional 10pF to 15pF feedforward capacitor (C_{FF}) is needed between the V_{OUT} and FB pins. The LTpowerCAD design tool is available for control loop optimization.

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RUN Enable

Pulling the RUN pin to ground forces the LTM4624 into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.7V turns on the internal reference only, while still keeping the power MOSFETs off. Increasing the RUN pin voltage above 1.25V will turn on the entire chip.

Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with some charge on the output capacitors. The LTM4624 can safely power up into a pre-biased output without discharging it.

The LTM4624 accomplishes this by forcing discontinuous mode (DCM) operation until the TRACK/SS pin voltage reaches 0.6V reference voltage. This will prevent the BG from turning on during the pre-biased output start-up which would discharge the output.

Do not pre-bias LTM4624 with an output voltage above $INTV_{CC}$ voltage (3.3V) or set voltage by FB resistor whichever is lower.

Overtemperature Protection

The internal overtemperature protection monitors the junction temperature of the module. If the junction temperature reaches approximately 160°C, both power switches will be turned off until the temperature drops about 15°C cooler.

Low Input Application

The LTM4624 module has a separate SV_{IN} pin which makes it suitable for low input voltage applications down to 2.375V. The SV_{IN} pin is the single input of the whole control circuitry while the V_{IN} pin is the power input which directly connects to the drain of the top MOSFET. In most applications where V_{IN} is greater than 4V, connect SV_{IN} directly to V_{IN} with a short trace. An optional filter, consisting of a resistor (1Ω to 10Ω) between SV_{IN} and V_{IN} along with a 0.1µF bypass capacitor between SV_{IN} and ground, can be placed for additional noise immunity. This filter is not necessary in most cases if good PCB layout practices are followed (see Figure 19). In a low input voltage (2.375V to 4V) application, or to reduce power dissipation by the internal bias LDO, connect SV_{IN} to an external voltage higher than 4V with a 0.1µF local bypass capacitor. Figure 21 shows an example of a low input voltage application. Please note the SV_{IN} voltage cannot go below the V_{OUT} voltage.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD 51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients is found in JESD 51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with four layers.

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2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match the user's application.

3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule package and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 5; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within the LTM4624 be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled environment chamber to reasonably define and correlate the thermal resistance

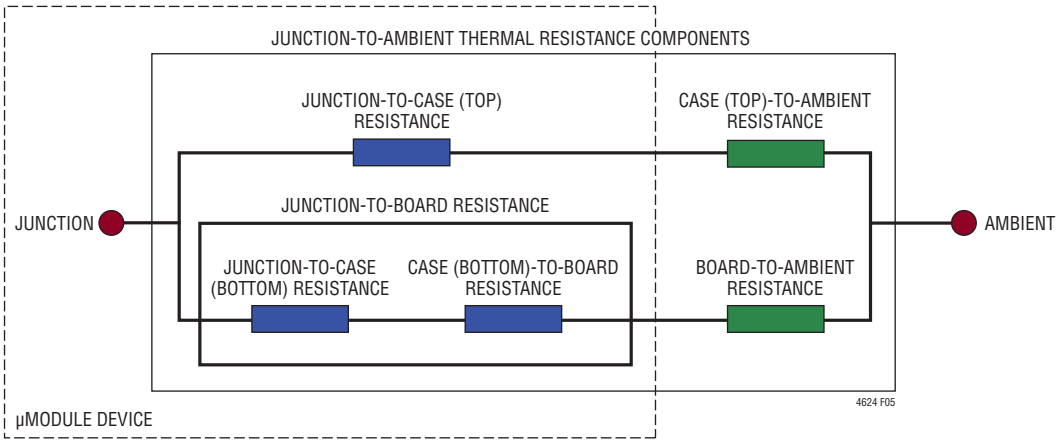

Figure 5. Graphical Representation of JESD 51-12 Thermal Coefficients

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values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4624 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JSED 51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4624 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due diligence yields the set of derating curves shown in this data sheet. After these laboratory tests have been performed and correlated to the LTM4624 model, then the θ_{JB} and θ_{BA} are summed together to provide a value that should closely equal the θ_{JA} value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 1.0V, 1.5V, 3.3V and 5V power loss curves in Figures 6 to 9 can be used in coordination with the load current derating curves in Figures 10 to 16 for calculating an approximate θ_{JA} thermal resistance for the LTM4624 with various airflow conditions. The power loss curves are taken at room temperature, and are increased with a multiplicative factor according to the ambient temperature. This approximate factor is: 1.4 for 120°C at junction temperature. Maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 120°C, which is a 5°C guard band from maximum junction temperature of 125°C. When the ambient temperature reaches a point where the junction temperature is 120°C, then the load current is lowered to maintain the junction at 120°C while increasing ambient temperature up to 120°C. The derating curves are plotted with the output current starting at 4A and the ambient temperature at 30°C. The output voltages are 1.0V, 1.5V, 3.3V and 5V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 11 the load current is derated to ~3A at ~95°C with no air flow or heat sink and the power loss for the 12V to 1.0V at 3A output is about 1.15W. The 1.15W loss is calculated with the ~0.82W room temperature loss from the 12V to 1.0V power loss curve at 3A, and the 1.4 multiplying factor at 120°C junction temperature. If the 95°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 25°C divided by 1.15W equals a 22°C/W θ_{JA} thermal resistance. Table 2 specifies a 22°C/W value which is very close. Table 3, Table 4 and Table 5 provide equivalent thermal resistances for 1.5V 3.3V and 5V outputs with and without airflow and heat sinking. The derived thermal resistances in Table 3, Table 4 and Table 5 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick 4-layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

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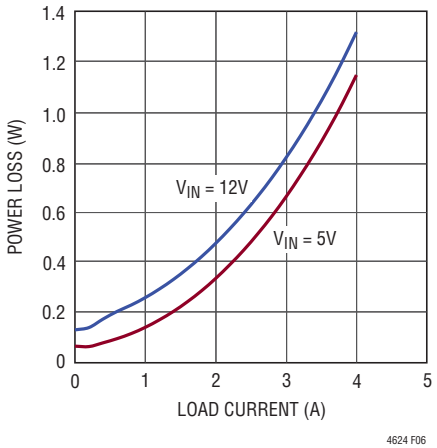

Figure 6. 1.0V Loss

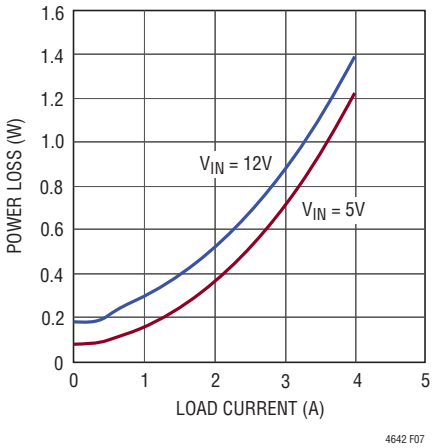

Figure 7. 1.5V Loss

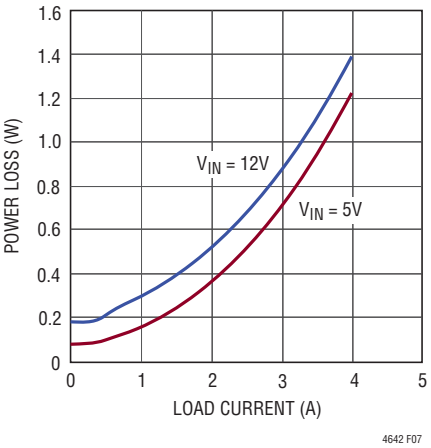

Figure 8. 3.3V Loss

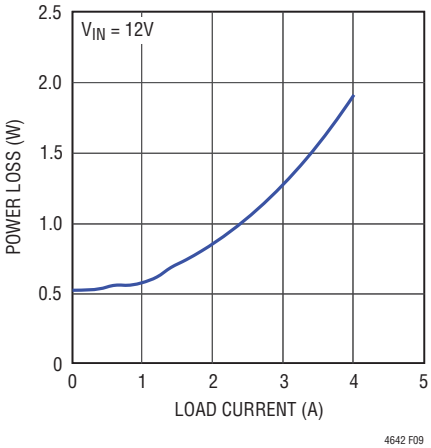

Figure 9. 5V Loss

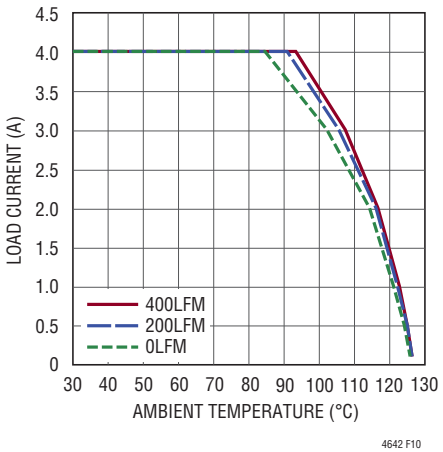

Figure 10. 5V to 1V Derating Curve, No Heat Sink

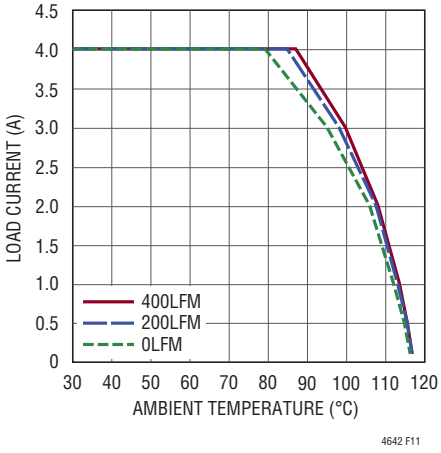

Figure 11. 12V to 1V Derating Curve, No Heat Sink

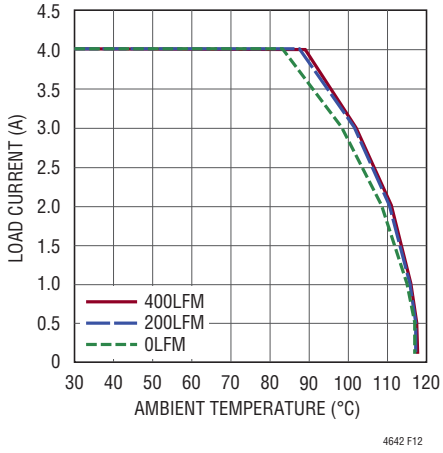

Figure 12. 5V to 1.5V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

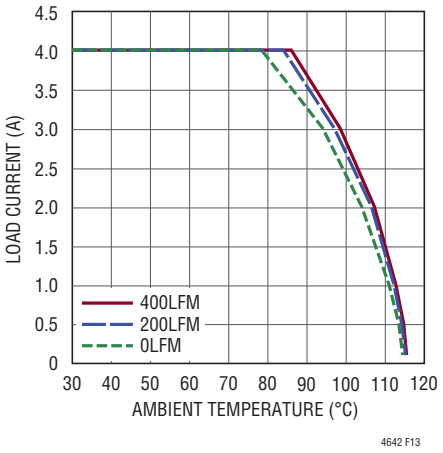

Figure 13. 12V to 1.5V Derating Curve, No Heat Sink

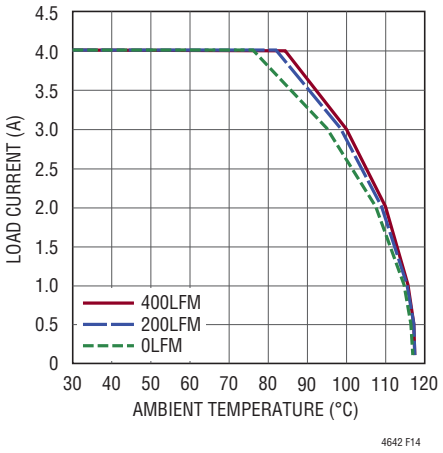

Figure 14. 5V to 3.3V Derating Curve, No Heat Sink

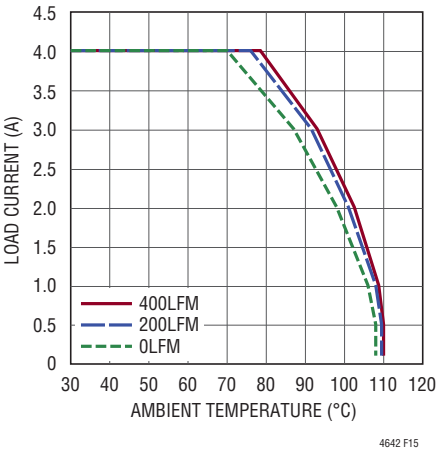

Figure 15. 12V to 3.3V Derating Curve, No Heat Sink

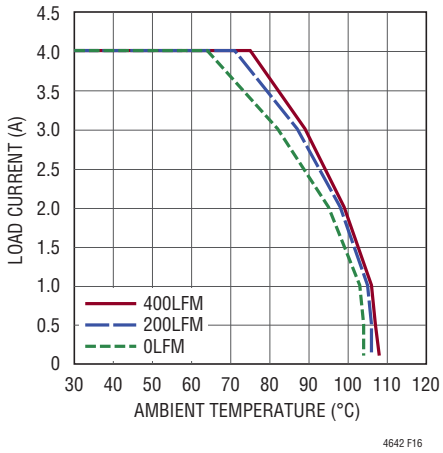

Figure 16. 12V to 5V Derating Curve, No Heat Sink

Table 2. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figures 10, 11	5, 12	Figure 6	0	None	22
Figures 10, 11	5, 12	Figure 6	200	None	19
Figures 10, 11	5, 12	Figure 6	400	None	18

Table 3. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figures 12, 13	5, 12	Figure 7	0	None	22
Figures 12, 13	5, 12	Figure 7	200	None	19
Figures 12, 13	5, 12	Figure 7	400	None	18

Table 4. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figures 14, 15	5, 12	Figure 8	0	None	22
Figures 14, 15	5, 12	Figure 8	200	None	19
Figures 14, 15	5, 12	Figure 8	400	None	18

Table 5. 5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	$\theta_{JA(°C/W)}$
Figure 16	12	Figure 9	0	None	22
Figure 16	12	Figure 9	200	None	19
Figure 16	12	Figure 9	400	None	18

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Table 6. Output Voltage Response vs Component Matrix (Refer to Figure 20)

C_{IN}	PART NUMBER	VALUE	C_{OUT1}	PART NUMBER	VALUE	C_{OUT2}	PART NUMBER	VALUE
Murata	GRM21BR61C106KE15L	10µF, 16V, 0805, X5R	Murata	GRM21BR60J476ME15	47µF, 6.3V, 0805, X5R	Sanyo	4TPE100MZB	4V 100µF
Taiyo Yuden	EMK212BJ106KG-T	10µF, 16V, 0805, X5R	Taiyo Yuden	JMK212BJ476MG-T	47µF, 6.3V, 0805, X5R			
Murata	GRM31CR61C226ME15L	22µF, 16V, 1206, X5R						
Taiyo Yuden	EMK316BJ226ML-T	22µF, 16V, 1206, X5R						

V_{OUT} (V)	C_{IN} (CERAMIC) (µF)	C_{IN} (BULK)	C_{OUT1} (CERAMIC) (µF)	C_{OUT2} (BULK) (µF)	C_{FF} (pF)	V_{IN} (V)	DROOP (mV)	P-P DERIVATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	R_{FB} (kΩ)
1	10		47			5, 12	5	72	40	1	1	90.9
1	10			100	10	5, 12	5	60	40	1	1	90.9
1	10		47			5, 12	5	127	40	2	1	90.9
1	10			100	10	5, 12	5	90	40	2	1	90.9
1.2	10		47			5, 12	5	76	40	1	1	60.4
1.2	10			100	10	5, 12	5	65	40	1	1	60.4
1.2	10		47			5, 12	5	145	40	2	1	60.4
1.2	10			100	10	5, 12	5	103	40	2	1	60.4
1.5	10		47			5, 12	5	80	40	1	1	40.2
1.5	10			100	10	5, 12	5	70	40	1	1	40.2
1.5	10		47			5, 12	5	161	40	2	1	40.2
1.5	10			100	10	5, 12	5	115	40	2	1	40.2
1.8	10		47			5, 12	5	95	40	1	1	30.1
1.8	10			100	10	5, 12	5	80	40	1	1	30.1
1.8	10		47			5, 12	5	177	40	2	1	30.1
1.8	10			100	10	5, 12	5	128	40	2	1	30.1
2.5	10		47			5, 12	5	125	40	1	1	19.1
2.5	10			100	10	5, 12	5	100	50	1	1	19.1
2.5	10		47			5, 12	5	225	40	2	1	19.1
2.5	10			100	10	5, 12	5	161	50	2	1	19.1
3.3	10		47			5, 12	5	155	40	1	1	13.3
3.3	10			100	10	5, 12	5	122	60	1	1	13.3
3.3	10		47			5, 12	5	285	40	2	1	13.3
3.3	10			100	10	5, 12	5	198	60	2	1	13.3
5	10		47			5, 12	5	220	40	1	1	8.25
5	10		47			5, 12	5	420	40	2	1	8.25

APPLICATIONS INFORMATION

Safety Considerations

The LTM4624 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and over current protection.

Layout Checklist/Example

The high integration of LTM4624 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- Bring out test points on the signal pins for monitoring.

Figure 19 gives a good example of the recommended layout.

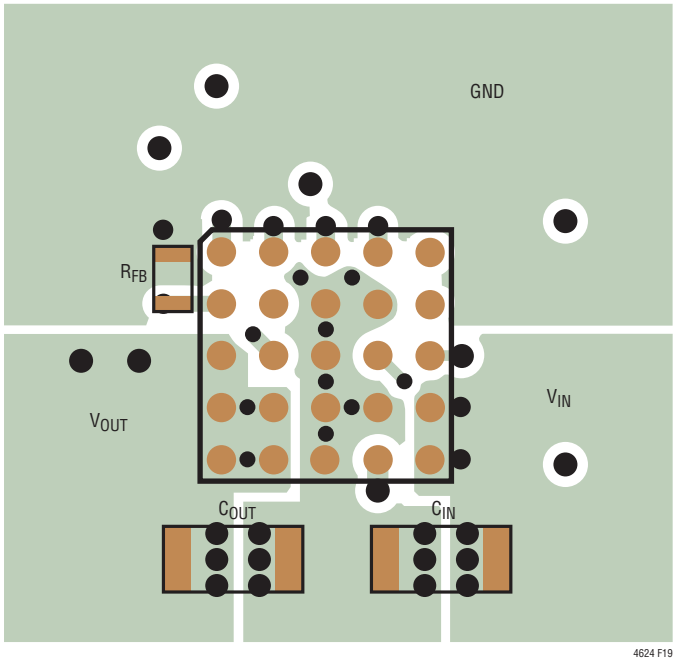


Figure 19. Recommended PCB Layout

APPLICATIONS INFORMATION

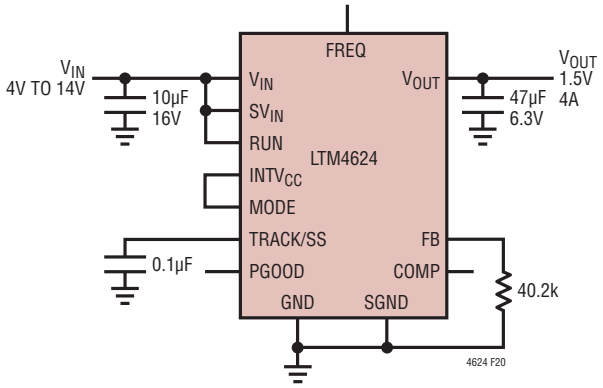


Figure 20. $4V_{IN}$ to $14V_{IN}$, 1.5V Output at 4A Design

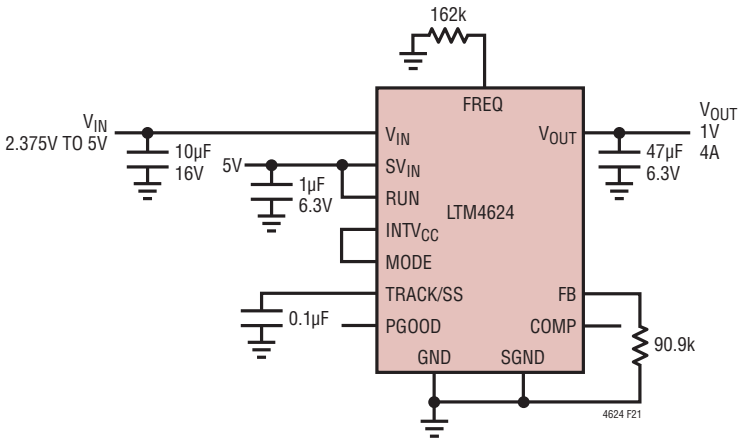


Figure 21. $2.375V_{IN}$ to $5V_{IN}$, 1V Output with 2MHz Operating Frequency

APPLICATIONS INFORMATION

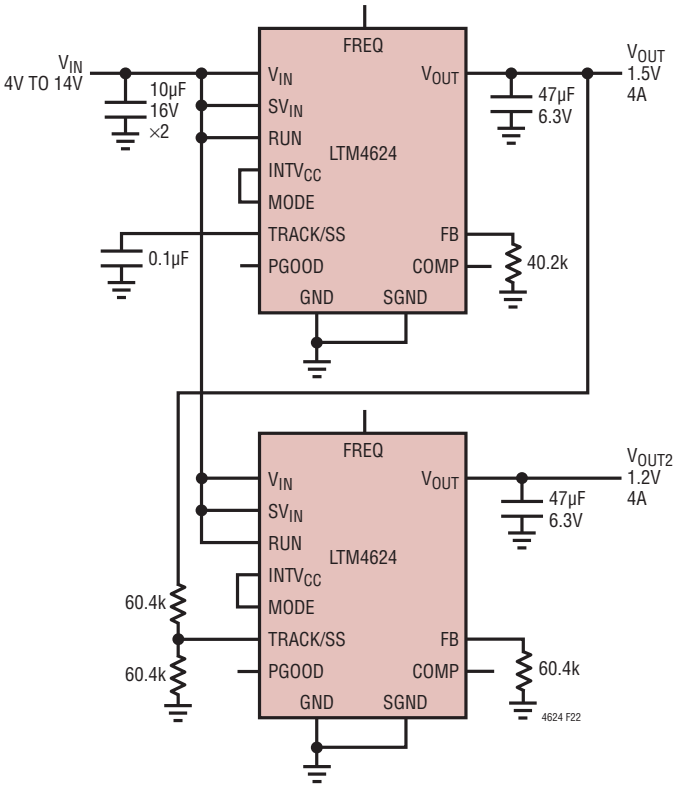


Figure 22. $4V_{IN}$ to $14V_{IN}$, 1.2V and 1.5V with Coincident Tracking

PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

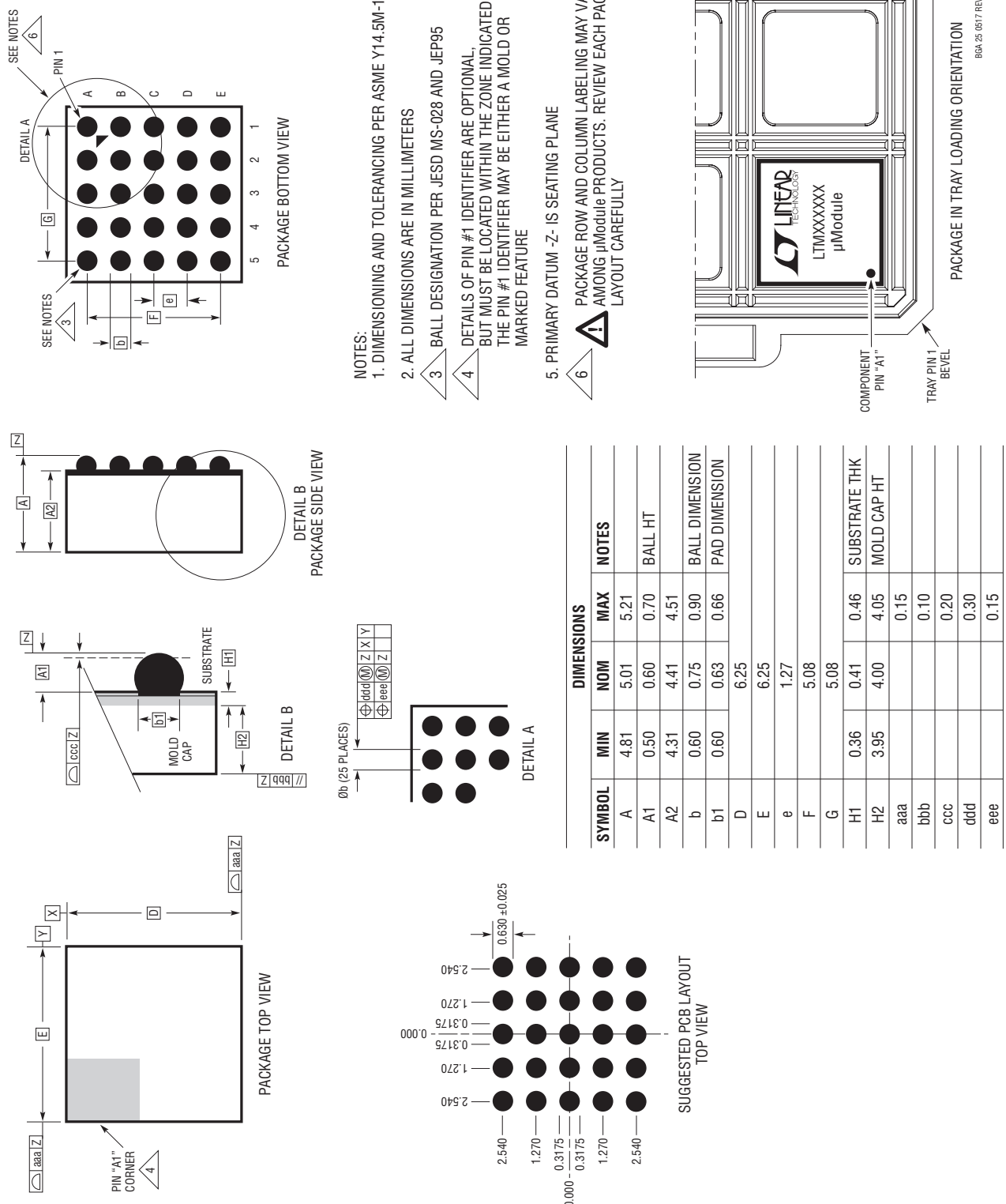
LTM4624 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	COMP	A2	TRACK/SS	A3	RUN	A4	FREQ	A5	NC
B1	FB	B2	NC	B3	GND	B4	SGND	B5	NC
C1	V_{OUT}	C2	PGOOD	C3	GND	C4	MODE	C5	SV_{IN}
D1	V_{OUT}	D2	V_{OUT}	D3	GND	D4	GND	D5	V_{IN}
E1	V_{OUT}	E2	V_{OUT}	E3	GND	E4	$INTV_{CC}$	E5	V_{IN}

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM4624#packaging for the most recent package drawings.

BGA Package
25-Lead (6.25mm × 6.25mm × 5.01mm)
(Reference LTC DWG # 05-08-1905 Rev C)



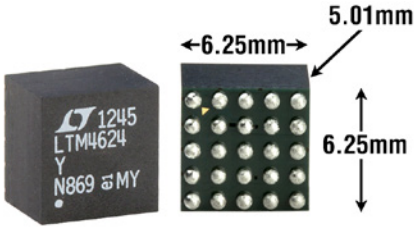
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.81	5.01	5.21	
A1	0.50	0.60	0.70	BALL HT
A2	4.31	4.41	4.51	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		6.25		
E		6.25		
e		1.27		
F		5.08		
G		5.08		
H1	0.36	0.41	0.46	SUBSTRATE THK
H2	3.95	4.00	4.05	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	

TOTAL NUMBER OF BALLS: 25

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	8/13	Update FREQ pin description	6
		Update output overvoltage protection description	8
B	2/14	Add SnPb BGA package option	1, 2
		Update RUN threshold	2
C	7/14	Add TechClip video hyperlink	1
		Update Absolute Maximum Ratings section	2
		Update Pre-Biased Output Start-Up section	13
D	7/17	RUN Abs Max Voltage Changed from SV_{IN} to 15V	2

PACKAGE PHOTO



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Search	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4619	Dual 26V, 4A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 26.5V$, $0.8V \le V_{OUT} \le 5V$, PLL Input, V_{OUT} Tracking, PGOOD, 15mm × 15mm × 2.82mm LGA
LTM4618	26V, 6A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 26.5V$, $0.8V \le V_{OUT} \le 5V$, PLL Input, V_{OUT} Tracking, 9mm × 15mm × 4.32mm LGA
LTM4628	Dual 26V, 8A Step-Down µModule Regulator	$4.5V \le V_{IN} \le 26.5V$, $0.6V \le V_{OUT} \le 5.5V$, Remote Sense Amplifier, Internal Temperature Sensing Output, 15mm × 15mm × 4.32mm LGA
LTM4614	Dual 5V, 4A µModule Regulator	$2.375V \le V_{IN} \le 5.5V$, $0.8V \le V_{OUT} \le 5V$, 15mm × 15mm × 2.82mm LGA
LTM4608A	5V, 8A Step-Down µModule Regulator with Tracking, Margining and Frequency Synchronization	$2.7V \le V_{IN} \le 5.5V$, $0.6V \le V_{OUT} \le 5V$, PLL input, Clock Output, V_{OUT} Tracking and Margining, PGOOD, 9mm × 15mm × 2.82mm LGA
LTM4616	Dual 5V, 8A Step-Down µModule Regulator with Tracking, Margining and Frequency Synchronization	$2.7V \le V_{IN} \le 5.5V$, $0.6V \le V_{OUT} \le 5V$, PLL input, Clock Output, V_{OUT} Tracking and Margining, PGOOD, 15mm × 15mm × 2.82mm LGA
LTM8045	Inverting or SEPIC µModule DC/DC Converter with Up to 700mA Output Current	$2.8V \le V_{IN} \le 18V$, $\pm 2.5V \le V_{OUT} \le \pm 15V$, Synchronizable, No Derating or Logic-Level Shift for Control Inputs when Inverting, 6.25mm × 11.25mm × 4.92mm BGA
LTC®2978	Octal Digital Power Supply Manager with EEPROM	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, 16-Bit ADC with ±0.25% TUE, 3.3V to 15V Operation
LTC2974	Quad Digital Power Supply Manager with EEPROM	I^2C/PMBus Interface, Configuration EEPROM, Fault Logging, Per Channel Voltage, Current and Temperature Measurements