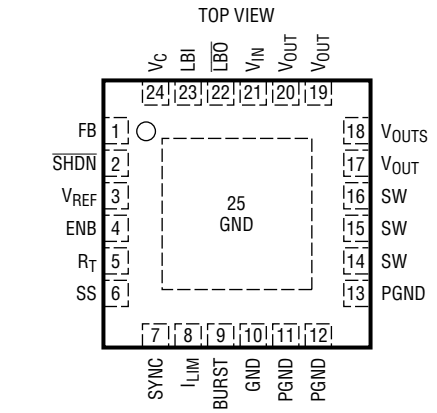
TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT}, V_{OUTS} Voltage ..... –0.3V to 6V
BURST, $\overline{SHDN}$, SS, ENB, SW,
$\overline{LBO}$, LBI, SYNC Voltages ..... –0.3V to 6V
Operating Temperature Range
(Notes 2, 5) ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 40°C/W 1 LAYER BOARD
θ_{JA} = 35°C/W 4 LAYER BOARD, θ_{JC} = 2.6°C/W
EXPOSED PAD IS GND (PIN 25) MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3421EUF#PBF	LTC3421EUF#TRPBF	3421	24-Lead Plastic QFN	–40°C to 85°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 1.2V, V_{OUT} = 3.3V, R_T = 28k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum V_{IN} Start-Up Voltage	I_{LOAD} < 1mA			0.88	1	V
Minimum V_{IN} Operating Voltage	(Note 4)	●			0.5	V
Output Voltage Adjust Range		 ●	2.25 2.40		5.25 5.25	V V
Feedback Voltage		●	1.196	1.220	1.244	V
Feedback Input Current	V_{FB} = 1.22V			1	50	nA
Quiescent Current—Burst Mode Operation	V_C = 0V, ENB = 0V (Note 3) V_C = 0V, ENB = 2V (Note 3)			12 23	20 50	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 1.2V, V_{OUT} = 3.3V, R_T = 28k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current—Shutdown	$\overline{SHDN}$ = 0V, ENB = 0V $\overline{SHDN}$ = 0V, ENB > 1.4V			0.1 0.2	1 2	µA µA
Quiescent Current—Active	(Note 3)			0.6	1.1	mA
NMOS Switch Leakage				0.1	5	µA
PMOS Switch Leakage				0.1	10	µA
NMOS Switch On Resistance				0.1		Ω
PMOS Switch On Resistance				0.14		Ω
NMOS Current Limit	I_{LIM} Resistor = 105k I_{LIM} Resistor = 36.5k	● ●	1 3	1.5 4.2		A A
Max Duty Cycle		●	84	91		%
Min Duty Cycle		●			0	%
Frequency Accuracy		●	0.85	1	1.15	MHz
SYNC Input High		●	2.2			V
SYNC Input Low		●			0.8	V
SYNC Input Current		●		0.01	1	µA
ENB Input High		●	1.2			V
ENB Input Low		●			0.4	V
ENB Input Current		●			1	µA
$\overline{SHDN}$ Input High	V_{OUT} = 0V (Initial Start-Up), ENB = 0V V_{OUT} > 2.4V, ENB = 0V		1.00 0.65			V V
$\overline{SHDN}$ Input Low					0.25	V
$\overline{SHDN}$ Input Current		●		0.01	1	µA
REF Output Voltage		●	1.183	1.22	1.257	V
REF Output Current Range			–100		8	µA
Error Amp Transconductance				45		µs
LBI Threshold	Falling Edge	●	0.58	0.6	0.62	V
LBI Input Current		●		0.01	1	µA
$\overline{LBO}$ Low Voltage	V_{IN} = 0V, I_{SINK} = 1mA V_{IN} = 0V, I_{SINK} = 20mA			12.0 0.25	50 0.5	mV V
$\overline{LBO}$ Leakage	$V_{\overline{LBO}}$ = 5.5V			0.01	1	µA
SS Current Source	V_{SS} = 1V		1.2	2.4	5	µA
BURST Threshold Voltage	Falling Edge		0.87	0.97	1.07	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3421E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the 40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

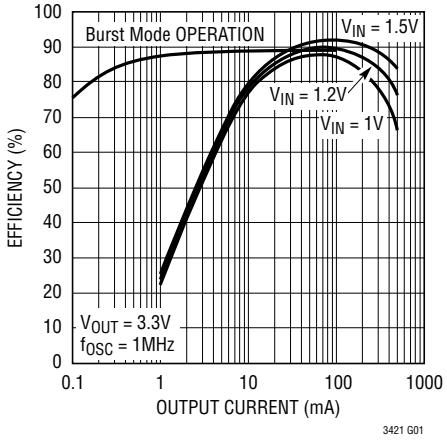
Note 3: Current is measured into the V_{OUTS} pin since the supply current is bootstrapped to the output. The current will reflect to the input supply by (V_{OUT}/V_{IN}) • Efficiency. The outputs are not switching.

Note 4: Once V_{OUT} is greater than 2.4V, the IC is not dependent on the V_{IN} supply.

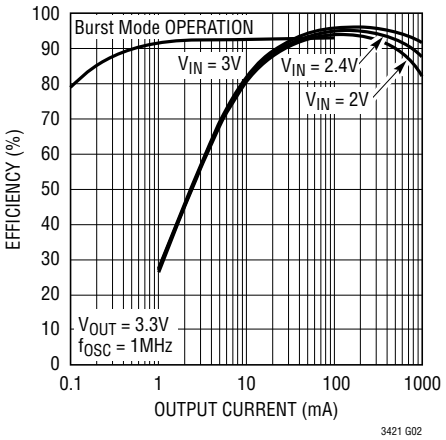
Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 85°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

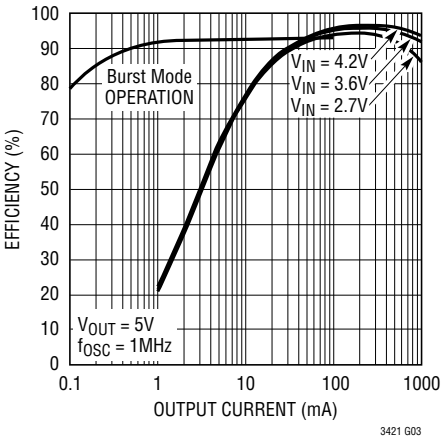
Single Cell to 3.3V Efficiency



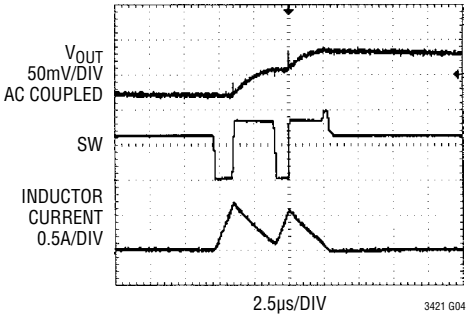
2-Cell to 3.3V Efficiency



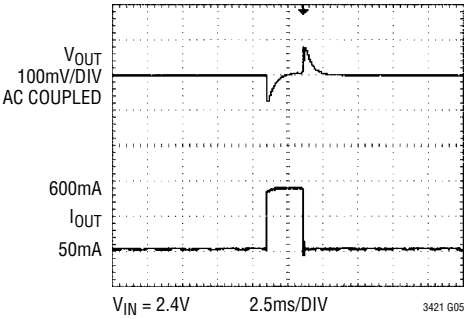
Li-Ion to 5V Efficiency



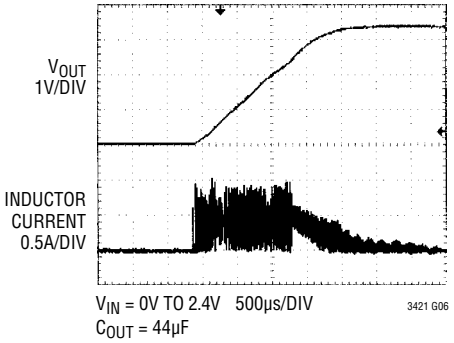
Burst Mode Operation



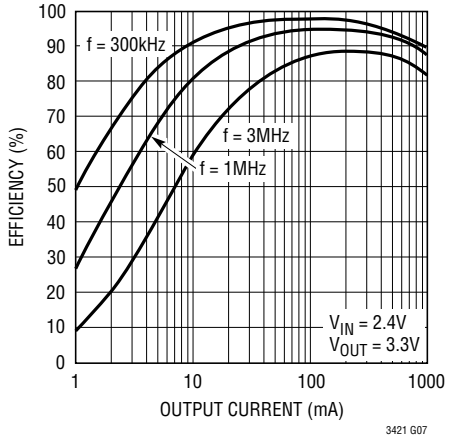
Load Transient Response



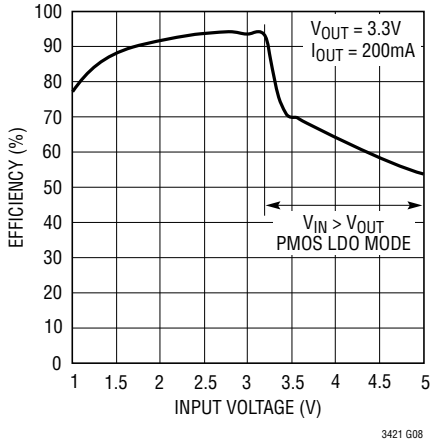
Inrush Current Control



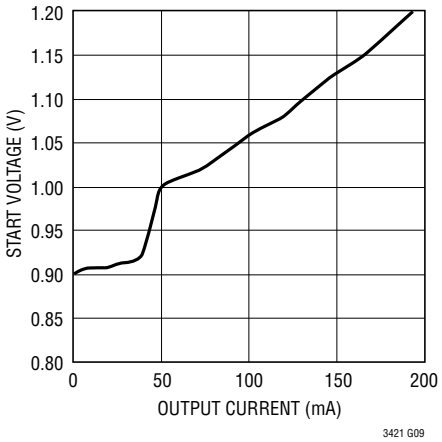
Efficiency vs Frequency



Efficiency vs V_{IN}

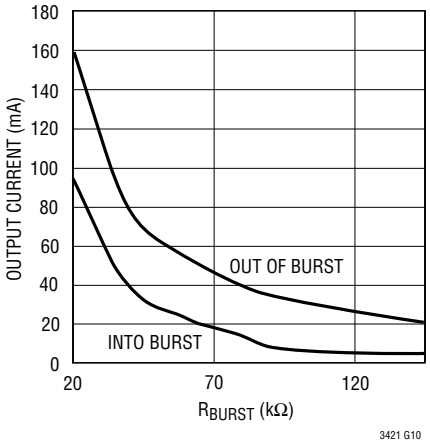


Start-Up Voltage vs Output Current

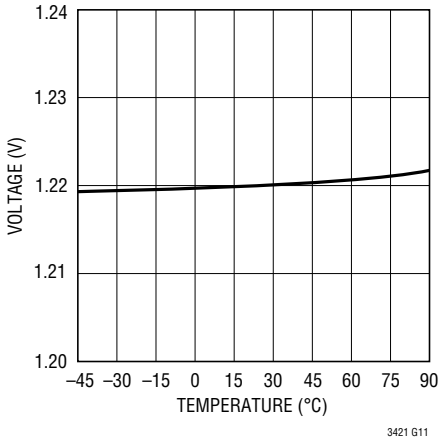


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

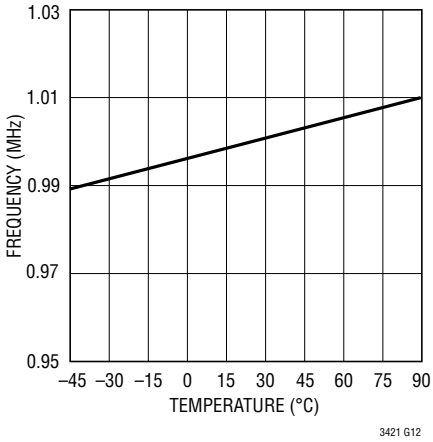
Burst Mode Threshold vs R_{BURST}



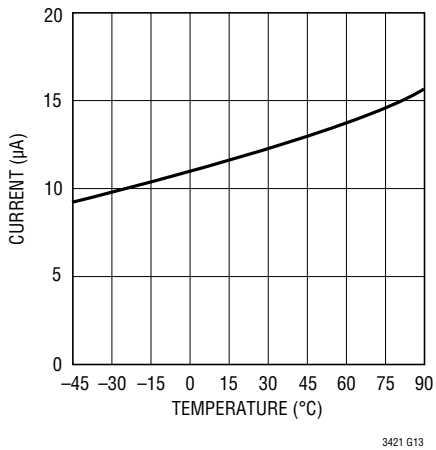
FB Voltage



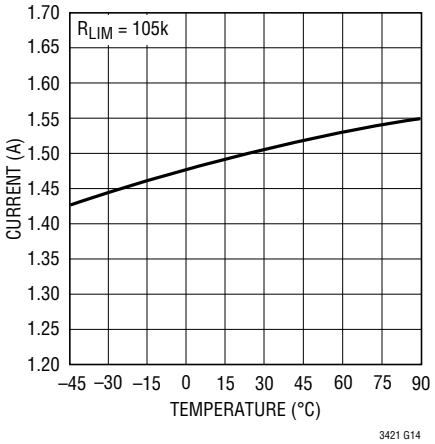
Frequency Accuracy



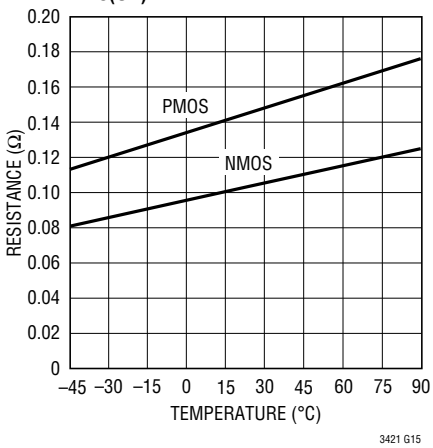
Burst Mode Quiescent Current



Current Limit Accuracy



$R_{DS(ON)}$



PIN FUNCTIONS

FB (Pin 1): Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 2.4V to 5.25V. The feedback reference voltage is typically 1.220V.

$\overline{SHDN}$ (Pin 2): Shutdown Pin. Less than 0.25V on this pin shuts down the IC. The IC is enabled when the $\overline{SHDN}$ voltage is greater than 1V. Once V_{OUT} is above 2.2V, hysteresis is applied to the pin (–500nA out of the pin) allowing it to operate at a logic high while the battery can drop to 0.5V.

V_{REF} (Pin 3): Buffered 1.22V Reference Output. This pin can source up to 100µA and sink up to 8µA. This pin must be decoupled with a 0.1µF capacitor for stability.

ENB (Pin 4): Reference Output (V_{REF}) Enable. When the converter is enabled ($\overline{SHDN}$ = High), forcing ENB = High enables the V_{REF} output, while forcing ENB = Low disables the V_{REF} output and lowers the quiescent current by 5µA. The low-battery comparator is always active when the converter is enabled. In shutdown, both the V_{REF} output and low-battery comparator are disabled unless both $V_{OUT} \geq 2.5V$ and ENB = High. Under these conditions, both the V_{REF} output and low-battery comparator are enabled.

PIN FUNCTIONS

R_T (Pin 5): Connect a resistor to ground to program the oscillator frequency according to the formula:

$$f_{OSC} = \frac{28,100}{R_T}$$

where f_{OSC} is in kHz and R_T is in kΩ.

SS (Pin 6): Soft-Start Pin. Connect a capacitor from this pin to ground to set the soft-start time according to the formula:

$$t(ms) = C_{SS}(\mu F) \bullet 320$$

The nominal soft-start charging current is 2.5µA. The active range of SS is from 0.8V to 1.6V.

SYNC (Pin 7): Oscillator Synchronization Pin. A clock pulse width of 100ns to 2µs is required to synchronize the internal oscillator. If not used SYNC should be grounded.

I_{LIM} (Pin 8): Current Limit Adjust Pin. Connect a resistor from this pin to ground to set the peak current limit threshold for the N-channel MOSFET according to the formula (note that this is the peak current in the inductor):

$$I_{LIM} = \frac{150}{R}$$

where I is in amps and R is in kΩ.

BURST (Pin 9): Burst Mode Threshold Adjust Pin. A resistor/capacitor combination from this pin to ground programs the average load current at which automatic Burst Mode operation is entered, according to the formula:

$$R_{BURST} = \frac{2}{I_{BURST}}$$

where R_{BURST} is in kΩ and I_{BURST} is in amps.

$$C_{BURST} \geq \frac{C_{OUT} \bullet V_{OUT}}{10,000}$$

where $C_{BURST(MIN)}$ and C_{OUT} are in µF.

For manual control of Burst Mode operation, ground the BURST pin to force Burst Mode operation or connect it to V_{OUT} to force fixed frequency PWM mode. Note that the BURST pin must not be pulled higher than V_{OUT}.

GND, Exposed Pad (Pins 10 and 25): Signal Ground Pin. Connect to ground plane near the RT resistor, error amp compensation components and feedback divider. The exposed pad must be soldered to the PCB and is typically connected through the power GND plane.

PGND (Pins 11 to 13): Source Terminal of Power Internal N-Channel MOSFET.

SW (Pins 14 to 16): Switch Pin for Inductor Connection. For applications where $V_{OUT} > 4.3V$, a Schottky diode from SW to V_{OUT} or to a snubber circuit is required to maintain absolute maximum rating for SW. (see Application Circuits for 5V).

V_{OUT} (Pins 17, 19 and 20): The output of the synchronous rectifier and bootstrapped power source for the IC. A ceramic bypass capacitor is required to be very close to the V_{OUT} and PGND pins of the IC.

V_{OUTS} (Pin 18): V_{OUT} Sense Pin. Connect V_{OUTS} directly to an output filter capacitor. The top of the feedback divider network should also be tied to this point.

V_{IN} (Pin 21): Input Supply Pin. Connect this pin to the input supply and decouple with at least a 4.7µF ceramic capacitor.

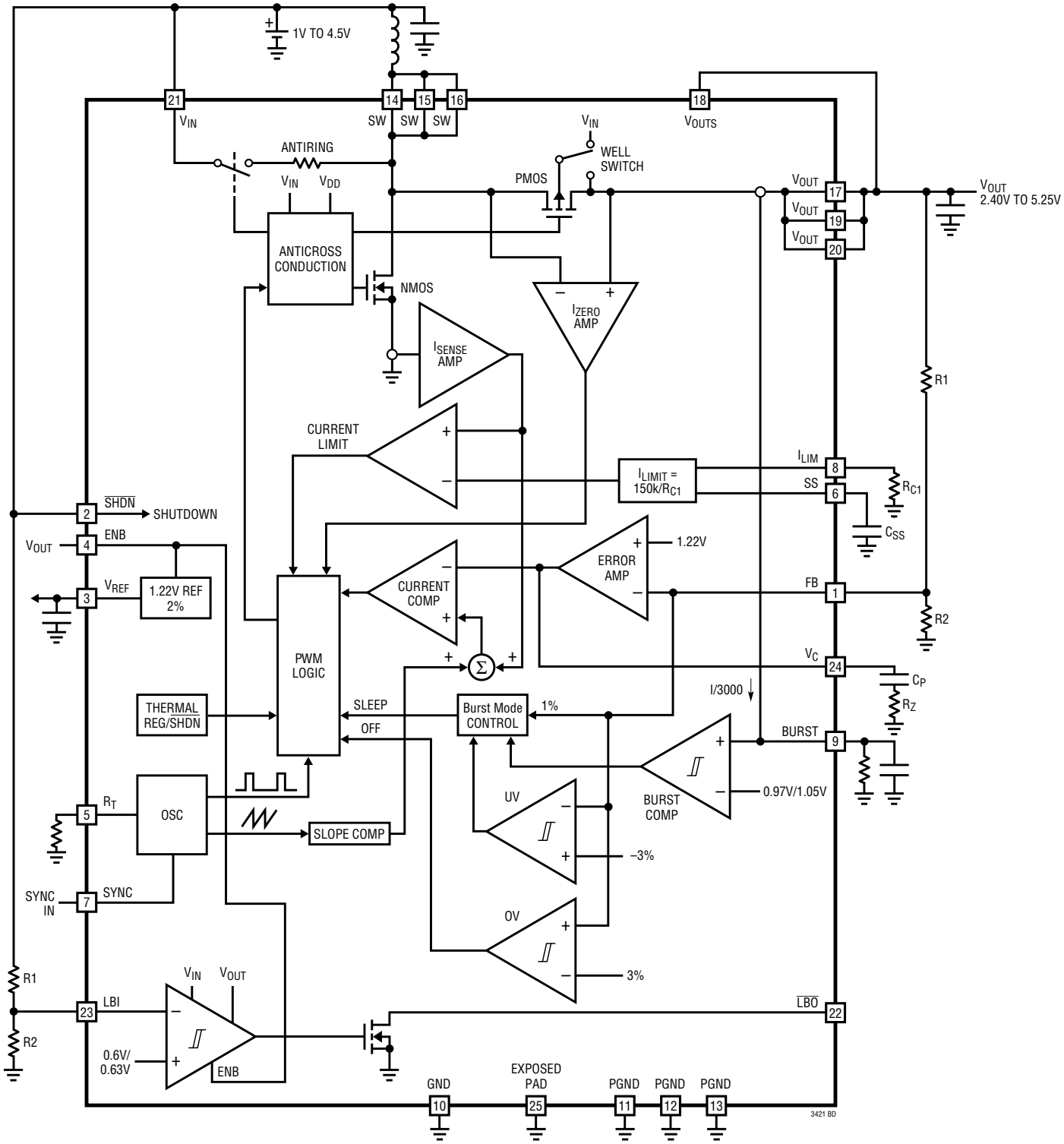
$\overline{LBO}$ (Pin 22): Open-Drain Output. This pin pulls low when the LBI input is below 0.6V. The open-drain output can sink up to 20mA. During Burst Mode operation $\overline{LBO}$ is only active during the time the IC wakes up to service the output.

LBI (Pin 23): Low-Battery Comparator Input. Typical threshold voltage is 0.6V with 30mV hysteresis. This function is always enabled in non-back-fed applications. To enable this comparator when V_{OUT} is back-fed, the ENB pin must be high. The low-battery comparator will operate off V_{IN} or V_{OUT}, whichever is greater.

V_C (Pin 24): Error Amp Output. A frequency compensation network is connected from this pin to ground to compensate the loop. See the section Closing the Feedback Loop for guidelines.

Exposed Pad (Pin 25): Ground. This pin must be soldered to the PCB and is typically connected through the power GND plane.

BLOCK DIAGRAM



OPERATION

LOW VOLTAGE START-UP

The LTC3421 includes an independent start-up oscillator designed to start-up at input voltages of 0.85V typical. The frequency and peak current limit during start-up are internally controlled. The device can start-up under some load (see graph of Start-Up Current vs Input Voltage). Soft-start and inrush current limiting are provided during start-up as well as normal mode. The same soft-start capacitor is used for each operating mode.

When either V_{IN} or V_{OUT} exceeds 2.25V, the IC enters normal operating mode. Once the output voltage exceeds the input by 0.3V, the IC powers itself from V_{OUT} instead of V_{IN}. At this point the internal circuitry has no dependency on the V_{IN} input voltage, eliminating the requirement for a large input capacitor. The input voltage can drop as low as 0.5V without affecting circuit operation. The limiting factor for the application becomes the availability of the power source to supply sufficient energy to the output at the low voltages and the maximum duty cycle, which is clamped at 91% typical.

LOW NOISE FIXED FREQUENCY OPERATION

Shutdown

The part is shut down by pulling $\overline{SHDN}$ below 0.25V, and activated by pulling the pin initially above 1V and maintaining a high state down to 0.5V. Note that the $\overline{SHDN}$ pin can be driven above V_{IN} or V_{OUT} as long as it is limited to less than the absolute maximum rating.

Soft-Start

The soft-start time is programmed with an external capacitor to ground on the SS pin. An internal current source charges it with a nominal 2.5µA. The voltage on the SS pin (in conjunction with the external resistor on the I_{LIM} pin) is used to control the peak current limit until the voltage on the capacitor exceeds 1.6V, at which point the external resistor sets the peak current. In the event of a commanded shutdown or a thermal shutdown, the capacitor is discharged automatically. Note that Burst Mode operation is inhibited during the soft-start time.

$$t(ms) = C_{SS}(\mu F) \bullet 320$$

Oscillator

The frequency of operation is set through a resistor from the R_T pin to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator can be synchronized with an external clock applied to the SYNC pin. When synchronizing the oscillator, the free running frequency must be set to an approximately 30% lower frequency than the desired synchronized frequency.

Current Sensing

Lossless current sensing converts the peak current signal to a voltage to sum in with the internal slope compensation. This summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. The slope compensation in the IC is adaptive to the input voltage and output voltage. Therefore, the converter provides the proper amount of slope compensation to ensure stability, but not an excess to cause a loss of phase margin in the converter.

Error Amplifier

The error amplifier is a transconductance amplifier, with its positive input internally connected to the 1.22V reference and its negative input connected to FB. A simple compensation network is placed from COMP to ground. Internal clamps limit the minimum and maximum error amplifier output voltage for improved large-signal transient response. During sleep (in Burst Mode operation), the compensation pin is high impedance; however, clamps limit the voltage on the external compensation network, preventing the compensation capacitor from discharging to zero during the sleep time.

Current Limit

The programmable current limit circuit sets the maximum peak current. This clamp level is programmed with a resistor from I_{LIM} to ground. In Burst Mode operation, the current limit is automatically set to a nominal value of 0.6A peak for optimal efficiency.

$$I_{LIM} = \frac{150}{R}$$

where I is in amps and R is in kΩ.

OPERATION

Zero Current Amplifier

The zero current amplifier monitors the inductor current to the output and shuts off the synchronous rectifier once the current is below 50mA typical, preventing negative inductor current.

Antiringing Control

The antiringing control places a resistor across the inductor to damp the ringing on the SW pin in discontinuous conduction mode. The LC_{SW} ringing (L = inductor, C_{SW} = capacitance on SW pin) is low energy, but can cause EMI radiation.

V_{REF}

The internal 1.22V reference is buffered and brought out to V_{REF}. It is active when the ENB pin is pulled high (above 1.2V). For stability, a minimum of a 0.1µF capacitor must be placed on the pin. The output can source up to 100µA and sink up to 8µA. For the lowest possible quiescent current in Burst Mode operation, the reference output should be disabled by grounding the ENB pin.

Burst Mode OPERATION

Burst Mode operation can be automatic or user controlled. In automatic operation, the IC will automatically enter Burst Mode operation at light load and return to fixed frequency PWM mode for heavier loads. The user can program the average load current at which the mode transition occurs using a single resistor.

The oscillator is shut down in this mode, since the on time is determined by the time it takes the inductor current to reach a fixed peak current and the off time is determined by the time it takes for the inductor current to return to zero.

In Burst Mode operation, the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 12µA of quiescent current. In this mode, the output ripple has a variable frequency component with load current and will be typically 2% peak-peak. This maximizes efficiency at very light loads by minimizing switching and quiescent losses. Burst Mode ripple can be reduced slightly by increasing the output capacitance. Another method of reducing Burst Mode ripple is to place a small feedforward capacitor across the upper resistor in the V_{OUT} feedback divider network.

During Burst Mode operation, the V_C pin is disconnected from the error amplifier in an effort to hold the voltage on the external compensation network where it was before entering Burst Mode operation. To minimize the effects of leakage current and stray resistance, voltage clamps limit the min and max voltage on V_C during Burst Mode operation. This minimizes the transient experienced when a heavy load is suddenly applied to the converter after being in Burst Mode operation for an extended period of time.

For automatic operation, an RC network should be connected from BURST to ground. The value of the resistor will control the average load current (I_{BURST}) at which Burst Mode operation will be entered and exited (there is hysteresis to prevent oscillation between modes). The equation given for the capacitor on BURST is for the minimum value to prevent ripple on BURST from causing the part to oscillate in and out of Burst Mode operation at the current where the mode transition occurs.

$$R_{BURST} = \frac{2}{I_{BURST}}$$

where R_{BURST} is in kΩ and I_{BURST} is in amps.

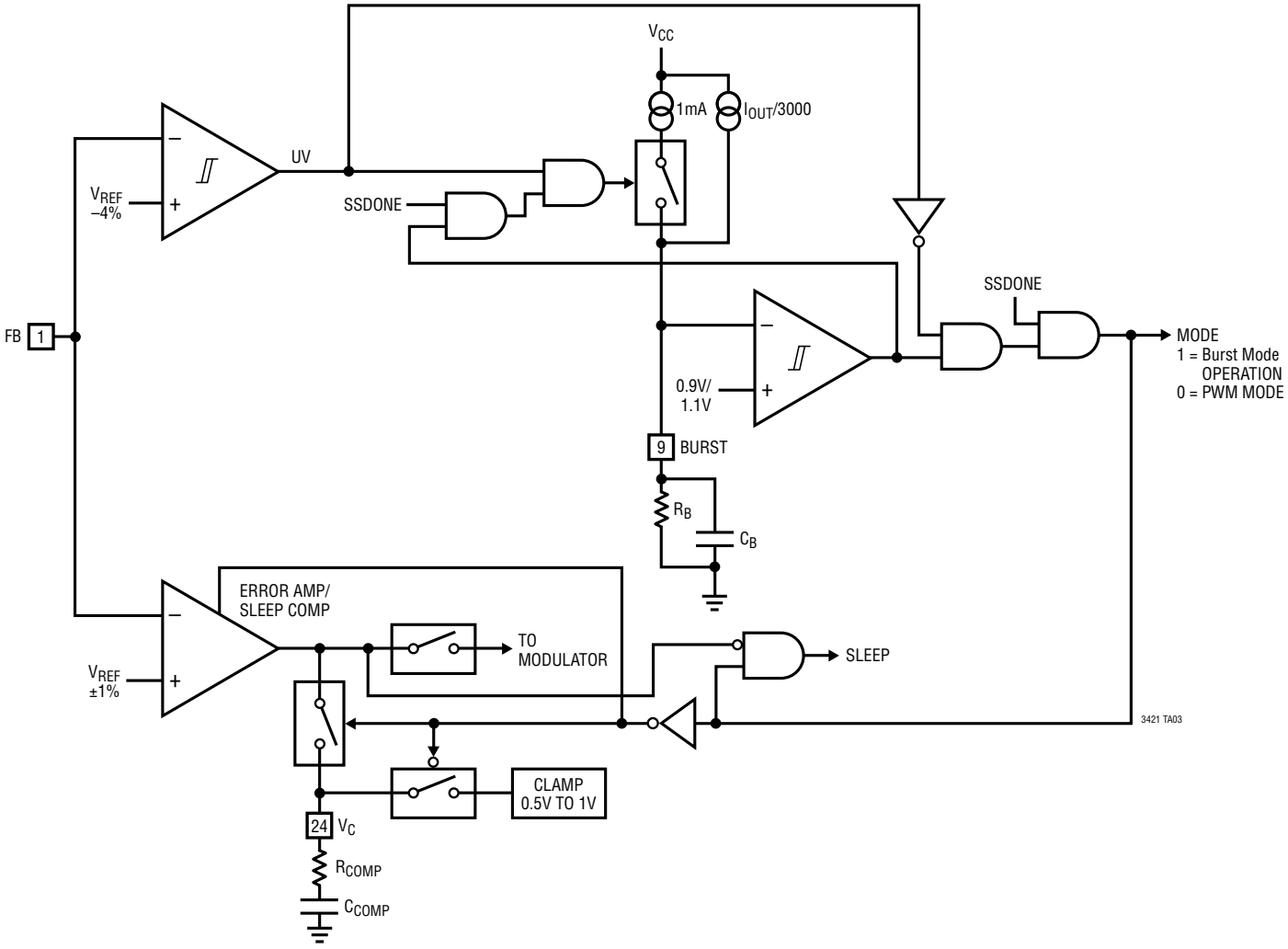
$$C_{BURST} \geq \frac{C_{OUT} \bullet V_{OUT}}{10{,}000}$$

where $C_{BURST(MIN)}$ and C_{OUT} are in µF.

In the event that a sudden load transient causes FB to deviate by more than 4% from the regulation value, an internal pull-up is applied to BURST, forcing the part quickly out of Burst Mode operation. For optimum transient response when going between Burst Mode operation and PWM mode, the mode should be controlled manually by the host. This way PWM mode can be commanded before the load step occurs, minimizing output voltage droop. For manual control of Burst Mode operation, the RC network can be eliminated. To force fixed frequency PWM mode, BURST should be connected to V_{OUT}. To force Burst Mode operation, BURST should be

OPERATION

Simplified Diagram of Automatic Burst Mode Control Circuit



grounded. The circuit connected to BURST should be able to sink or source up to 2mA. Note that Burst Mode operation is inhibited during start-up and soft-start.

Note that if V_{IN} is above V_{OUT} – 0.3V, the part will exit Burst Mode operation and the synchronous rectifier will be disabled.

Note that if the load applied during forced Burst Mode operation exceeds the current that can be supplied, the output voltage will start to droop and the part will automatically come out of Burst Mode operation and enter fixed frequency mode, raising V_{OUT}. The maximum current that can be supplied in Burst Mode operation is given by:

$$I_{O(MAX)} = \frac{0.55}{2 \bullet \frac{1+(V_{OUT}-V_{IN})}{V_{IN}}} \text{ in amps}$$

OUTPUT DISCONNECT AND INRUSH LIMITING

The LTC3421 is designed to allow true output disconnect by eliminating body diode conduction of the internal P-channel MOSFET rectifier. This allows V_{OUT} to go to zero volts during shutdown without drawing any current from the input source. It also allows for inrush current limiting at turn-on, minimizing surge currents seen by the input supply. Note that to obtain the advantages of output

OPERATION

disconnect, there must not be any external Schottky diodes connected between the SW pins and V_{OUT}.

Note: Board layout is extremely critical to minimize voltage overshoot on the SW pins due to stray inductance. Keep the output filter capacitors as close as possible to the V_{OUT} pins and use very low ESR/ESL ceramic capacitors, tied to a good ground plane. In V_{OUT} > 4.3V applications, a Schottky diode is required from the switch nodes to V_{OUT} to limit the peak switch voltage to less than 6V unless some form of external snubbing is employed. (See 5V Applications section.)

APPLICATIONS INFORMATION

COMPONENT SELECTION

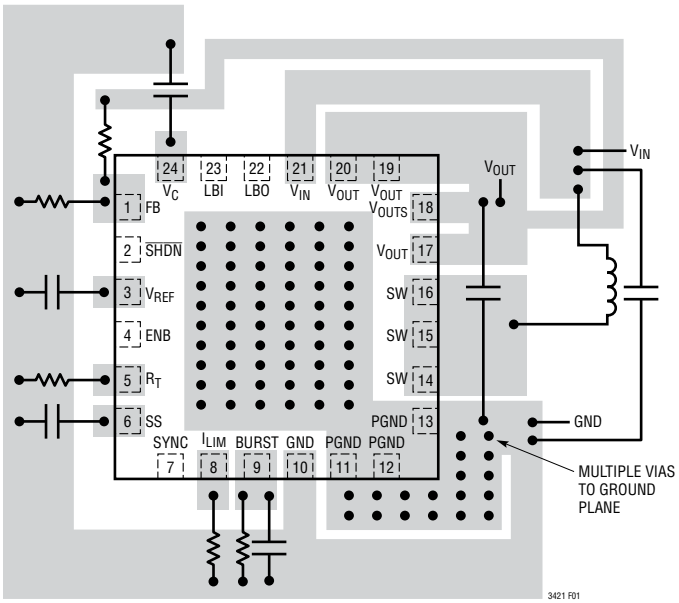


Figure 1. Recommended Component Placement. Traces Carrying High Current are Direct (PGND, SW, V_{OUT}). Trace Area at FB and V_C are Kept Low. Lead Length to Battery Should be Kept Short. V_{IN} and V_{OUT} Ceramic Capacitors Should be as Close to the IC Pins as Possible

Inductor Selection

The high frequency operation of the LTC3421 allows the use of small surface mount inductors. The minimum inductance value is proportional to the operating frequency and is limited by the following constraints:

$$L > \frac{3}{f} \text{ and } L > \frac{V_{IN(MIN)} \bullet \left(V_{OUT(MAX)} - V_{IN(MIN)}\right)}{f \bullet Ripple \bullet V_{OUT(MAX)}}$$

where

f = Operating Frequency in MHz

Ripple = Allowable Inductor Current Ripple (Amps Peak-Peak)

$V_{IN(MIN)}$ = Minimum Input Voltage

$V_{OUT(MAX)}$ = Maximum Output Voltage

The inductor current ripple is typically set to 20% to 40% of the maximum inductor current.

For high efficiency, choose an inductor with high frequency core material, such as ferrite, to reduce core loses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support peak inductor currents in the 1A to 4A region. To minimize radiated noise, use a toroidal or shielded inductor. See Table 1 for suggested inductor suppliers and Table 2 for a list of capacitor suppliers.

Table 1. Inductor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
Coiltronics	(561) 241-7876	(516) 241-9339	
Murata	USA: (814) 237-1431 (800) 831-9172	USA: (814) 238-0490	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81-3-3607-5111	USA: (847) 956-0702 Japan 81-3-3607-5144	www.sumida.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com
TOKO	(847) 297-0070	(847) 669-7864	www.toko.com

APPLICATIONS INFORMATION

Output Capacitor Selection

The output voltage ripple has two components to it. The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The maximum ripple due to charge is given by:

$$V_{RBULK} = \frac{I_P \bullet V_{IN}}{C_{OUT} \bullet V_{OUT} \bullet f}$$

where I_P = peak inductor current.

The ESR (equivalent series resistance) is usually the most dominant factor for ripple in most power converters. The ripple due to capacitor ESR is simply given by:

$$V_{RCESR} = I_P \bullet C_{ESR}$$

where C_{ESR} = capacitor series resistance.

Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, AVX TPS series tantalum capacitors, Sanyo POSCAP or Taiyo Yuden ceramic capacitors are recommended. For through-hole applications, Sanyo OS-CON capacitors offer low ESR in a small package size.

In some layouts it may be necessary to place a 1µF low ESR ceramic capacitor as close to the V_{OUT} and GND pins as possible.

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. Since the IC can operate at voltages below 0.5V once the output is regulated, the demand on the input capacitor is much less. In most applications 1µF per amp of peak input current is recommended. Taiyo Yuden offers very low ESR ceramic capacitors, for example the 1µF in a 0603 case (JMK107BJ105MA).

Table 2. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com
Murata	USA: (814) 237-1431 (800) 831-9172	USA: (814) 238-0490	www.murata.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com

Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is, which are the sensitive frequency bands that cannot tolerate any spectral noise? The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade off is in efficiency since the switching losses due to gate charge are going up proportional with frequency.

Another operating frequency consideration is whether the application can allow "pulse skipping." In this mode, the minimum on time of the converter cannot support the duty cycle, so the converter ripple will go up and there will be a low frequency component of the output ripple. In many applications where physical size is the main criterion, running the converter in this mode is acceptable. In applications where it is preferred not to enter this mode, the maximum operating frequency is given by:

$$f_{MAX\_NOSKIP} = \frac{V_{OUT} - V_{IN}}{V_{OUT} \bullet t_{ON(MIN)}} Hz$$

where $t_{ON(MIN)}$ = minimum on time = 120ns.

Thermal Considerations

To deliver the power that the LTC3421 is capable of, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the large thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible. In the event that the junction temperature gets too high, the peak current limit will automatically be decreased. If the junction temperature continues to rise, the part will go into thermal shutdown, and all switching will stop until the temperature drops.

$V_{IN} > V_{OUT}$ Operation

The LTC3421 will maintain voltage regulation when the input voltage is above the output voltage. This is achieved by terminating the switching on the synchronous PMOS and applying V_{IN} statically on the gate. This will ensure

APPLICATIONS INFORMATION

the volts • seconds of the inductor will reverse during the time current is flowing to the output. Since this mode will dissipate more power in the IC, the maximum output current is limited in order to maintain an acceptable junction temperature.

$$I_{OUT(MAX)} = \frac{125 - T_A}{40 \bullet \left((V_{IN} + 1.5) - V_{OUT} \right)}$$

where T_A = ambient temperature.

For example at V_{IN} = 4.5V and V_{OUT} = 3.3V and T_A = 85°C, the maximum output current is 370mA.

Short Circuit

The LTC3421 output disconnect feature allows output short circuit while maintaining a maximum set current limit. The IC has incorporated internal features such as current limit and thermal shutdown for protection from an excessive overload or short circuit. In applications that require a prolonged short circuit, it is recommended to limit the power dissipation in the IC to maintain an acceptable junction temperature. The circuit in Figure 2 will limit the maximum current during a prolonged short by reducing the current limit value in a short circuit by disconnecting R2 with the N-channel MOSFET switch. R3 and C1 provide a soft-start function after a short circuit. Resistor R1 lowers the current limit value as V_{IN} rises, maintaining a relatively constant power. The current limit equation for the circuit in Figure 2 is given by:

$$I_{LIMIT} = \left(\frac{0.6}{R_{LIM}} - \frac{V_{IN} - 0.6}{R1} \right) \bullet 250$$

where I_{LIMIT} is in Amps; R_{LIM} and R1 are in kΩ.

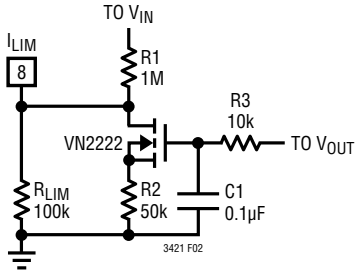


Figure 2. Current Limit Foldback Circuit for Extended Short Conditions

Closing the Feedback Loop

The LTC3421 uses current mode control with internal adaptive slope compensation. Current mode control eliminates the 2nd order filter due to the inductor and output capacitor exhibited in voltage mode controllers, and simplifies it to a single pole filter response. The product of the modulator control to output DC gain and the error amp open-loop gain gives the DC gain of the system:

$$G_{DC} = G_{CONTROL\_OUTPUT} \bullet G_{EA} \bullet \frac{V_{REF}}{V_{OUT}}$$

$$G_{CONTROL} = \frac{2 \bullet V_{IN}}{I_{OUT}}, G_{EA} \approx 2000$$

The output filter pole is given by:

$$f_{FILTER\_POLE} = \frac{I_{OUT}}{\pi \bullet V_{OUT} \bullet C_{OUT}}$$

where C_{OUT} is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

where R_{ESR} is the capacitor equivalent series resistance.

A troublesome feature of the boost regulator topology is the right-half plane zero (RHP) and is given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2 \bullet \pi \bullet I_{OUT} \bullet L}$$

At heavy loads this gain increase with phase lag can occur at a relatively low frequency. The loop gain is typically rolled off before the RHP zero frequency.

The typical error amp compensation is shown in Figure 4. The equations for the loop dynamics are as follows:

$$f_{POLE1} \approx \frac{1}{2 \bullet \pi \bullet 20e6 \bullet C_{C1}}$$ which is extremely close to DC

$$f_{ZERO1} \approx \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{C1}}$$

$$f_{POLE2} \approx \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{C2}}$$

APPLICATIONS INFORMATION

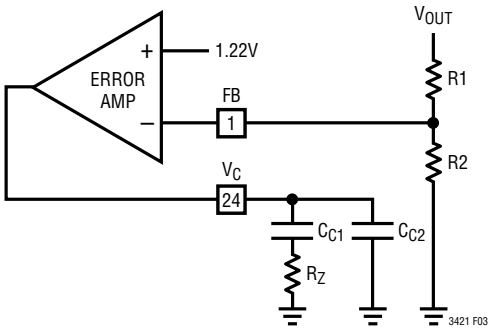
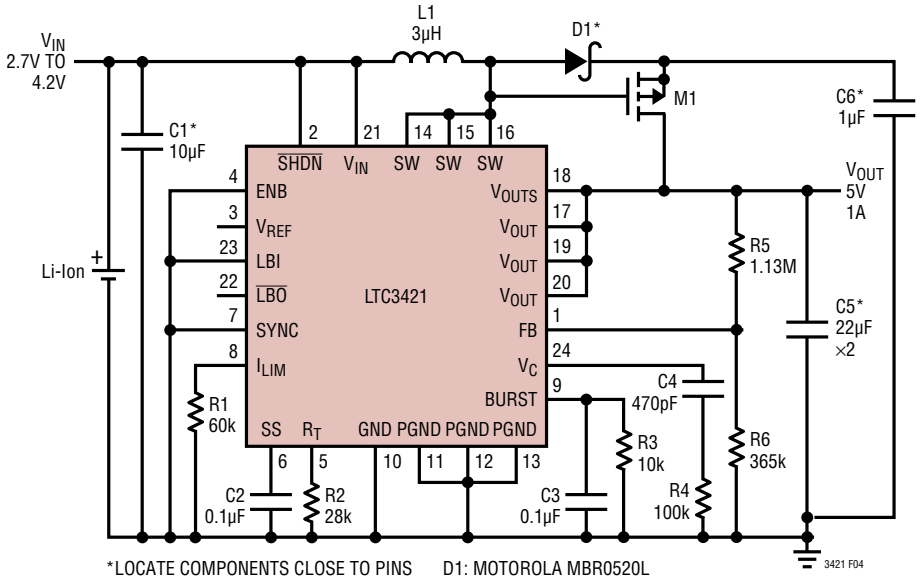


Figure 4.

TYPICAL APPLICATION

5V Applications

When the output voltage is programmed above 4.3V it is necessary to add a Schottky diode either from SW to V_{OUT}, or to a snubber network in order to maintain an acceptable peak voltage on SW. The Schottky to the output will provide a peak efficiency improvement but will negate the output disconnect feature. If output disconnect is required, the Schottky to an active snubber network is suggested as shown in Figure 3.



*LOCATE COMPONENTS CLOSE TO PINS
C1: TAIYO YUDEN JMK212BJ106MM
C5: TAIYO YUDEN JMK325BJ226MM
D1: MOTOROLA MBR0520L
L1: SUMIDA CDRH6D28-3R0
M1: ZETEX ZXM61P025

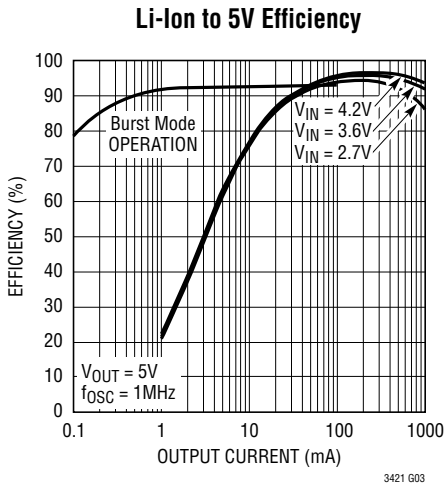
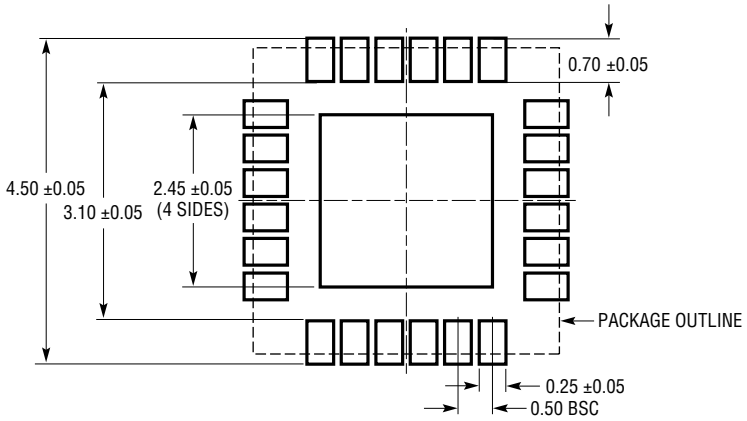


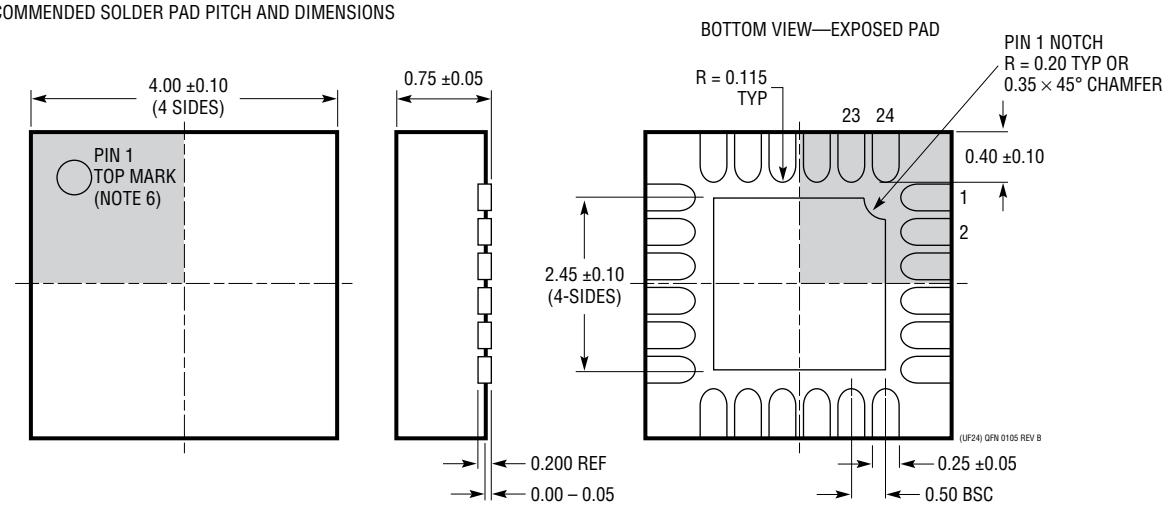
Figure 3. Lithium-Ion to 5V at 1A Application with an Active Snubber Circuit

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



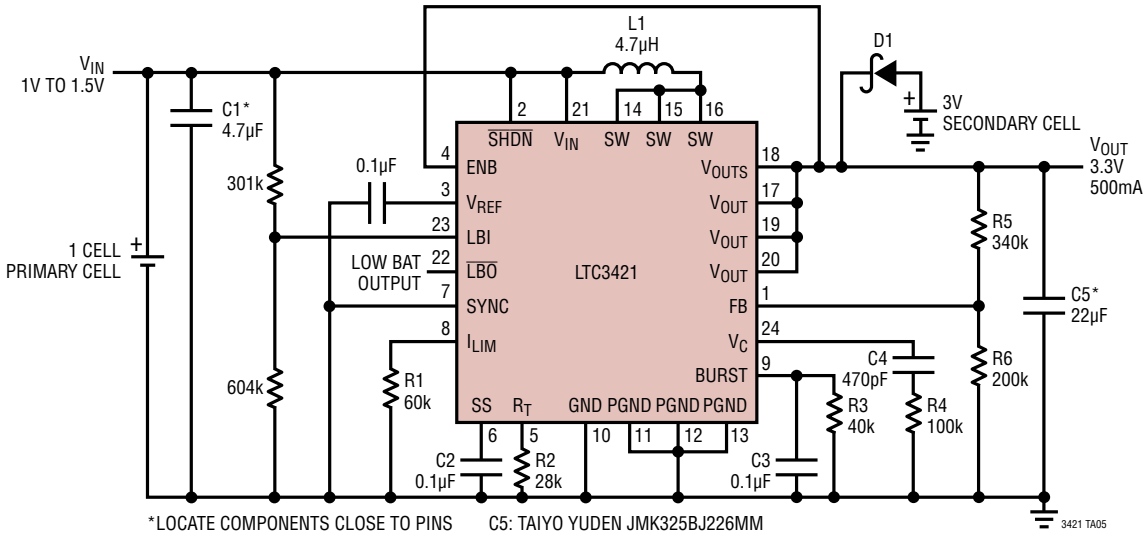
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/18	Clarified Typical Application	1
		Clarified Order Information	2
		Clarified Note 5	3
		Clarified SHDN Input High and LDO Leakage Conditions	3
		Clarified $R_{DS(ON)}$ vs Temp Graph	5
		Clarified ENB (Pin 4) description	5
		Clarified GND, Exposed Pad (Pin 10, Pin 25) and LBI (Pin 23) description	6
		Clarified Shutdown paragragh	8
		Clarified V_{REF} paragragh	9
		Clarified $V_{IN} > V_{OUT}$ paragraph	13

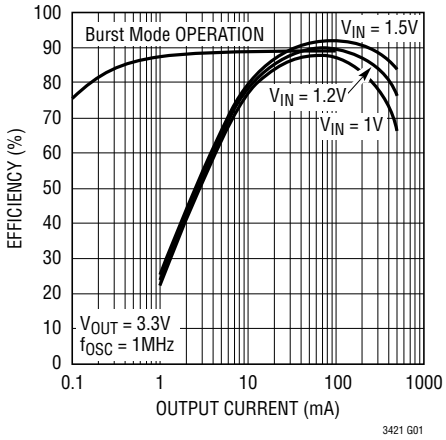
TYPICAL APPLICATION

Single Cell to 3.3V at 500mA with Secondary Cell Backup During Shutdown. LOWBAT and V_{REF} Output are Enabled



*LOCATE COMPONENTS CLOSE TO PINS
C1: TAIYO YUDEN JMK212BJ106MM
C5: TAIYO YUDEN JMK325BJ226MM
L1: TOKO A916CY-4R7M

Single Cell to 3.3V Efficiency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3402	2A I_{SW}, 3MHz, Synchronous Step-Up DC/DC Converter	97% Efficiency, V_{IN} = 0.5V to 5V, $V_{OUT(MAX)}$ = 5.5V, I_Q = 38µA, I_{SD} < 1µA, MS10
LTC3425	5A I_{SW}, 8MHz, Low Ripple, 4-Phase Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA, QFN32
LTC3539/ LTC3539-2	2A I_{SW}, 1MHz/2MHz Synchronous Step-Up DC/DC Converters with Output Disconnect, Burst Mode Operation	94% Efficiency, V_{IN}: 700mV to 5.25V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 10µA, I_{SD} < 1µA, 2mm × 3mm DFN Package
LTC3122	2.5A I_{SW}, 3MHz, Synchronous Step-Up DC/DC Converter with Output Disconnect, Burst Mode Operation	95% Efficiency V_{IN}: 1.8V to 5.5V [500mV After Start-Up], $V_{OUT(MAX)}$ = 15V, I_Q = 25µA, I_{SD} < 1µA, 3mm × 4mm DFN and MSOP Packages
LTC3124	5A I_{SW}, 6MHz, Dual Phase, Synchronous Step-Up DC/DC Converter with Output Disconnect, Burst Mode Operation	95% Efficiency, V_{IN}: 1.8V to 5.5V [500mV After Start-Up], $V_{OUT(MAX)}$ = 15V, I_Q = 25µA, I_{SD} < 1µA, 3mm × 4mm DFN and TSSOP Packages