

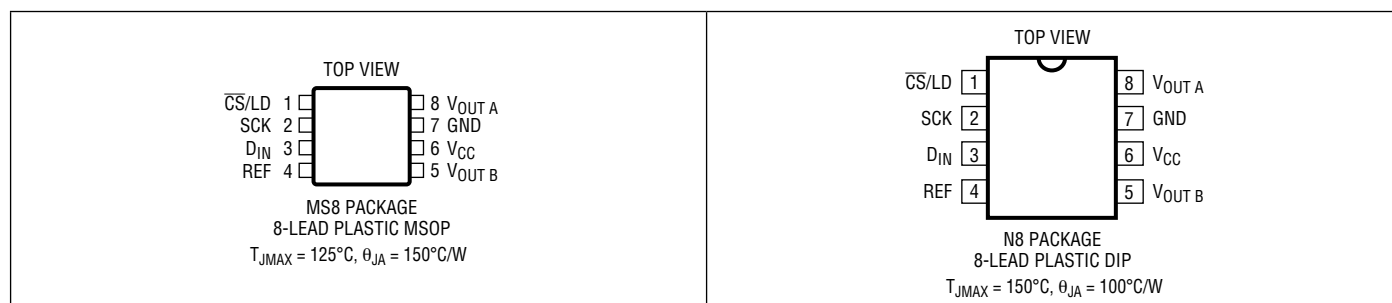
# LTC1661

## ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{CC}$  to GND ..... -0.3V to 7.5V  
 Logic Inputs to GND ..... -0.3V to 7.5V  
 $V_{OUT A}$ ,  $V_{OUT B}$ , REF to GND ..... -0.3V to  $V_{CC} + 0.3V$   
 Maximum Junction Temperature..... 125°C  
 Storage Temperature Range..... -65°C to 150°C

Operating Temperature Range  
 LTC1661C ..... 0°C to 70°C  
 LTC1661I ..... -40°C to 85°C  
 Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION



## ORDER INFORMATION (<http://www.linear.com/product/LTC1661#orderinfo>)

### Lead Free Finish

| TUBE            | TAPE AND REEL     | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|-----------------|-------------------|--------------|---------------------|-------------------|
| LTC1661CMS8#PBF | LTC1661CMS8#TRPBF | LTDV         | 8-Lead Plastic MSOP | 0°C to 70°C       |
| LTC1661IMS8#PBF | LTC1661IMS8#TRPBF | LTDW         | 8-Lead Plastic MSOP | -40°C to 85°C     |
| LTC1661CN8#PBF  | LTC1661CN8#TRPBF  | LTC1661CN8   | 8-Lead Plastic DIP  | 0°C to 70°C       |
| LTC1661IN8#PBF  | LTC1661IN8#TRPBF  | LTC1661IN8   | 8-Lead Plastic DIP  | -40°C to 85°C     |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$ . $V_{CC} = 2.7V$ to 5.5V, $V_{REF} \leq V_{CC}$ , $V_{OUT}$ unloaded unless otherwise noted.

| SYMBOL          | PARAMETER                                | CONDITIONS                                    | MIN | TYP  | MAX   | UNITS |
|-----------------|------------------------------------------|-----------------------------------------------|-----|------|-------|-------|
| <b>Accuracy</b> |                                          |                                               |     |      |       |       |
|                 | Resolution                               |                                               | ●   | 10   |       | Bits  |
|                 | Monotonicity                             | $1V \leq V_{REF} \leq V_{CC} - 0.1V$ (Note 2) | ●   | 10   |       | Bits  |
| DNL             | Differential Nonlinearity                | $1V \leq V_{REF} \leq V_{CC} - 0.1V$ (Note 2) | ●   | ±0.1 | ±0.75 | LSB   |
| INL             | Integral Nonlinearity                    | $1V \leq V_{REF} \leq V_{CC} - 0.1V$ (Note 2) | ●   | ±0.4 | ±2    | LSB   |
| $V_{OS}$        | Offset Error                             | Measured at Code 20                           | ●   | ±5   | ±30   | mV    |
|                 | $V_{OS}$ Temperature Coefficient         |                                               |     | ±15  |       | μV/°C |
| FSE             | Full-Scale Error                         | $V_{CC} = 5V$ , $V_{REF} = 4.096V$            | ●   | ±1   | ±12   | LSB   |
|                 | Full-Scale Error Temperature Coefficient |                                               |     | ±30  |       | μV/°C |

1661fb

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 2.7\text{V}$  to  $5.5\text{V}$ ,  $V_{REF} \leq V_{CC}$ ,  $V_{OUT}$  unloaded unless otherwise noted.

| SYMBOL          | PARAMETER                    | CONDITIONS                                                |        | MIN          | TYP      | MAX        | UNITS                    |
|-----------------|------------------------------|-----------------------------------------------------------|--------|--------------|----------|------------|--------------------------|
| PSR             | Power Supply Rejection       | $V_{REF} = 2.5V$                                          |        | 0.18         |          |            | LSB/V                    |
| Reference Input |                              |                                                           |        |              |          |            |                          |
|                 | Input Voltage Range          |                                                           | ●      | 0            | $V_{CC}$ |            | V                        |
|                 | Resistance                   | Active Mode                                               | ●      | 140          | 260      |            | k $\Omega$               |
|                 | Capacitance                  |                                                           | ●      | 15           |          |            | pF                       |
| $I_{REF}$       | Reference Current            | Sleep Mode                                                | ●      | 0.001        | 1        |            | $\mu A$                  |
| Power Supply    |                              |                                                           |        |              |          |            |                          |
| $V_{CC}$        | Positive Supply Voltage      | For Specified Performance                                 | ●      | 2.7          | 5.5      |            | V                        |
| $I_{CC}$        | Supply Current               | $V_{CC} = 5V$ (Note 3)                                    | ●      | 120          |          | 195        | $\mu A$                  |
|                 |                              | $V_{CC} = 3V$ (Note 3)                                    | ●      | 95           |          | 154        | $\mu A$                  |
|                 |                              | Sleep Mode (Note 3)                                       | ●      | 1            |          | 3          | $\mu A$                  |
| DC Performance  |                              |                                                           |        |              |          |            |                          |
|                 | Short-Circuit Current Low    | $V_{OUT} = 0V, V_{CC} = V_{REF} = 5V, \text{Code} = 1023$ | ●      | 10           | 25       | 100        | mA                       |
|                 | Short-Circuit Current High   | $V_{OUT} = V_{CC} = V_{REF} = 5V, \text{Code} = 0$        | ●      | 7            | 19       | 120        | mA                       |
| AC Performance  |                              |                                                           |        |              |          |            |                          |
|                 | Voltage Output Slew Rate     | Rising (Notes 4, 5)<br>Falling (Notes 4, 5)               |        | 0.60<br>0.25 |          |            | V/ $\mu s$<br>V/ $\mu s$ |
|                 | Voltage Output Settling Time | To $\pm 0.5LSB$ (Notes 4, 5)                              |        | 30           |          |            | $\mu s$                  |
|                 | Capacitive Load Driving      |                                                           |        | 1000         |          |            | pF                       |
| Digital I/O     |                              |                                                           |        |              |          |            |                          |
| $V_{IH}$        | Digital Input High Voltage   | $V_{CC} = 2.7V$ to $5.5V$<br>$V_{CC} = 2.7V$ to $3.6V$    | ●<br>● | 2.4<br>2.0   |          |            | V<br>V                   |
| $V_{IL}$        | Digital Input Low Voltage    | $V_{CC} = 4.5V$ to $5.5V$<br>$V_{CC} = 2.7V$ to $5.5V$    | ●<br>● |              |          | 0.8<br>0.6 | V<br>V                   |
| $I_{LK}$        | Digital Input Leakage        | $V_{IN} = GND$ to $V_{CC}$                                | ●      |              |          | $\pm 10$   | $\mu A$                  |
| $C_{IN}$        | Digital Input Capacitance    | (Note 6)                                                  | ●      |              |          | 10         | pF                       |

## TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

| SYMBOL                                                               | PARAMETER                                                  | CONDITIONS           | MIN | TYP | MAX  | UNITS |
|----------------------------------------------------------------------|------------------------------------------------------------|----------------------|-----|-----|------|-------|
| <b><math>V_{CC} = 4.5\text{V}</math> to <math>5.5\text{V}</math></b> |                                                            |                      |     |     |      |       |
| $t_1$                                                                | $D_{IN}$ Valid to SCK Setup                                |                      | ●   | 40  |      | ns    |
| $t_2$                                                                | $D_{IN}$ Valid to SCK Hold                                 |                      | ●   | 0   |      | ns    |
| $t_3$                                                                | SCK High Time                                              | (Note 6)             | ●   | 30  |      | ns    |
| $t_4$                                                                | SCK Low Time                                               | (Note 6)             | ●   | 30  |      | ns    |
| $t_5$                                                                | $\overline{\text{CS}}/\text{LD}$ Pulse Width               | (Note 6)             | ●   | 80  |      | ns    |
| $t_6$                                                                | LSB SCK High to $\overline{\text{CS}}/\text{LD}$ High      | (Note 6)             | ●   | 30  |      | ns    |
| $t_7$                                                                | $\overline{\text{CS}}/\text{LD}$ Low to SCK High           | (Note 6)             | ●   | 20  |      | ns    |
| $t_9$                                                                | SCK Low to $\overline{\text{CS}}/\text{LD}$ Low            | (Note 6)             | ●   | 0   |      | ns    |
| $t_{11}$                                                             | $\overline{\text{CS}}/\text{LD}$ High to SCK Positive Edge | (Note 6)             | ●   | 20  |      | ns    |
|                                                                      | SCK Frequency                                              | Square Wave (Note 6) | ●   |     | 16.7 | MHz   |

## TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

| SYMBOL                                                               | PARAMETER                                    | CONDITIONS           | MIN | TYP | MAX | UNITS   |
|----------------------------------------------------------------------|----------------------------------------------|----------------------|-----|-----|-----|---------|
| <b><math>V_{CC} = 2.7\text{V}</math> to <math>5.5\text{V}</math></b> |                                              |                      |     |     |     |         |
| $t_1$                                                                | $D_{IN}$ Valid to SCK Setup                  | (Note 6)             | ●   | 60  |     | ns      |
| $t_2$                                                                | $D_{IN}$ Valid to SCK Hold                   | (Note 6)             | ●   | 0   |     | ns      |
| $t_3$                                                                | SCK High Time                                | (Note 6)             | ●   | 50  |     | ns      |
| $t_4$                                                                | SCK Low Time                                 | (Note 6)             | ●   | 50  |     | ns      |
| $t_5$                                                                | $\overline{CS}/LD$ Pulse Width               | (Note 6)             | ●   | 100 |     | ns      |
| $t_6$                                                                | LSB SCK High to $\overline{CS}/LD$ High      | (Note 6)             | ●   | 50  |     | ns      |
| $t_7$                                                                | $\overline{CS}/LD$ Low to SCK High           | (Note 6)             | ●   | 30  |     | ns </td |
| $t_9$                                                                | SCK Low to $\overline{CS}/LD$ Low            | (Note 6)             | ●   | 0   |     | ns      |
| $t_{11}$                                                             | $\overline{CS}/LD$ High to SCK Positive Edge | (Note 6)             | ●   | 30  |     | ns      |
|                                                                      | SCK Frequency                                | Square Wave (Note 6) | ●   |     | 10  | MHz     |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Nonlinearity and monotonicity are defined from code 20 to code 1023 (full scale). See Applications Information.

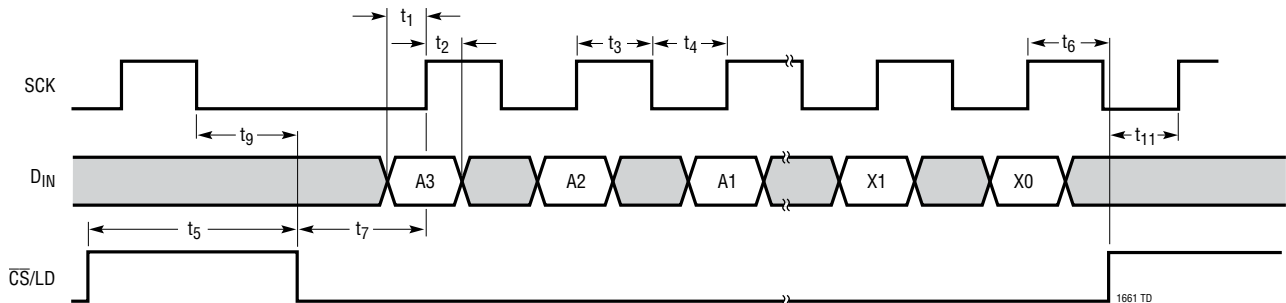
**Note 3:** Digital inputs at 0V or  $V_{CC}$ .

**Note 4:** Load is  $10\text{k}\Omega$  in parallel with  $100\text{pF}$ .

**Note 5:**  $V_{CC} = V_{REF} = 5\text{V}$ . DAC switched between  $0.1V_{FS}$  and  $0.9V_{FS}$ , i.e., codes  $k = 102$  and  $k = 922$ .

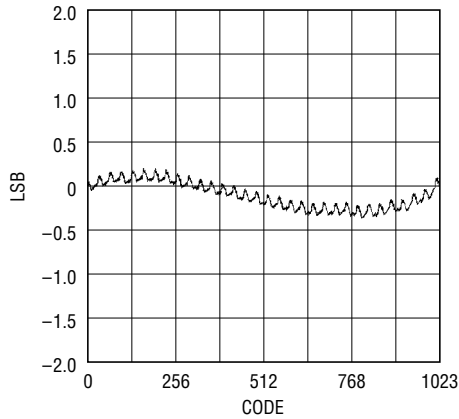
**Note 6:** Guaranteed by design and not subject to test.

## TIMING DIAGRAM



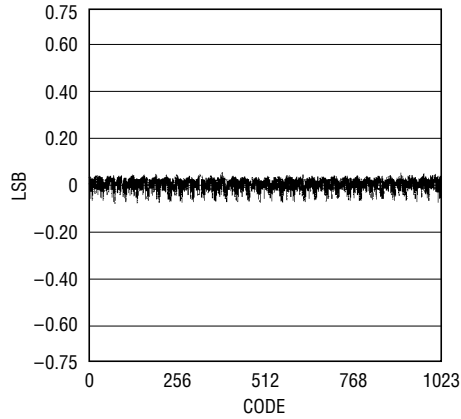
## TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity (INL)



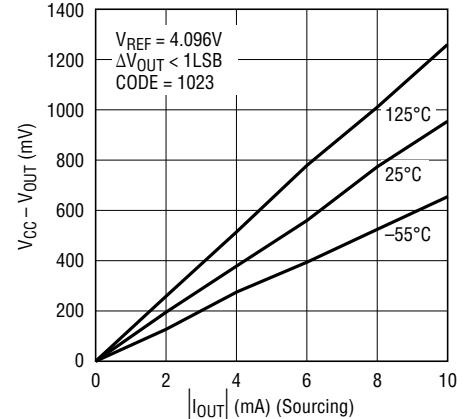
1661 G01

Differential Nonlinearity (DNL)

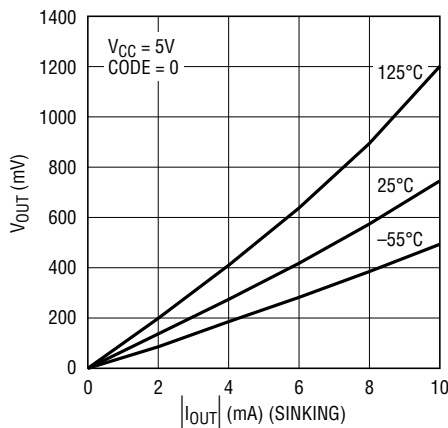


1661 G02

Minimum Supply Headroom vs Load Current (Output Sourcing)

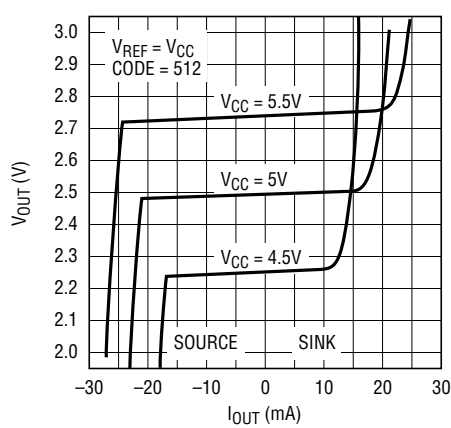


1661 G03

Minimum  $V_{OUT}$  vs Load Current (Output Sinking)

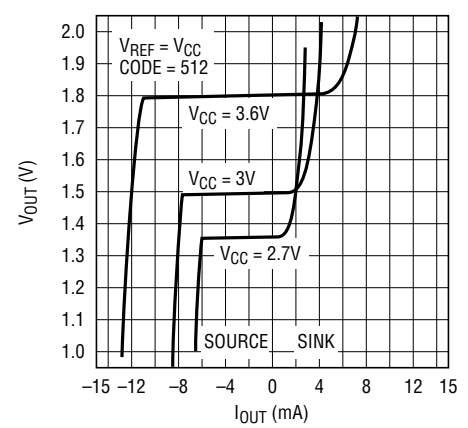
1661 G04

Mid-Scale Output Voltage vs Load Current



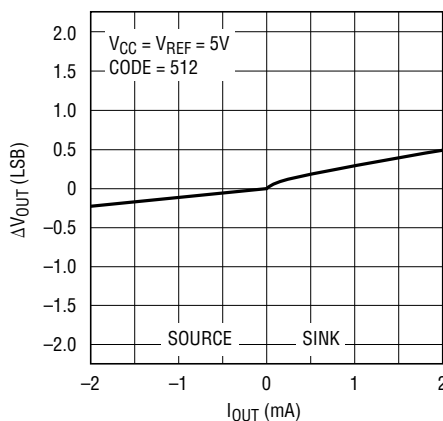
1661 G05

Mid-Scale Output Voltage vs Load Current



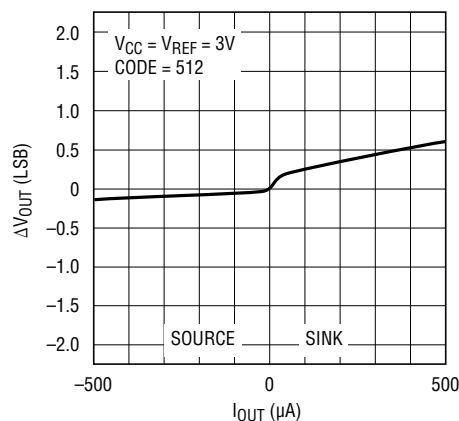
1661 G06

Load Regulation vs Output Current



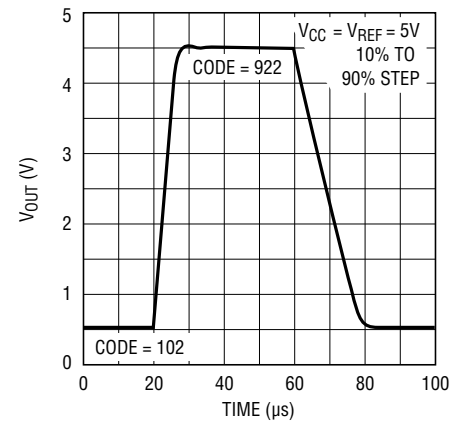
1661 G07

Load Regulation vs Output Current



1661 G08

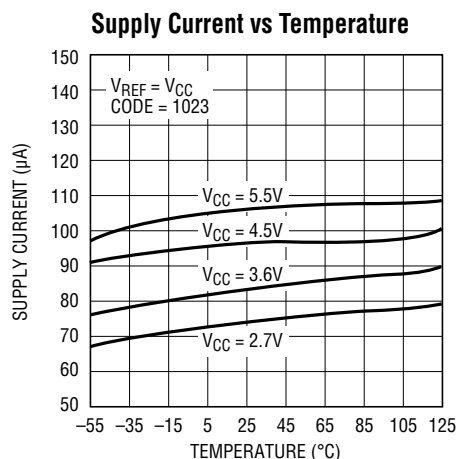
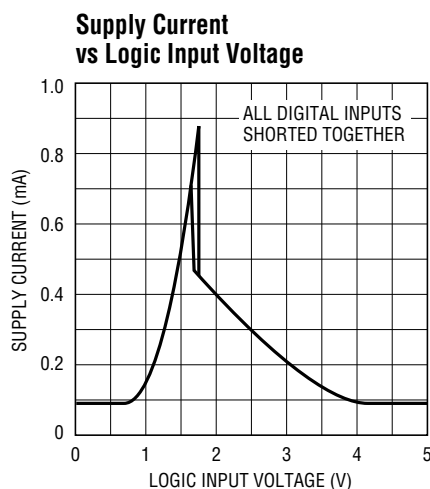
Large-Signal Step Response



1661 G09

1661fb

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**$\overline{\text{CS/LD}}$  (Pin 1):** Serial Interface Chip Select/Load Input. When  $\overline{\text{CS/LD}}$  is low, SCK is enabled for shifting data on  $D_{\text{IN}}$  into the register. When  $\overline{\text{CS/LD}}$  is pulled high, SCK is disabled and the operation(s) specified in the control code, A3-A0, is (are) performed. CMOS and TTL compatible.

**SCK (Pin 2):** Serial Interface Clock Input. CMOS and TTL compatible.

**$D_{\text{IN}}$  (Pin 3):** Serial Interface Data Input. Input word data on the  $D_{\text{IN}}$  pin is shifted into the 16-bit register on the rising edge of SCK. CMOS and TTL compatible.

**REF (Pin 4):** Reference Voltage Input.  $0V \leq V_{\text{REF}} \leq V_{\text{CC}}$ .

**$V_{\text{OUTA}}$ ,  $V_{\text{OUTB}}$  (Pin 8, Pin 5):** DAC Analog Voltage Outputs. The output range is

$$0 \leq V_{\text{OUTA}}, V_{\text{OUTB}} \leq V_{\text{REF}} \left( \frac{1023}{1024} \right)$$

**$V_{\text{CC}}$  (Pin 6):** Supply Voltage Input.  $2.7V \leq V_{\text{CC}} \leq 5.5V$ .

**GND (Pin 7):** System Ground.

## DEFINITIONS

**Differential Nonlinearity (DNL):** The difference between the measured change and the ideal 1LSB change for any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$\text{DNL} = \frac{\Delta V_{\text{OUT}} - \text{LSB}}{\text{LSB}}$$

where  $\Delta V_{\text{OUT}}$  is the measured voltage difference between two adjacent codes.

**Full-Scale Error (FSE):** The deviation of the actual full-scale voltage from ideal. FSE includes the effects of offset and gain errors (see Applications Information).

**Integral Nonlinearity (INL):** The deviation from a straight line passing through the endpoints of the DAC transfer curve (endpoint INL). Because the output cannot go below zero, the linearity is measured between full scale and the lowest code which guarantees the output will be greater than zero. The INL error at a given input code is calculated as follows:

$$\text{INL} = \frac{V_{\text{OUT}} - V_{\text{OS}} - (V_{\text{FS}} - V_{\text{OS}}) \left( \frac{\text{Code}}{1023} \right)}{\text{LSB}}$$

where  $V_{\text{OUT}}$  is the output voltage of the DAC measured at the given input code.

**Least Significant Bit (LSB):** The ideal voltage difference between two successive codes.

$$\text{LSB} = \frac{V_{\text{REF}}}{1024}$$

**Resolution (n):** Defines the number of DAC output states ( $2^n$ ) that divide the full-scale range. Resolution does not imply linearity.

**Voltage Offset Error ( $V_{\text{OS}}$ ):** Nominally, the voltage at the output when the DAC is loaded with all zeros. A single supply DAC can have a true negative offset, but the output cannot go below zero (see Applications Information).

For this reason, single supply DAC offset is measured at the lowest code that guarantees the output will be greater than zero.

## OPERATION

### Transfer Function

The transfer function for the LTC1661 is:

$$V_{\text{OUT(DEAL)}} = \left( \frac{k}{1024} \right) V_{\text{REF}}$$

where  $k$  is the decimal equivalent of the binary DAC input code D9-D0 and  $V_{\text{REF}}$  is the voltage at REF (Pin 6).

### Power-On Reset

The LTC1661 positively clears the outputs to zero scale when power is first applied, making system initialization consistent and repeatable.

### Power Supply Sequencing

The voltage at REF (Pin 4) must not ever exceed the voltage at  $V_{\text{CC}}$  (Pin 6) by more than 0.3V. Particular care should be taken in the power supply turn-on and turn-off sequences to assure that this limit is observed. See Absolute Maximum Ratings.

### Serial Interface

See Table 1. The 16-bit Input word consists of the 4-bit Control code, the 10-bit Input code and two don't-care bits.

**Table 1. LTC1661 Input Word**

| INPUT WORD   |    |    |    |            |    |    |    |    |    |    |    |    |    |            |    |
|--------------|----|----|----|------------|----|----|----|----|----|----|----|----|----|------------|----|
| A3           | A2 | A1 | A0 | D9         | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | X1         | X0 |
| CONTROL CODE |    |    |    | INPUT CODE |    |    |    |    |    |    |    |    |    | DON'T CARE |    |

After the Input word is loaded into the register (see Figure 1), it is internally converted from serial to parallel format. The parallel 10-bit-wide input code data path is then buffered by two latch registers.

The first of these, the input register, is used for loading new input codes. The second buffer, the DAC register, is used for updating the DAC outputs. Each DAC has its own 10-bit input register and 10-bit DAC register.

By selecting the appropriate 4-bit control code (see Table 2) it is possible to perform single operations, such as loading one DAC or changing power-down status (sleep/wake). In addition, some Control codes perform two or more operations at the same time. For example, one such code loads DAC A, updates both outputs and wakes the part up. The DACs can be loaded separately or together, but the outputs are always updated together.

### Register Loading Sequence

See Figure 1. With  $\overline{\text{CS/LD}}$  held low, data on the  $D_{\text{IN}}$  input is shifted into the 16-bit shift register on the positive edge of SCK. The 4-bit control code, A3-A0, is loaded first, then the 10-bit Input code, D9-D0, ordered MSB-to-LSB in each case. Two don't-care bits, X1 and X0, are loaded last. When the full 16-bit Input word has been shifted in,  $\overline{\text{CS/LD}}$  is pulled high, causing the system to respond according to Table 2. The clock is disabled internally when  $\overline{\text{CS/LD}}$  is high. Note: SCK must be low when  $\overline{\text{CS/LD}}$  is pulled low.

### Sleep Mode

DAC control code 1110<sub>b</sub> is reserved for the special sleep instruction (see Table 2). In this mode, the digital parts of the circuit stay active while the analog sections are disabled; static power consumption is greatly reduced. The reference input and analog outputs are set in a high impedance state and all DAC settings are retained in memory so that when Sleep mode is exited, the outputs of DACs not updated by the wake command are restored to their last active state.

Sleep mode is initiated by performing a load sequence using control code 1110<sub>b</sub> (the DAC input code D9-D0 is ignored).

To save instruction cycles, the DACs may be prepared with new input codes during Sleep (control codes 0001<sub>b</sub> and 0010<sub>b</sub>); then, a single command (1000<sub>b</sub>) can be used both to wake the part and to update the output values.

## OPERATION

Table 2. DAC Control Functions

| CONTROL |    |    |    | INPUT REGISTER STATUS                | DAC REGISTER STATUS | POWER-DOWN STATUS (SLEEP/WAKE) | COMMENTS                                                                                                                       |
|---------|----|----|----|--------------------------------------|---------------------|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------|
| A3      | A2 | A1 | A0 |                                      |                     |                                |                                                                                                                                |
| 0       | 0  | 0  | 0  | No Change                            | No Update           | No Change                      | No Operation. Power-Down Status Unchanged (Part Stays in Wake or Sleep Mode)                                                   |
| 0       | 0  | 0  | 1  | Load DAC A                           | No Update           | No Change                      | Load Input Register A with Data. DAC Outputs Unchanged. Power-Down Status Unchanged                                            |
| 0       | 0  | 1  | 0  | Load DAC B                           | No Update           | No Change                      | Load Input Register B with Data. DAC Outputs Unchanged. Power-Down Status Unchanged                                            |
| 0       | 0  | 1  | 1  | Reserved                             |                     |                                |                                                                                                                                |
| 0       | 1  | 0  | 0  | Reserved                             |                     |                                |                                                                                                                                |
| 0       | 1  | 0  | 1  | Reserved                             |                     |                                |                                                                                                                                |
| 0       | 1  | 1  | 0  | Reserved                             |                     |                                |                                                                                                                                |
| 0       | 1  | 1  | 1  | Reserved                             |                     |                                |                                                                                                                                |
| 1       | 0  | 0  | 0  | No Change                            | Update Outputs      | Wake                           | Load Both DAC Regs with Existing Contents of Input Regs. Outputs Update. Part Wakes Up                                         |
| 1       | 0  | 0  | 1  | Load DAC A                           | Update Outputs      | Wake                           | Load Input Reg A. Load DAC Regs with New Contents of Input Reg A and Existing Contents of Reg B. Outputs Update. Part Wakes Up |
| 1       | 0  | 1  | 0  | Load DAC B                           | Update Outputs      | Wake                           | Load Input Reg B. Load DAC Regs with Existing Contents of Input Reg A and New Contents of Reg B. Outputs Update. Part Wakes Up |
| 1       | 0  | 1  | 1  | Reserved                             |                     |                                |                                                                                                                                |
| 1       | 1  | 0  | 0  | Reserved                             |                     |                                |                                                                                                                                |
| 1       | 1  | 0  | 1  | No Change                            | No Update           | Wake                           | Part Wakes Up. Input and DAC Regs Unchanged. DAC Outputs Reflect Existing Contents of DAC Regs                                 |
| 1       | 1  | 1  | 0  | No Change                            | No Update           | Sleep                          | Part Goes to Sleep. Input and DAC Regs Unchanged. DAC Outputs Set to High Impedance State                                      |
| 1       | 1  | 1  | 1  | Load DACs A, B with Same 10-Bit Code | Update Outputs      | Wake                           | Load Both Input Regs. Load Both DAC Regs with New Contents of Input Regs. Outputs Update. Part Wakes Up                        |

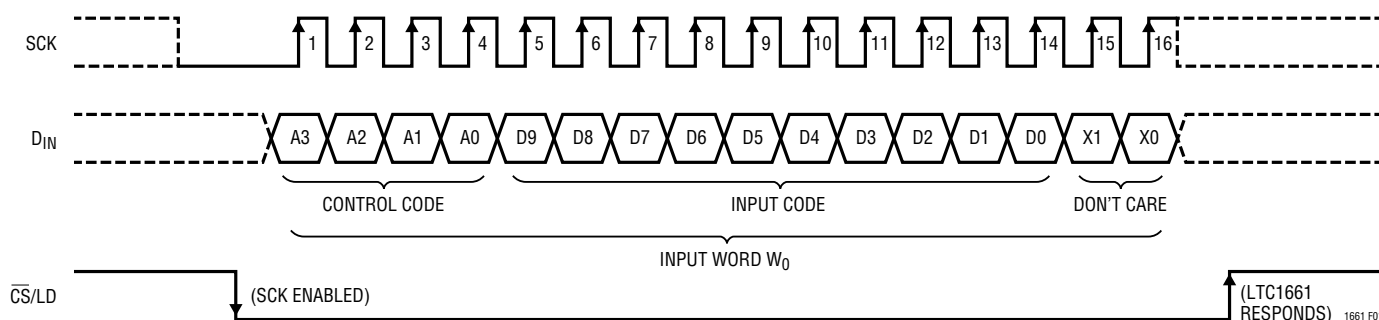


Figure 1. Register Loading Sequence

## OPERATION

### Voltage Outputs

Each of the rail-to-rail output amplifiers contained in the LTC1661 can typically source or sink up to 5mA ( $V_{CC} = 5V$ ). The outputs swing to within a few millivolts of either supply when unloaded and have an equivalent output resistance of 85 $\Omega$  (typical) when driving a load to the rails. The output amplifiers are stable driving capacitive loads up to 1000pF.

A small resistor placed in series with the output can be used to achieve stability for any load capacitance. A 1 $\mu F$  load can be successfully driven by inserting a 20 $\Omega$  resistor in series with the  $V_{OUT}$  pin. A 2.2 $\mu F$  load needs only a 10 $\Omega$  resistor, and a 10 $\mu F$  electrolytic capacitor can be used without any resistor (the equivalent series resistance of the capacitor itself provides the required small resistance). In any of these cases, larger values of resistance, capacitance or both may be substituted for the values given.

### Rail-to-Rail Output Considerations

In any rail-to-rail DAC, the output swing is limited to voltages within the supply range.

If the DAC offset is negative, the output for the lowest codes limits at 0V as shown in Figure 2b.

Similarly, limiting can occur near full scale when the REF pin is tied to  $V_{CC}$ . If  $V_{REF} = V_{CC}$  and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at  $V_{CC}$  as shown in Figure 2c. No full-scale limiting can occur if  $V_{REF}$  is less than  $V_{CC} - FSE$ .

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

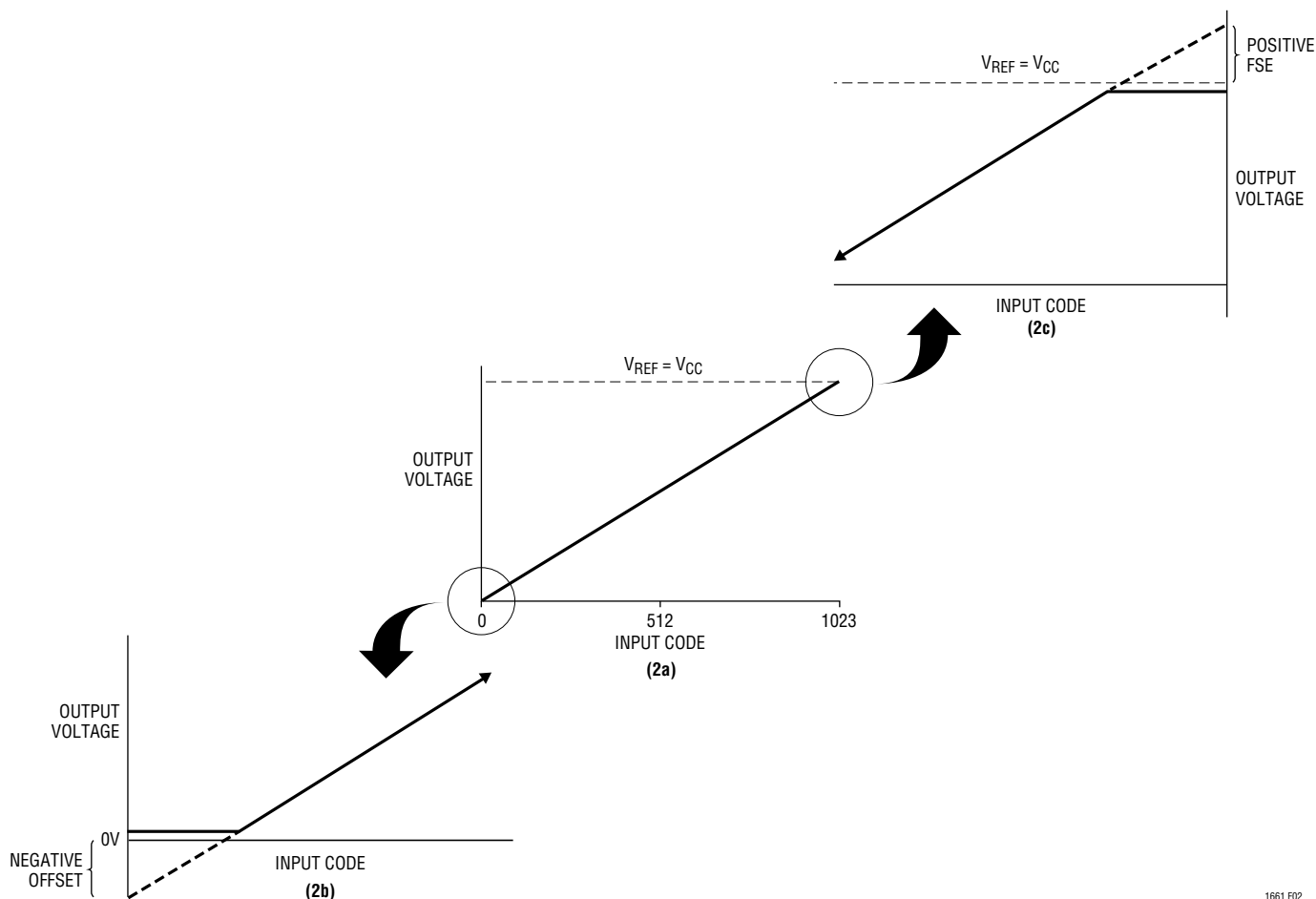


Figure 2. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (2a) Overall Transfer Function (2b) Effect of Negative Offset for Codes Near Zero Scale (2c) Effect of Positive Full-Scale Error for Input Codes Near Full Scale When  $V_{REF} = V_{CC}$

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# TYPICAL APPLICATIONS

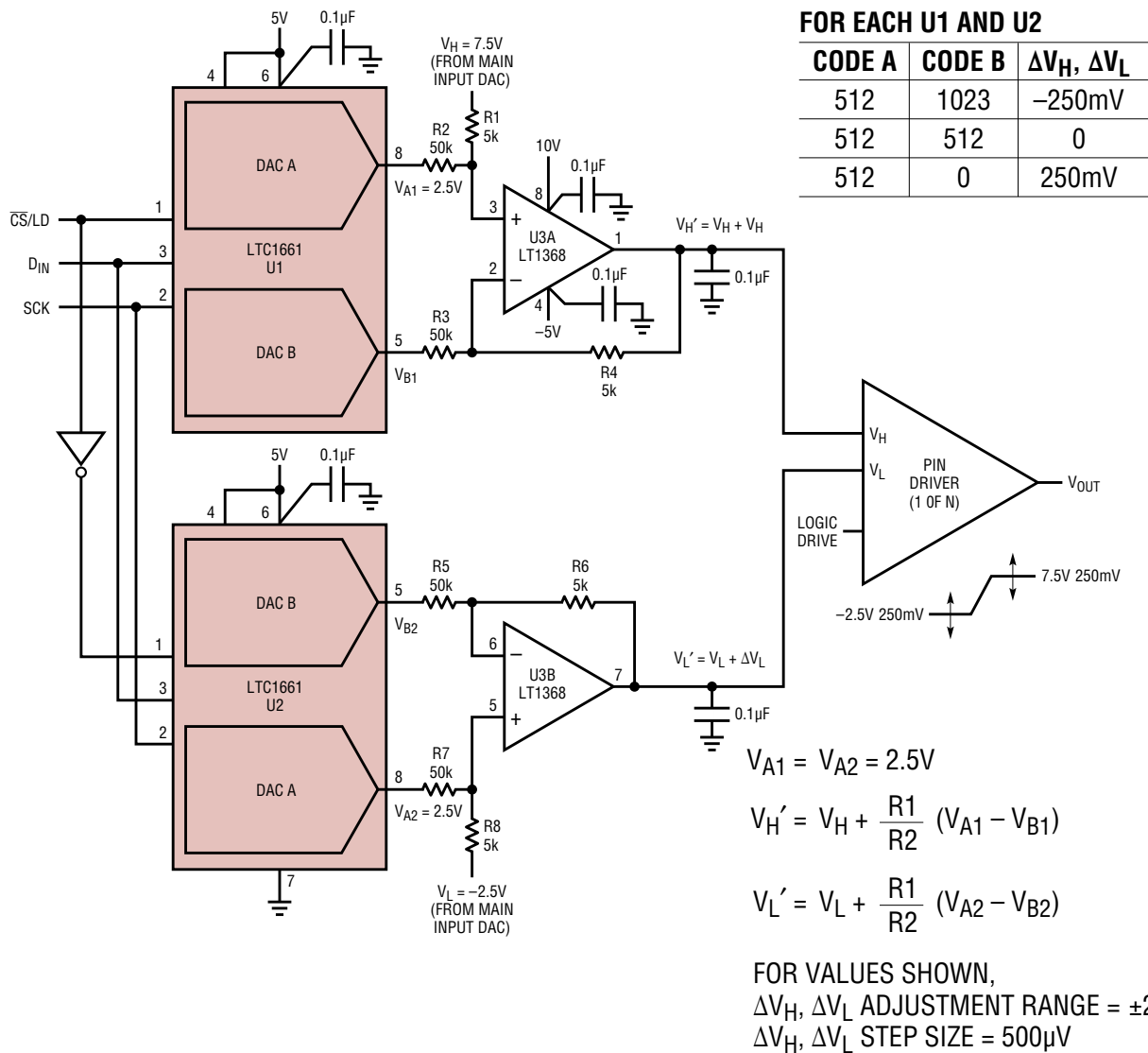


Figure 3. Pin Driver  $V_H$  and  $V_L$  Adjustment in ATE Applications

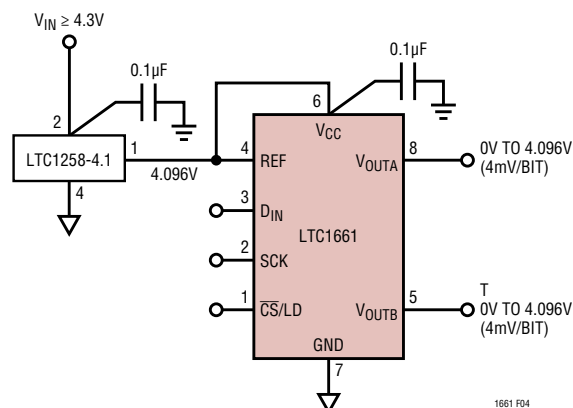


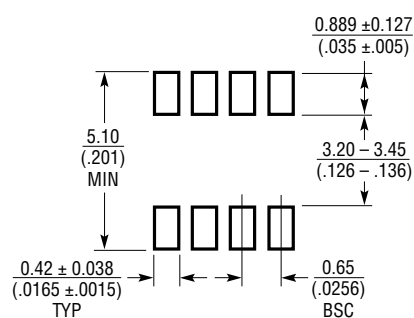
Figure 4. Using the LTC1258 and the LTC1661 In a Single Li-Ion Battery Application

## PACKAGE DESCRIPTION

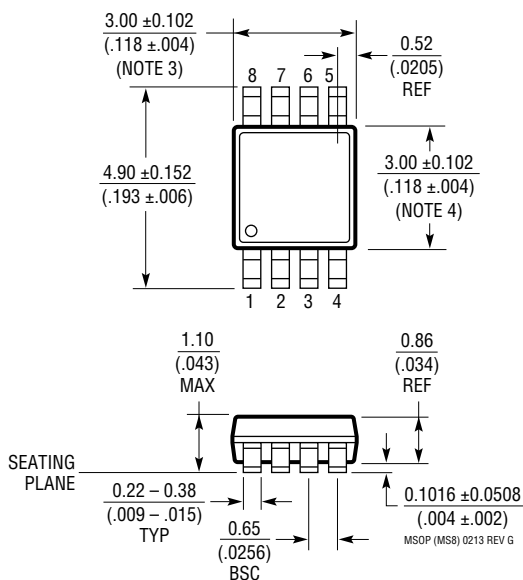
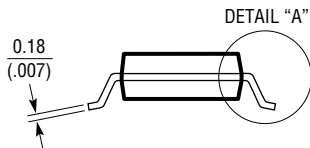
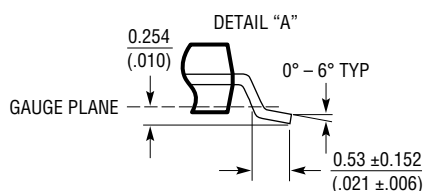
Please refer to <http://www.linear.com/product/LTC1661#packaging> for the most recent package drawings.

### MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev G)



RECOMMENDED SOLDER PAD LAYOUT

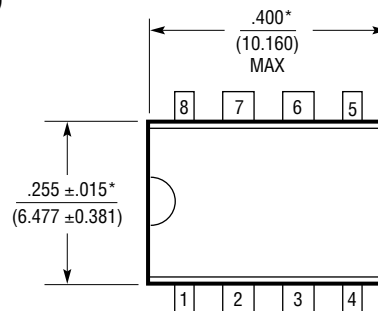
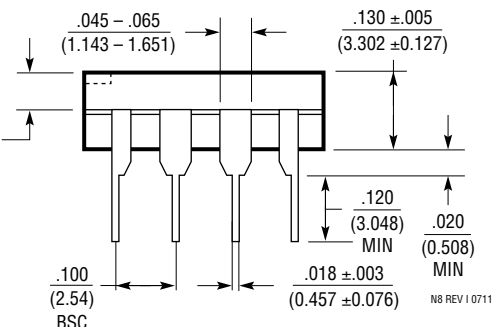
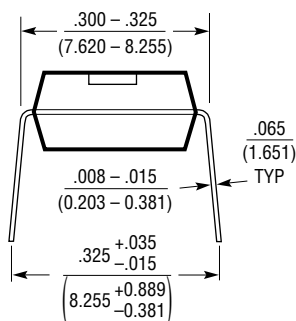


#### NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED  $0.152\text{mm}$  ( $.006$ ) PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED  $0.152\text{mm}$  ( $.006$ ) PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE  $0.102\text{mm}$  ( $.004$ ) MAX

### N Package 8-Lead PDIP (Narrow .300 Inch)

(Reference LTC DWG # 05-08-1510 Rev I)



#### NOTE:

1. DIMENSIONS ARE  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

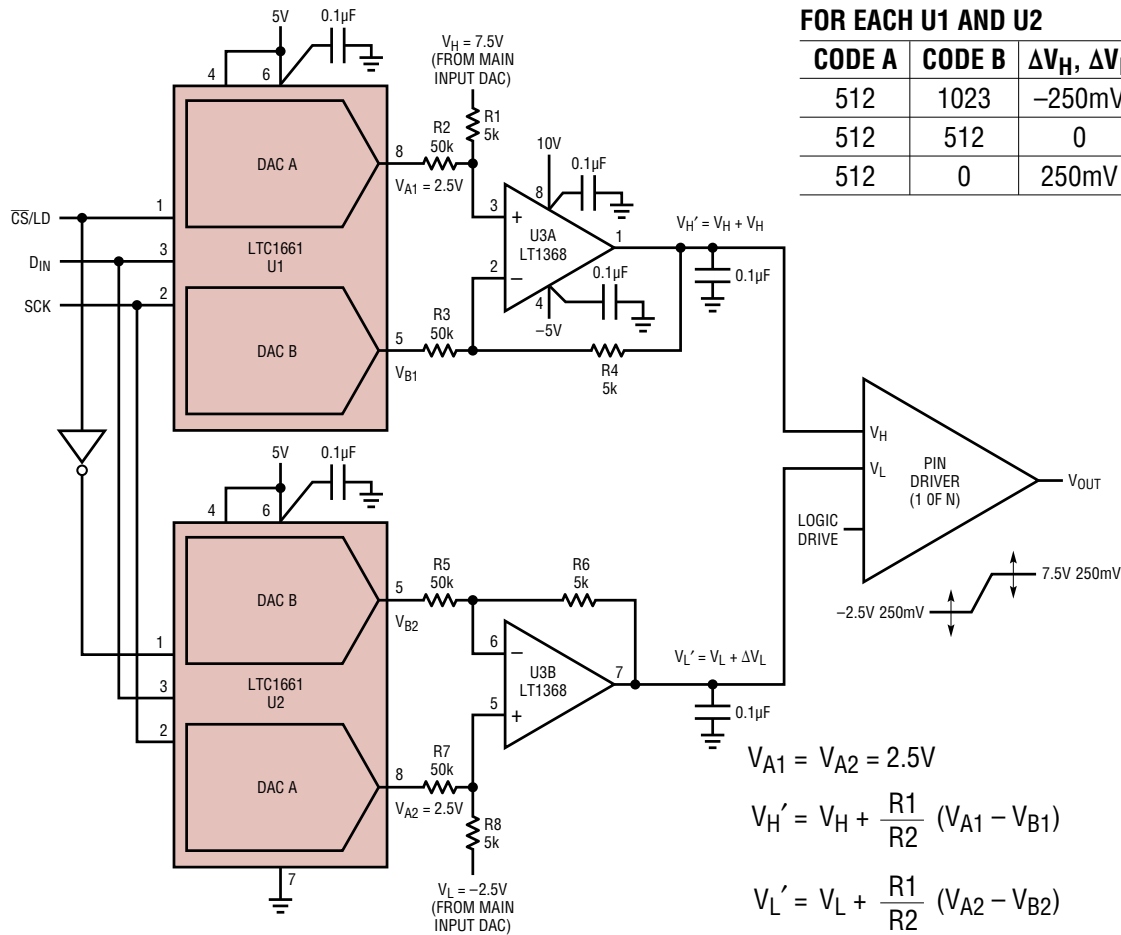
\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED  $0.010$  INCH ( $0.254\text{mm}$ )

## REVISION HISTORY

| REV | DATE  | DESCRIPTION                                                | PAGE NUMBER |
|-----|-------|------------------------------------------------------------|-------------|
| A   | 11/10 | Removed typical values from Timing Characteristics section | 3, 4        |
| B   | 4/16  | Corrected typo for $V_{CC}$ under Power Supply             | 3           |

## TYPICAL APPLICATION

### Pin Driver $V_H$ and $V_L$ Adjustment in ATE Applications



## RELATED PARTS

| PART NUMBER                      | DESCRIPTION                                                                                  | COMMENTS                                                                                                                          |
|----------------------------------|----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| <a href="#">LTC1446/LTC1446L</a> | Dual 12-Bit $V_{OUT}$ DACs in SO-8 Package with Internal Reference                           | LTC1446: $V_{CC} = 4.5V$ to $5.5V$ , $V_{OUT} = 0V$ to $4.095V$<br>LTC1446L: $V_{CC} = 2.7V$ to $5.5V$ , $V_{OUT} = 0V$ to $2.5V$ |
| <a href="#">LTC1448</a>          | Dual 12-Bit $V_{OUT}$ DAC in SO-8 Package                                                    | $V_{CC} = 2.7V$ to $5.5V$ , External Reference Can Be Tied to $V_{CC}$                                                            |
| <a href="#">LTC1454/LTC1454L</a> | Dual 12-Bit $V_{OUT}$ DACs in SO-16 Package with Added Functionality                         | LTC1454: $V_{CC} = 4.5V$ to $5.5V$ , $V_{OUT} = 0V$ to $4.095V$<br>LTC1454L: $V_{CC} = 2.7V$ to $5.5V$ , $V_{OUT} = 0V$ to $2.5V$ |
| <a href="#">LTC1458/LTC1458L</a> | Quad 12-Bit Rail-to-Rail Output DACs with Added Functionality                                | LTC1458: $V_{CC} = 4.5V$ to $5.5V$ , $V_{OUT} = 0V$ to $4.095V$<br>LTC1458L: $V_{CC} = 2.7V$ to $5.5V$ , $V_{OUT} = 0V$ to $2.5V$ |
| <a href="#">LTC1659</a>          | Single Rail-to-Rail 12-Bit $V_{OUT}$ DAC in 8-Lead MSOP Package<br>$V_{CC} = 2.7V$ to $5.5V$ | Low Power Multiplying $V_{OUT}$ DAC. Output Swings from GND to REF. REF Input Can Be Tied to $V_{CC}$                             |
| <a href="#">LTC1663</a>          | Single 10-Bit $V_{OUT}$ DAC in SOT-23 Package                                                | $V_{CC} = 2.7V$ to $5.5V$ , Internal Reference, $60\mu A$                                                                         |
| <a href="#">LTC1665/LTC1660</a>  | Octal 8/10-Bit $V_{OUT}$ DAC in 16-Pin Narrow SSOP                                           | $V_{CC} = 2.7V$ to $5.5V$ , Micropower, Rail-to-Rail Output                                                                       |

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