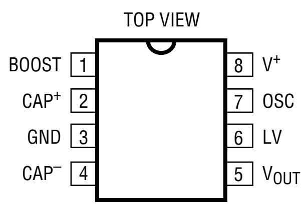
ABSOLUTE MAXIMUM RATINGS

(Note 1)

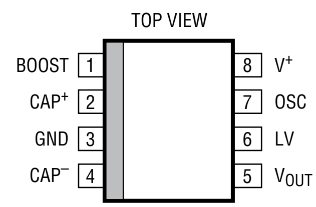
Supply Voltage 13V
Input Voltage on Pins 1, 6 and 7
(Note 2) .... –0.3V < V_{IN} < V^+ + 0.3V
Current into Pin 6 .... 20μA
Output Short-Circuit Duration
$V^+ \leq 6.5V$ .... Continuous

Operating Temperature Range
LTC1044AC .... 0°C to 70°C
LTC1044AI .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PIN CONFIGURATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 110°C, θ_{JA} = 100°C/W



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 110°C, θ_{JA} = 130°C/W

Consult factory for military grade parts

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1044ACN8#PBF	LTC1044ACN8#TRPBF	LTC1044 ACN8	8-Lead Plastic DIP	0°C to 70°C
LTC1044AIN8#PBF	LTC1044AIN8#TRPBF	LTC1044 AIN8	8-Lead Plastic DIP	–40°C to 85°C
LTC1044ACS8#PBF	LTC1044ACS8#TRPBF	1044A	8-Lead Plastic SO	0°C to 70°C
LTC1044AIS8#PBF	LTC1044AIS8#TRPBF	1044AI	8-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, C_{OSC} = 0pF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1044AC MIN	LTC1044AC TYP	LTC1044AC MAX	LTC1044AI MIN	LTC1044AI TYP	LTC1044AI MAX	UNITS
I_S	Supply Current	R_L = ∞, Pins 1 and 7, No Connection R_L = ∞, Pins 1 and 7, No Connection, V^+ = 3V			60 15	200		60 15	200	μA μA
	Minimum Supply Voltage	R_L = 10k	●	1.5			1.5			V
	Maximum Supply Voltage	R_L = 10k	●			12			12	V
R_{OUT}	Output Resistance	I_L = 20mA, f_{OSC} = 5kHz V^+ = 2V, I_L = 3mA, f_{OSC} = 1kHz	 ● ●			100 120 310			100 130 325	Ω Ω Ω
f_{OSC}	Oscillator Frequency	V^+ = 5V, (Note 3) V^+ = 2V	● ●	5 1			5 1			kHz kHz
P_{EFF}	Power Efficiency	RL = 5k, f_{OSC} = 5kHz		95	98		95	98		%
	Voltage Conversion Efficiency	RL = ∞		97	99.9		97	99.9		%
	Oscillator Sink or Source Current	V_{OSC} = 0V or V^+ Pin 1 (BOOST) = 0V Pin 1 (BOOST) = V^+	 ● ●			 3 20			 3 20	 μA μA

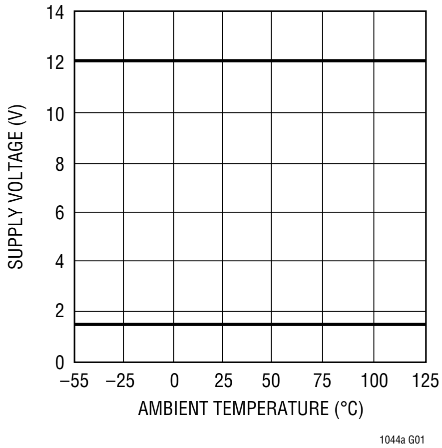
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044A.

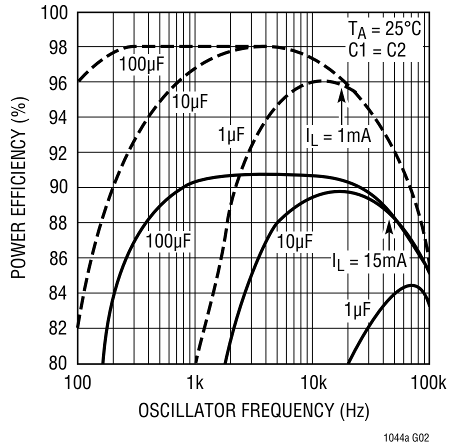
Note 3: f_{OSC} is tested with C_{OSC} = 100pF to minimize the effects of test fixture capacitance loading. The 0pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

TYPICAL PERFORMANCE CHARACTERISTICS

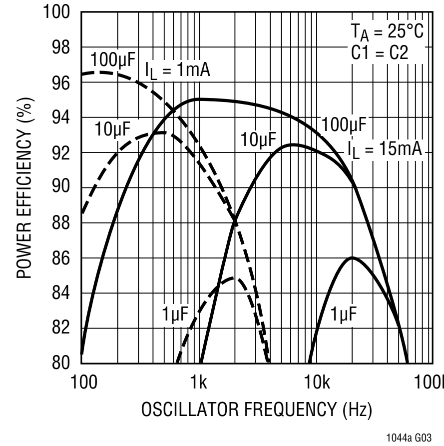
Operating Voltage Range vs Temperature



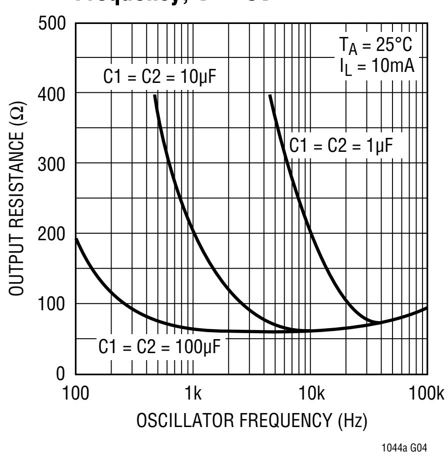
Power Efficiency vs Oscillator Frequency, V^+ = 5V



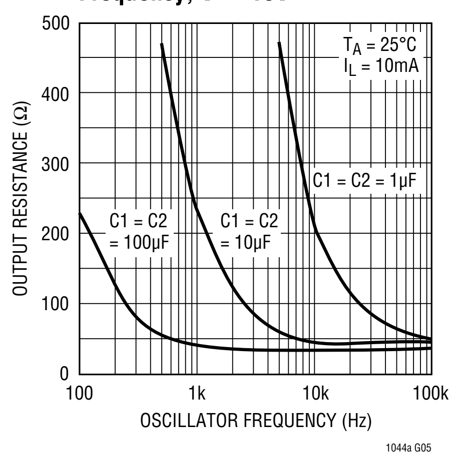
Power Efficiency vs Oscillator Frequency, V^+ = 10V



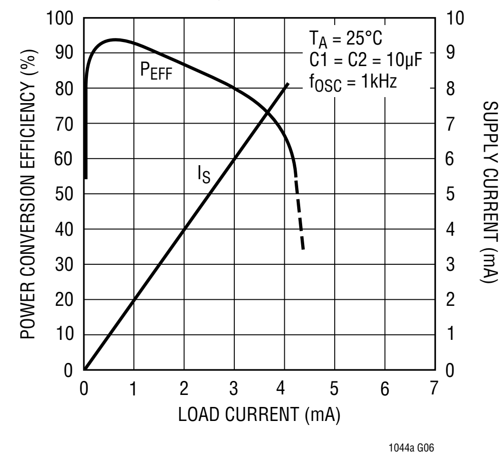
Output Resistance vs Oscillator Frequency, V^+ = 5V



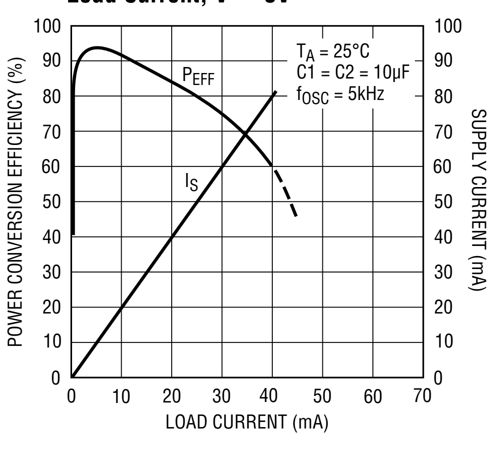
Output Resistance vs Oscillator Frequency, V^+ = 10V



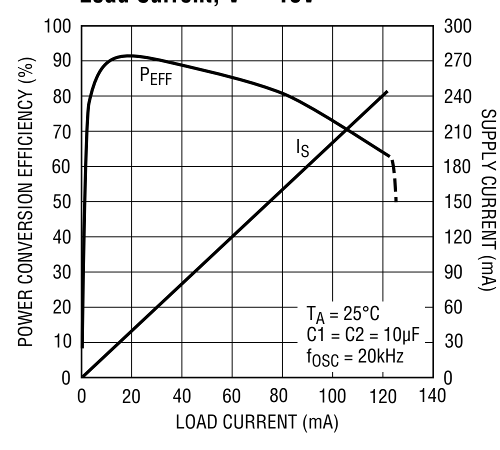
Power Conversion Efficiency vs Load Current, V^+ = 2V



Power Conversion Efficiency vs Load Current, V^+ = 5V

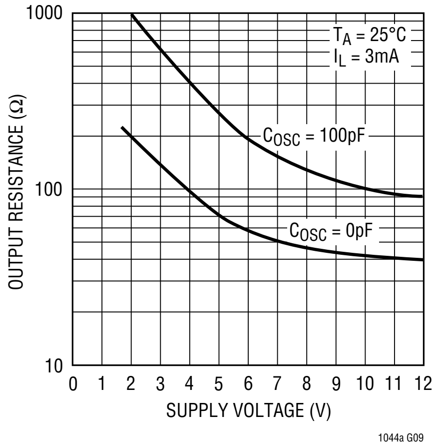


Power Conversion Efficiency vs Load Current, V^+ = 10V

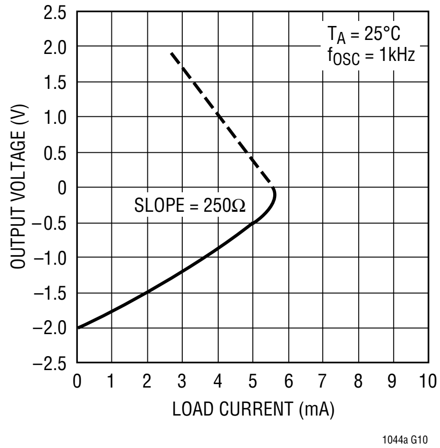


TYPICAL PERFORMANCE CHARACTERISTICS

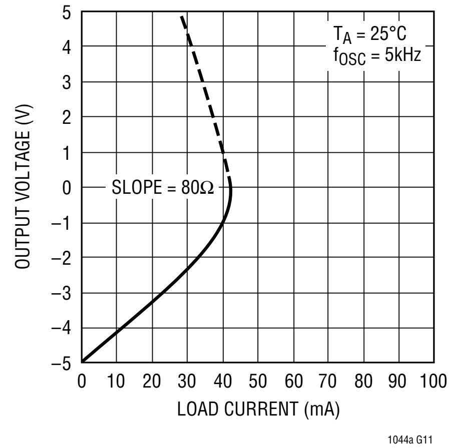
Output Resistance vs Supply Voltage



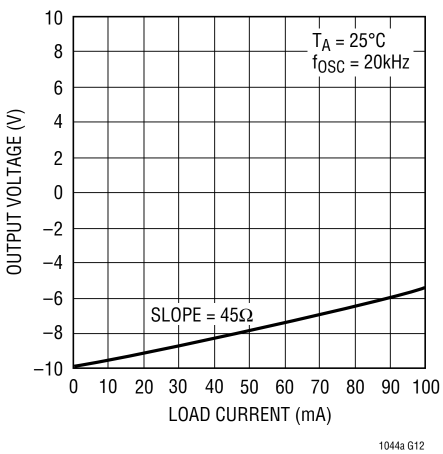
Output Voltage vs Load Current, $V^+ = 2V$



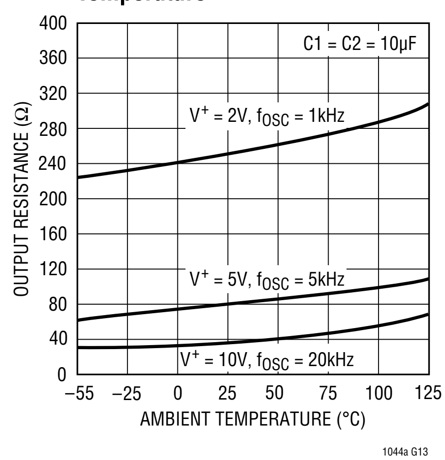
Output Voltage vs Load Current, $V^+ = 5V$



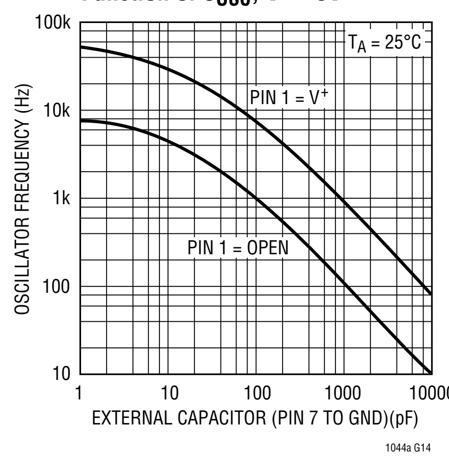
Output Voltage vs Load Current, $V^+ = 10V$



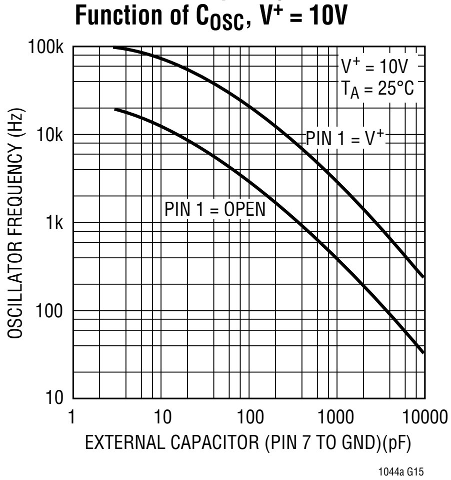
Output Resistance vs Temperature



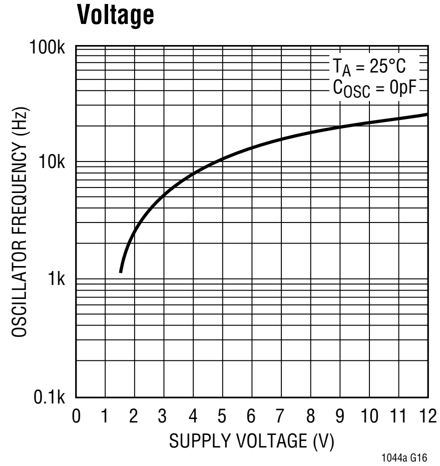
Oscillator Frequency as a Function of C_{OSC}, $V^+ = 5V$



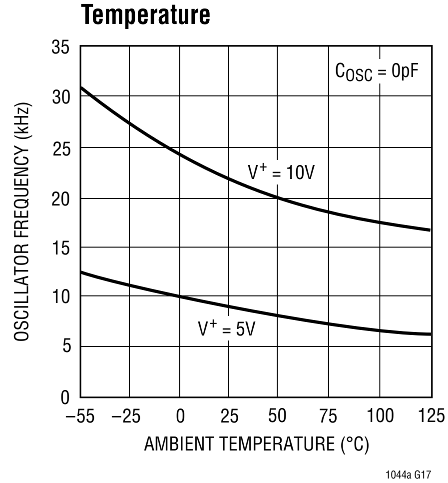
Oscillator Frequency as a Function of C_{OSC}, $V^+ = 10V$



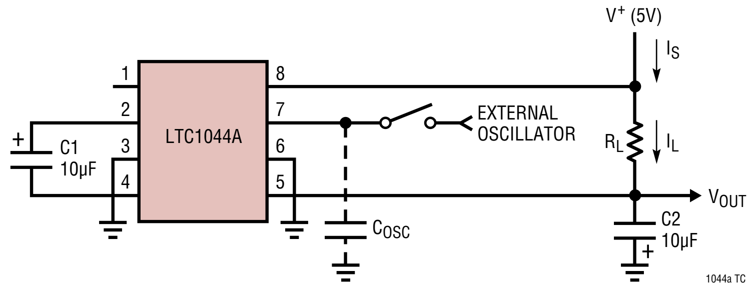
Oscillator Frequency vs Supply Voltage



Oscillator Frequency vs Temperature



TEST CIRCUIT



APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LTC1044A, a review of a basic switched-capacitor building block is helpful.

In Figure 1, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \bullet \Delta q = f \bullet C1(V1 - V2)$$

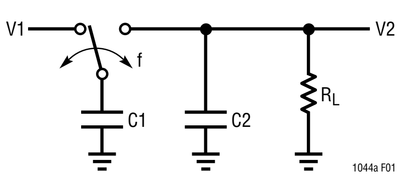


Figure 1. Switched-Capacitor Building Block

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{\frac{1}{(f \bullet C1)}} = \frac{V1 - V2}{R_{EQUIV}}$$

A new variable, R_{EQUIV}, has been defined such that $R_{EQUIV} = 1/(f \bullet C1)$. Thus, the equivalent circuit for the switched-capacitor network is as shown in Figure 2.

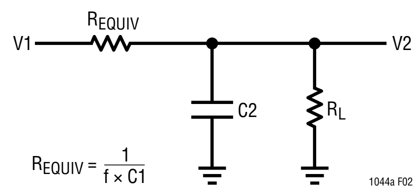


Figure 2. Switched-Capacitor Equivalent Circuit

Examination of Figure 3 shows that the LTC1044A has the same switching action as the basic switched-capacitor building block. With the addition of finite switch-on resistance and output voltage ripple, the simple theory although not exact, provides an intuitive feel for how the device works.

For example, if you examine power conversion efficiency as a function of frequency (see typical curve), this simple theory will explain how the LTC1044A behaves. The loss, and hence the efficiency, is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the $1/(f \bullet C1)$ term, and power efficiency will drop. The typical curves for Power Efficiency vs Frequency show this effect for various capacitor values.

Note also that power efficiency decreases as frequency goes up. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and the power efficiency starts to decrease.

APPLICATIONS INFORMATION

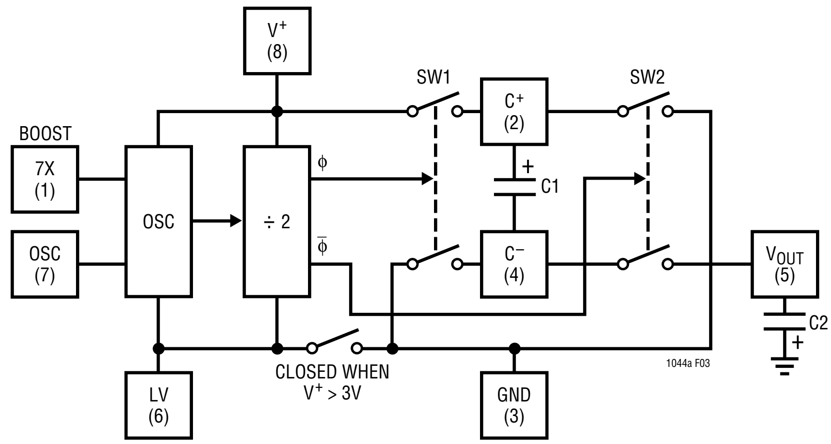


Figure 3. LTC1044A Switched-Capacitor Voltage Converter Block Diagram

LV (Pin 6)

The internal logic of the LTC1044A runs between V+ and LV (pin 6). For V+ greater than or equal to 3V, an internal switch shorts LV to GND (pin 3). For V+ less than 3V, the LV pin should be tied to GND. For V+ greater than or equal to 3V, the LV pin can be tied to GND or left floating.

OSC (Pin 7) and Boost (Pin 1)

The switching frequency can be raised, lowered, or driven from an external source. Figure 4 shows a functional diagram of the oscillator circuit.

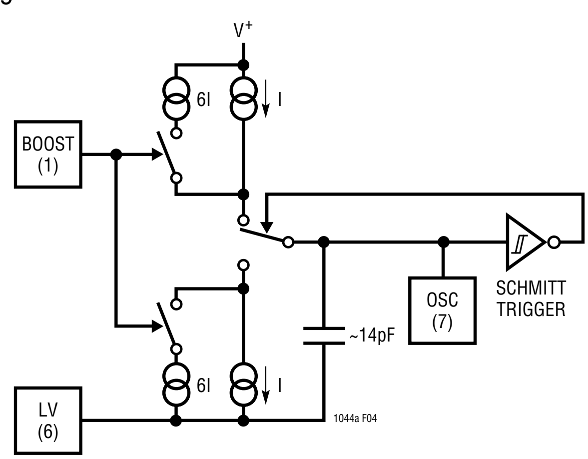


Figure 4. Oscillator

By connecting the boost pin (pin 1) to V+, the charge and discharge current is increased and hence, the frequency is increased by approximately seven times. Increasing the frequency will decrease output impedance and ripple for higher load currents.

Loading pin 7 with more capacitance will lower the frequency. Using the boost (pin 1) in conjunction with external capacitance on pin 7 allows user selection of the frequency over a wide range.

Driving the LTC1044A from an external frequency source can be easily achieved by driving pin 7 and leaving the boost pin open as shown in Figure 5. The output current from pin 7 is small (typically 0.5μA) so a logic gate is capable of driving this current. The choice of using a CMOS logic gate is best because it can operate over a wide supply voltage range (3V to 15V) and has enough voltage swing to drive the internal Schmitt trigger shown in Figure 4. For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 5).

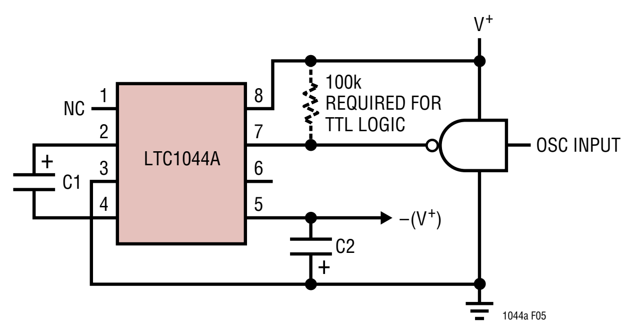


Figure 5. External Clocking

For more information www.linear.com/LTC1044A

APPLICATIONS INFORMATION

Capacitor Selection

External capacitors C1 and C2 are not critical. Matching is not required, nor do they have to be high quality or tight tolerance. Aluminum or tantalum electrolytics are excellent choices with cost and size being the only consideration.

Negative Voltage Converter

Figure 6 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges *without* the need of any external diodes. The LV pin (pin 6) is shown grounded, but for $V^+ \geq 3V$ it may be *floated*, since LV is internally switched to ground (pin 3) for $V^+ \geq 3V$.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with an 80Ω resistor. The 80Ω output impedance is composed of two terms:

1. The equivalent switched-capacitor resistance (see Theory of Operation).
2. A term related to the on-resistance of the MOS switches.

At an oscillator frequency of 10kHz and C1 = 10µF, the first term is:

$$R_{EQUIV} = \frac{1}{(f_{OSC}/2) \bullet C1}$$

$$= \frac{1}{5 \bullet 10^3 \bullet 10 \bullet 10^{-6}} = 20\Omega$$

Notice that the above equation for R_{EQUIV} is *not* a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

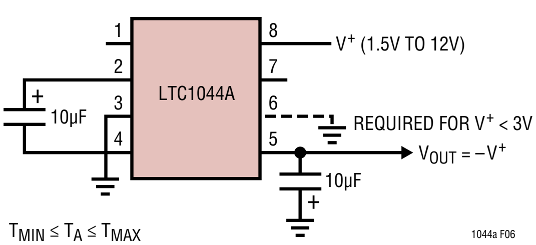


Figure 6. Negative Voltage Converter

The exact expression for output resistance is extremely complex, but the dominant effect of the capacitor is clearly shown on the typical curves of Output Resistance and Power Efficiency vs Frequency. For C1 = C2 = 10µF, the output impedance goes from 60Ω at f_{OSC} = 10kHz to 200Ω at f_{OSC} = 1kHz. As the $1/(f \bullet C)$ term becomes large compared to the switch-on resistance term, the output resistance is determined by $1/(f \bullet C)$ only.

Voltage Doubling

Figure 7 shows a two-diode capacitive voltage doubler. With a 5V input, the output is 9.93V with no load and 9.13V with a 10mA load. With a 10V input, the output is 19.93V with no load and 19.28V with a 10mA load.

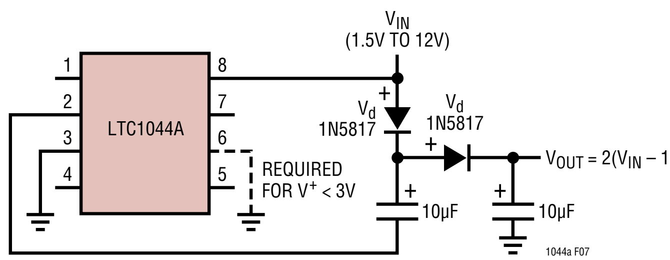


Figure 7. Voltage Doubler

Ultra-Precision Voltage Divider

An ultra-precision voltage divider is shown in Figure 8. To achieve the 0.002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy the load current can be increased.

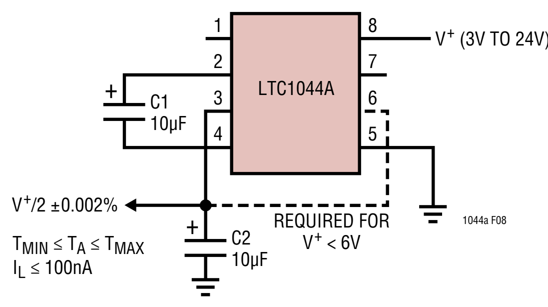


Figure 8. Ultra-Precision Voltage Divider

APPLICATIONS INFORMATION

Battery Splitter

A common need in many systems is to obtain (+) and (–) supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 9 is a simple solution. It provides symmetrical ± output voltages, both equal to one half input voltage. The output voltages are both referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 is less than 6V, pin 6 should also be connected to pin 3 as shown by the dashed line.

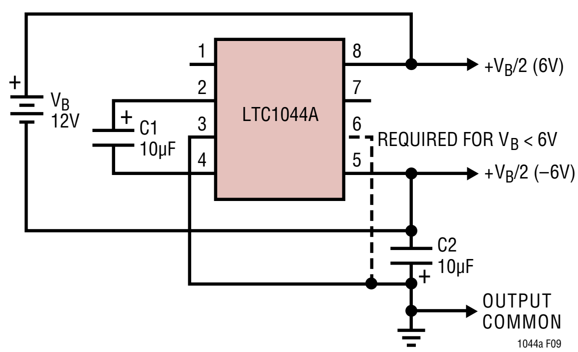


Figure 9. Battery Splitter

Paralleling for Lower Output Resistance

Additional flexibility of the LTC1044A is shown in Figures 10 and 11.

Figure 10 shows two LTC1044As connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by 1/(f•C1), increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

Figure 11 makes use of *stacking* two LTC1044As to provide even higher voltages. A negative voltage doubler or tripler can be achieved, depending upon how pin 8 of the second LTC1044A is connected, as shown schematically by the switch. The available output current will be dictated/decreased by the product of the individual power conversion efficiencies and the voltage step-up ratio.

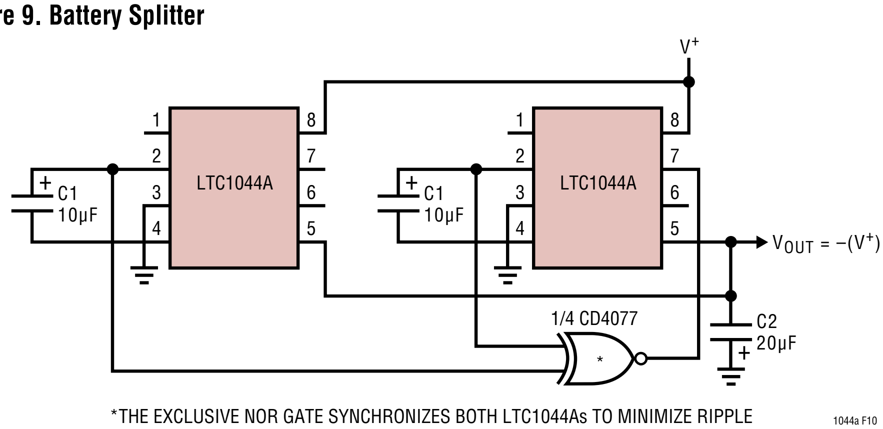


Figure 10. Paralleling for Lower Output Resistance

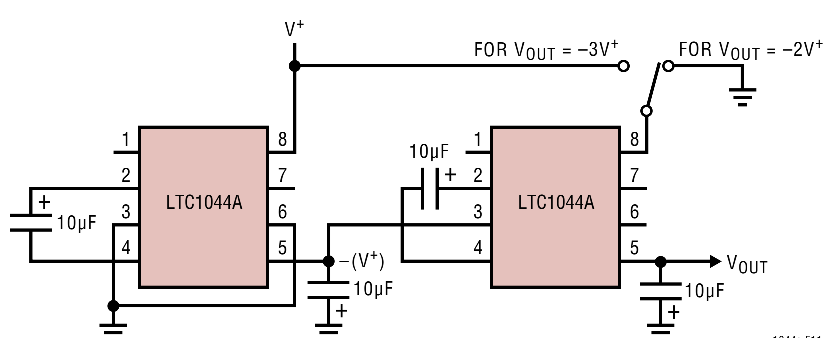
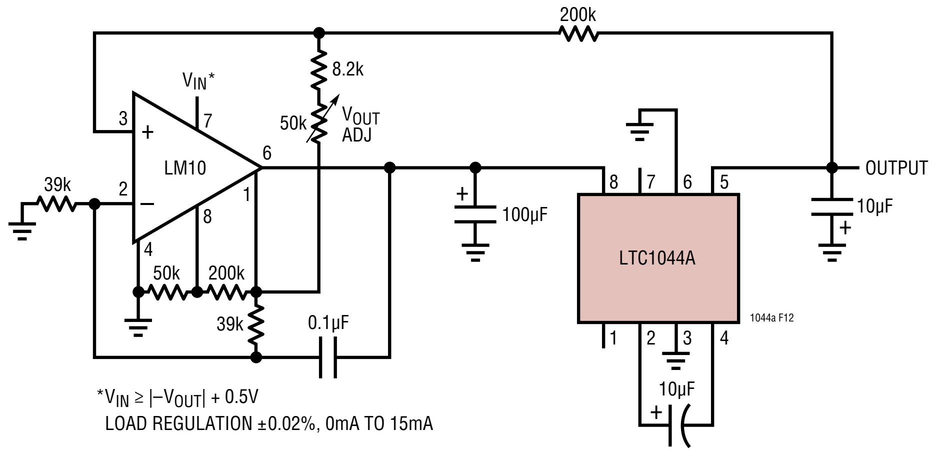


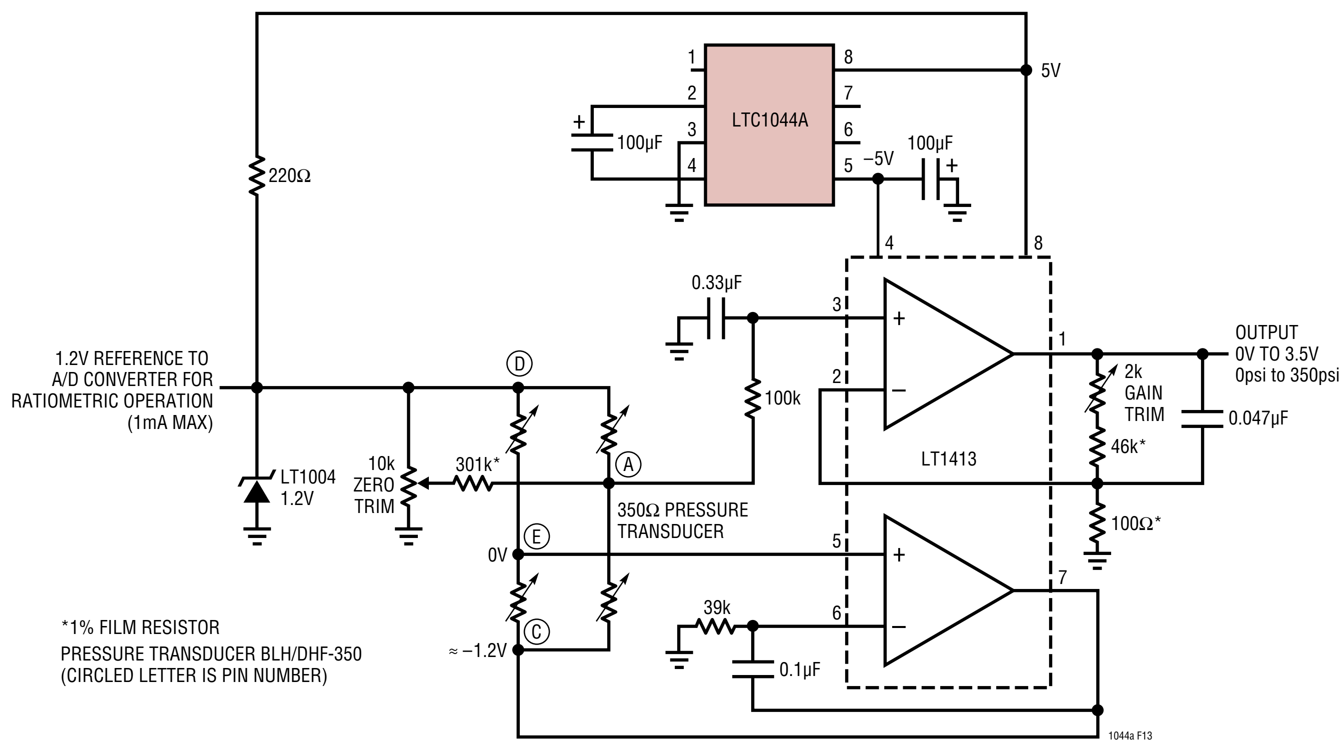
Figure 11. Stacking for Higher Voltage

TYPICAL APPLICATIONS

Low Output Impedance Voltage Converter

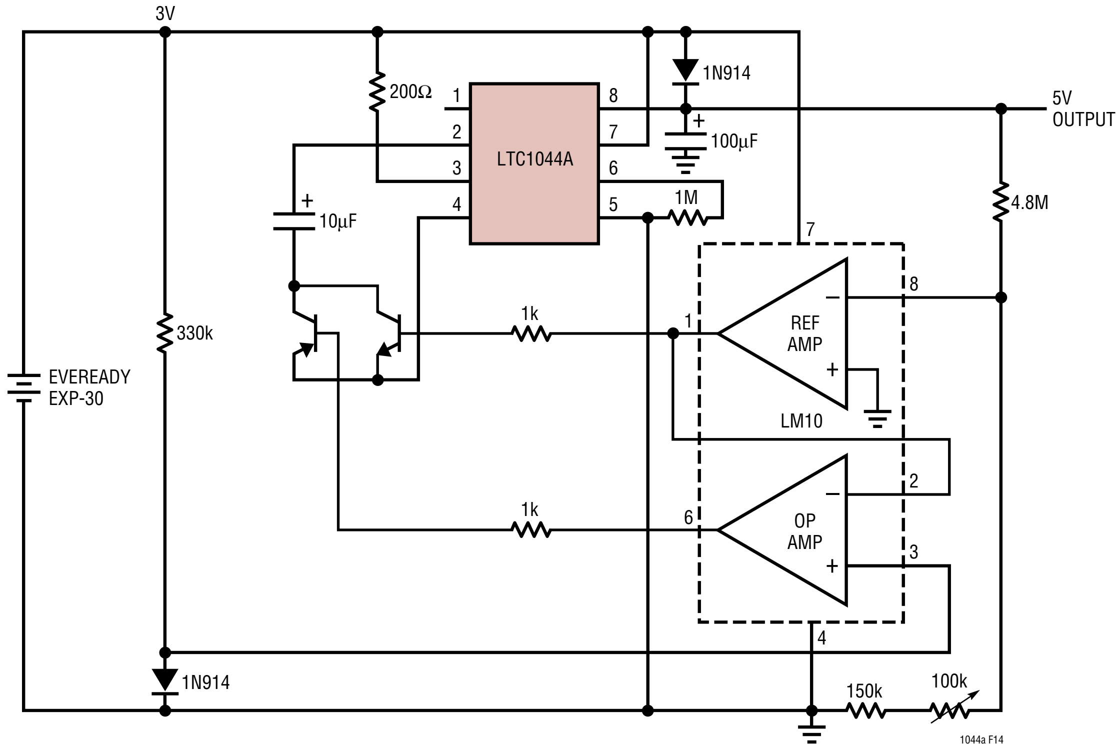


Single 5V Strain Gauge Bridge Signal Conditioner

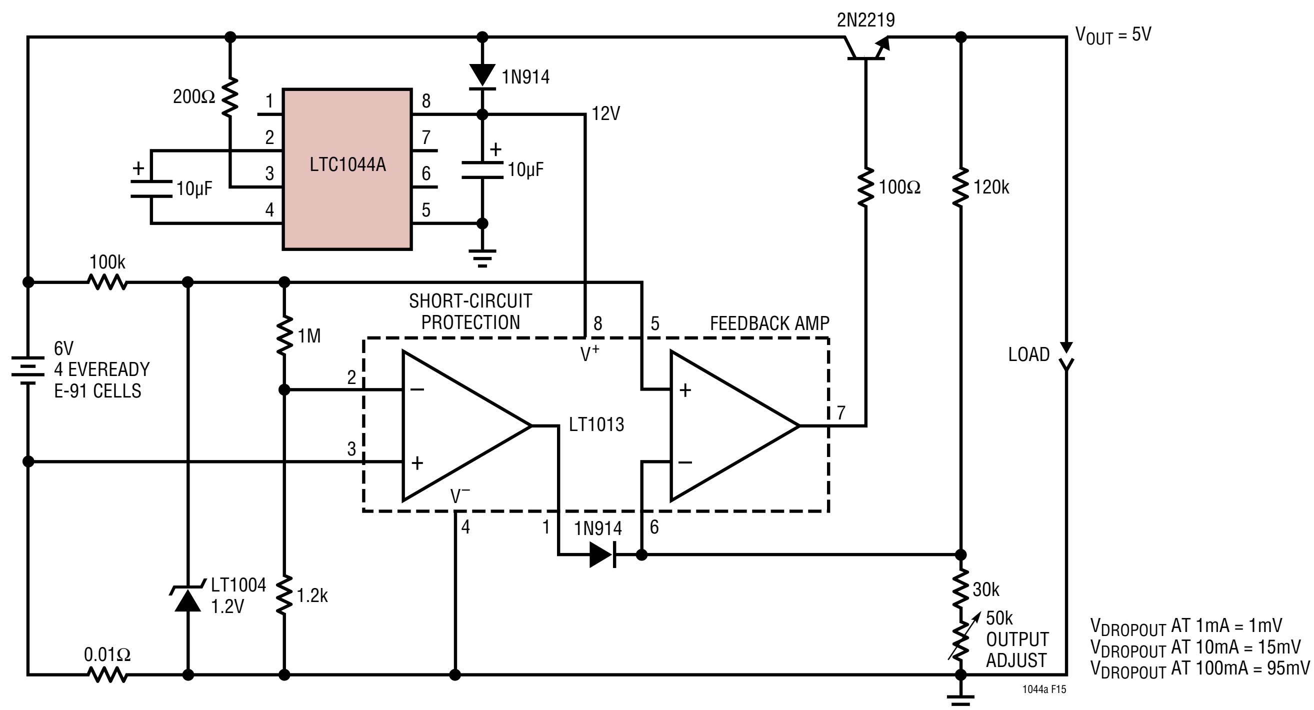


TYPICAL APPLICATIONS

Regulated Output 3V to 5V Converter



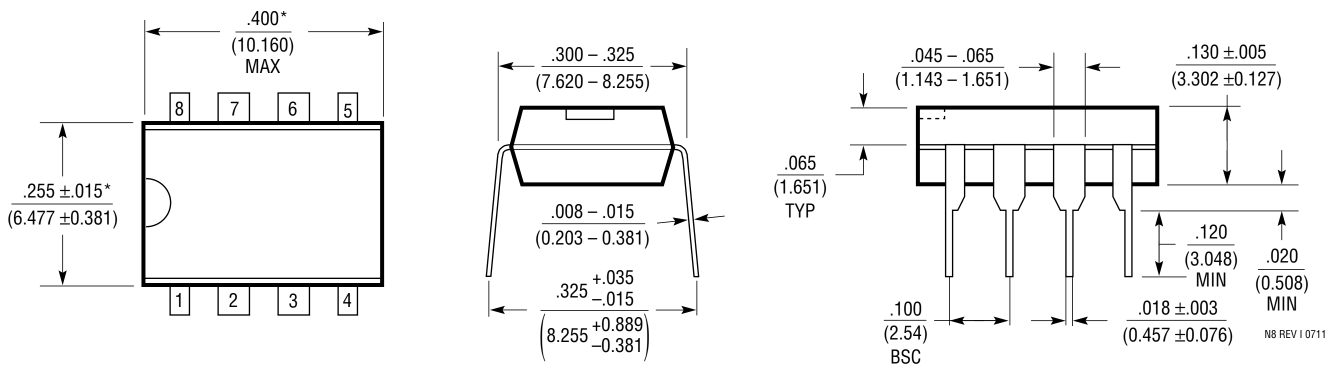
Low Dropout 5V Regulator



PACKAGE DESCRIPTION

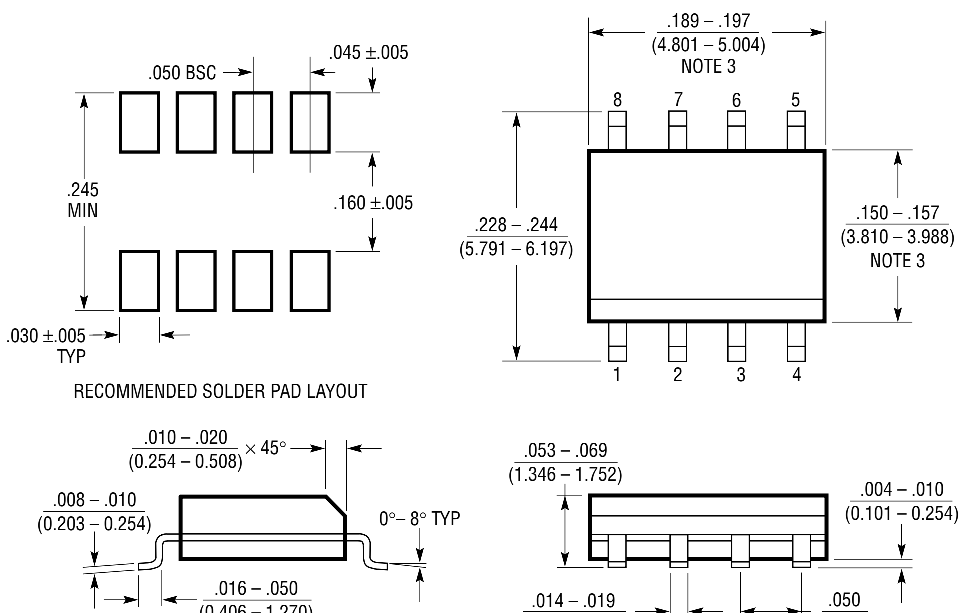
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

N Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

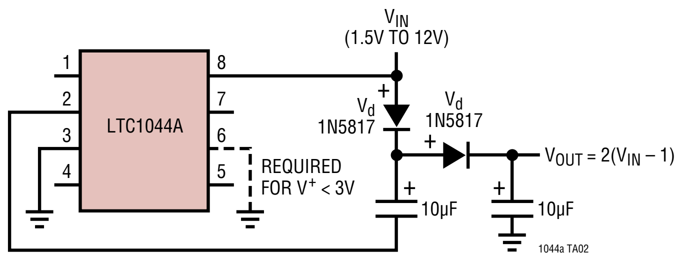
SO8 REV G 0212

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/14	Changed 0.0002% to 0.002% in the Ultra-Precision Voltage Divider section	8

TYPICAL APPLICATION

Two-Diode Capacitive Voltage Doubler



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3240-3.3/ LTC3240-2.5	3.3V/2.5V Step-Up/Step-Down Charge Pump DC/DC Converter	V_{IN}: 1.8V to 5.5V, $V_{OUT(MAX)}$ = 3.3V/2.5V, I_Q = 65µA, I_{SD} < 1µA, (2mm × 2mm) DFN Package
LTC3245	Wide V_{IN} Range Low Noise 250mA Buck-Boost Charge Pump	V_{IN}: 2.7V to 38V, $V_{OUT(MAX)}$ = 5V, I_Q = 20µA, I_{SD} = 4µA, 12-Lead MS and (3mm × 4mm) DFN Packages
LTC3255	Wide V_{IN} Range 50mA Buck (Step-Down) Charge Pump	V_{IN}: 4V to 48V, $V_{OUT(MAX)}$ = 12.5V, I_Q = 16µA, 10-Lead MSOP and (3mm × 3mm) DFN Packages

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