ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply (V_{CC})
- Low Impedance Source Voltage ..... –0.3V to 20V
- Shutdown Mode:
  - (Supply Self-Regulates to 18V)
  - Maximum Input Current 20mA

Topside Supply (V_{BST}) .....
V_{BSTREF} – 0.3V to V_{BSTREF} +20V ($V_{BST(MAX)}$ = 90V)

Topside Reference Pin (V_{BSTREF}) ..... –0.6V to 75V

$\overline{SHDN}$ Pin Voltage ..... –0.3V to V_{CC} + 0.3V

All Other Input Voltages ..... –0.3V to $5V_{REF}$ + 0.3V

$5V_{REF}$ Pin Sink Current 10mA

FSET Pin Current ..... –2mA to 5mA

All Other Input Pin Currents ..... –2mA to 2mA

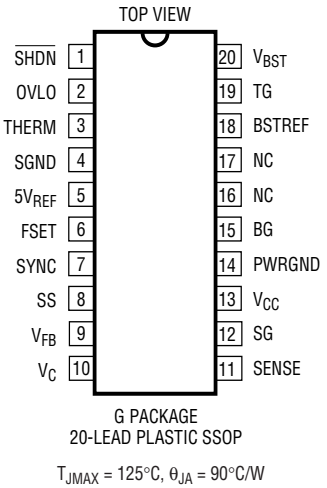
Operating Ambient
- Temperature Range (Note 4) ..... –40°C to 85°C

Operating Junction
Temperature Range ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
20-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 90°C/W

ORDER PART NUMBER
LT3781EG
LT3781IG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = V_{BST} = 12V, V_{BSTREF} = 0V, V_{VC} = 2V, V_{FB} = V_{REF} = 1.25V, C_{TG} = C_{BG} = C_{SG} = 1000pF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Protection							
V_{CCUVLO}	Undervoltage Lockout Threshold	Falling Edge Rising Edge	● ●	8.0 13	8.4 14.5	8.6 16	V V
V_{CCSHDN}	Shutdown Mode Shunt Regulator	100µA < I_{VCC} ≤ 10mA	●	16.5	18	19.9	V
I_{CC}	DC Active Supply Current	(Note 2)	 ●		17	22 25	mA mA
	DC Active UVLO Supply Current	$V_{\overline{SHDN}}$ = 1.35V, V_{CC} = 8V	●		800	1200	µA
	DC Standby Supply Current	$V_{\overline{SHDN}}$ < 0.3V	●		16	30	µA
V_{BST}	DC Active Supply Current	TG Logic High (Note 2)	●		5.0	8.5	mA
	DC Standby Supply Current	$V_{\overline{SHDN}}$ < 0.3V			0.1		µA
$V_{\overline{SHDN}}$	Shutdown Rising Threshold		●	1.15	1.25	1.35	V
	Shutdown Threshold Hysteresis			100	150	200	mV
I_{SS}	Soft-Start Charge Current	V_{SS} = 2V	●	–14	–10	–6	µA
V_{SS}	Soft-Start Reset Threshold				225		mV
$V_{BSTUVLO}$	Boost Undervoltage Lockout (V_{BST}-BSTREF) Boost UVLO Hysteresis	Falling Edge Rising Edge	● ●	5.7 6.5	6.4 7.0	7.1 7.5	V V
			●	0.3	0.6		V
5V External Reference							
V_{5VREF}	5V Reference Voltage	0 ≤ (I_{5VREF} – I_{VC}) < 20mA	 ●	4.85 4.80	5.0	5.10 5.15	V V
$I_{5VREFSC}$	Short-Circuit Current	Source, I_{VC} = 0	●	20	45		mA
R_{5VREF}	Output Impedance	0 ≤ (I_{5VREF} – I_{VC}) < 20mA			1		Ω

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ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = V_{BST} = 12V, V_{BSTREF} = 0V, V_{VC} = 2V, V_{TS} = 0V, V_{FB} = V_{REF} = 1.25V, C_{TG} = C_{BG} = C_{SG} = 1000pF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amp							
V_{FB}	Error Amplifier Reference Voltage	Measured at Feedback Pin	 ●	1.242 1.225	1.250	1.258 1.265	V V
I_{FB}	Feedback Input Current	V_{FB} = V_{REF}			–50		nA
A_V	Error Amplifier Voltage Gain				72		dB
I_{VC}	Error Amplifier Current Limit	Source Sink	● ●	10 0.5	25 1		mA mA
V_{VC}	Zero Current Output Voltage				1.4		V
	Maximum Output Voltage				3.2		V
GBW	Gain Bandwidth Product	(Note 3)			1		MHz
Current Sense							
A_V	Amplifier DC Gain				12		V/V
I_{SENSE}	Input Bias Current				–275		µA
V_{SENSE}	Current Limit Threshold	Measured at SENSE Pin	 ●	135 130	150	165 170	mV mV
t_D	Current Sense to Switch Delay				175		ns
t_{MIN}	Switch Minimum On Time	Measured at BG Output			250		ns
THERM and OVLO Fault Detectors							
V_{THERM}/	Threshold (Rising Edge)		●	1.2	1.25	1.3	V
V_{OVLO}	Threshold Hysteresis		●	20	40	60	mV
t_D	Fault Delay to Output Disable	>50mV Overdrive			650		ns
Oscillator and Synchronization Decoder							
f_{OSC}	Oscillator Frequency, Free Run	Measured at F_{SET} Pin				700	kHz
	Frequency Programming Error	f_{OSC} ≤ 500kHz (Note 3)	●	–10		5	%
I_{FSET}	FSET Input Bias Current	F_{SET} Charging, V_{FSET} = 2V			50		nA
V_{SYNC}	SYNC Logic High Input Threshold SYNC Logic Low Input Threshold	Positive-Going Edge Negative-Going Edge	● ●	 0.8	1.4 1.4	2	V V
f_{SYNC}	SYNC Frequency		●	f_{OSC}/2		350	kHz
$t_{H, L}$	Maximum SYNC Pulse Width (Logic High or Logic Low)	f_{OSC} = Oscillator Free-Run Frequency				1/f_{OSC}	s
Output Drivers							
V_{TG}	TG On Voltage TG Off Voltage		● ●	11	11.5 0.1	 0.5	V V
$t_{TGr/f}$	TG Rise/Fall Time	10% to 90%/90% to 10%			35		ns
V_{BG}	BG On Voltage BG Off Voltage		● ●	11	11.5 0.1	12 0.5	V V
$t_{BGr/f}$	BG Rise/Fall Time	10% to 90%/90% to 10%			35		ns
V_{SG}	SG On Voltage SG Off Voltage		● ●	11	11.5 0.1	12 0.5	V V
$t_{SGr/f}$	SG Rise/Fall Time	10% to 90%/90% to 10%			35		ns
t_{SG-BG}	SG to BG Enable Lag Time	4V On/Off Thresholds	●	80	150	300	ns
t_{TG-BG}	TG to BG Enable Lag Time	4V On/Off Thresholds			100		ns

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ELECTRICAL CHARACTERISTICS

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

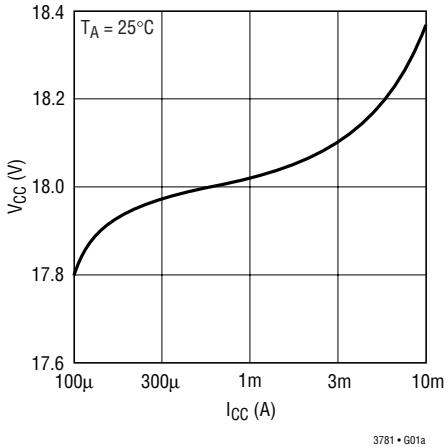
Note 2: Supply current specification does not include external FET gate charge currents. Actual supply currents will be higher and vary with operating frequency, operating voltages, and the type of external switch elements used. See Applications Information.

Note 3: Guaranteed but not tested.

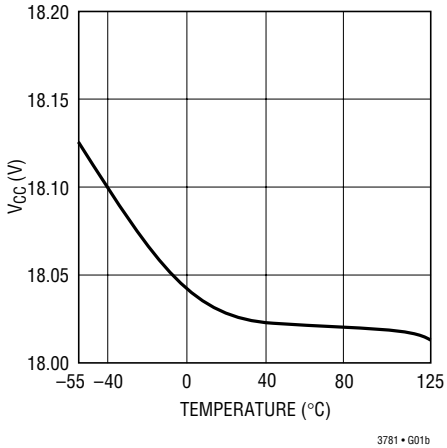
Note 4: The LT3781E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating ambient temperature range are assured by design, characterization and correlation with statistical process controls. For guaranteed performance to specifications over the –40°C to 85°C operating ambient temperature range, the LT3781I is available.

TYPICAL PERFORMANCE CHARACTERISTICS

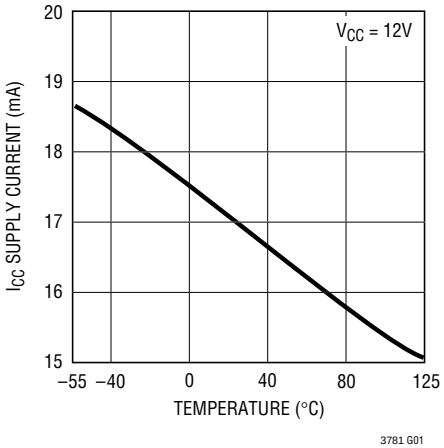
Shutdown Mode: V_{CC} vs I_{CC}



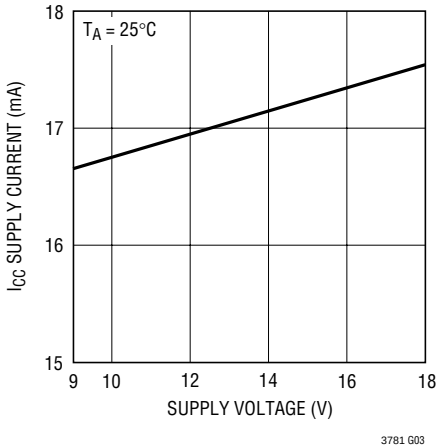
Shutdown Mode: V_{CC} vs Temperature (I_{CC} = 1mA)



I_{CC} Supply Current vs Temperature



I_{CC} Supply Current vs V_{CC} Supply Voltage



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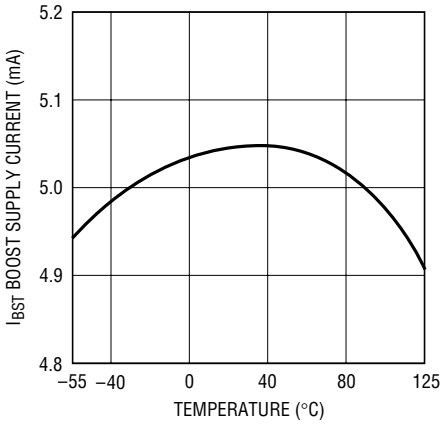
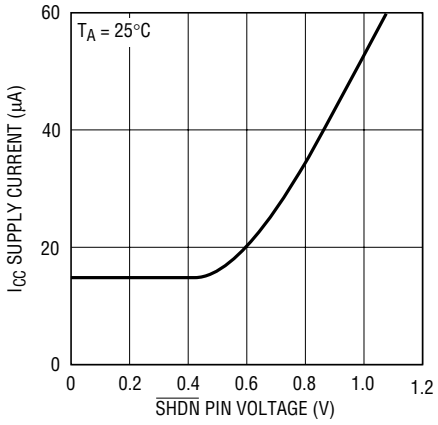
TYPICAL PERFORMANCE CHARACTERISTICS

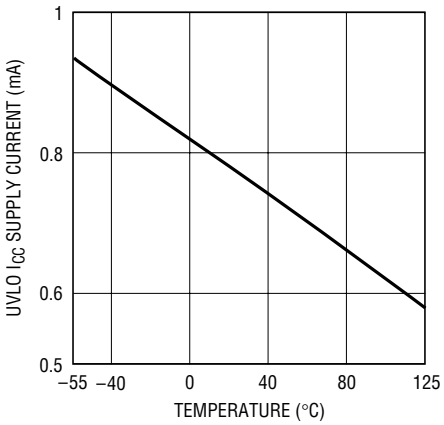
I_{BST} Boost Supply Current vs Temperature



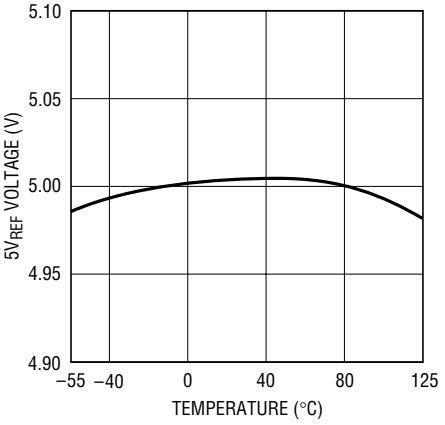
I_{CC} Supply Current vs $\overline{SHDN}$ Pin Voltage



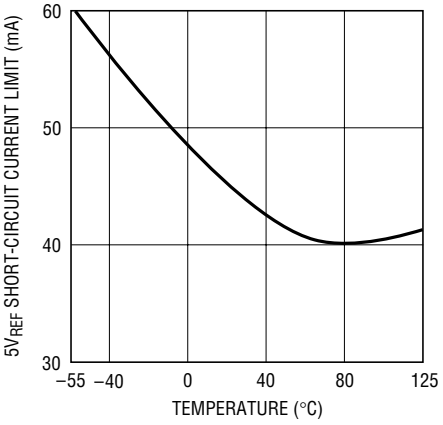
UVLO I_{CC} Supply Current vs Temperature



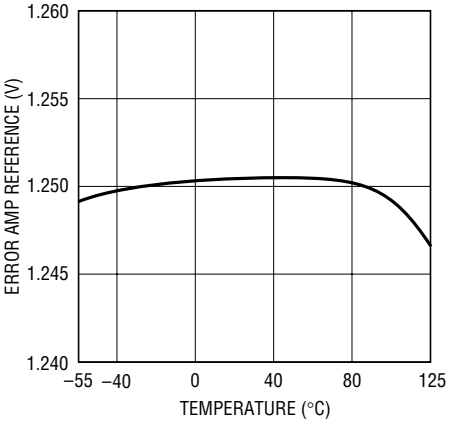
$5V_{REF}$ Voltage vs Temperature



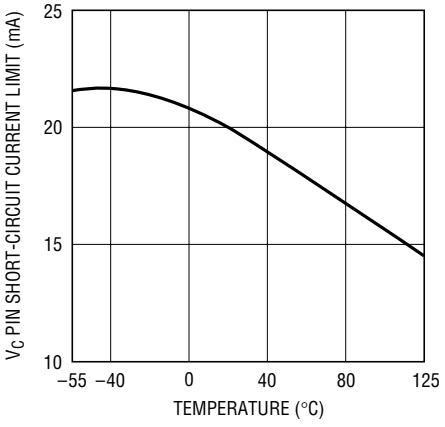
$5V_{REF}$ Short-Circuit Current Limit vs Temperature



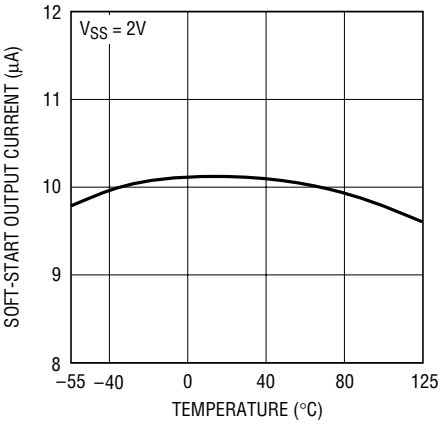
Error Amp Reference vs Temperature



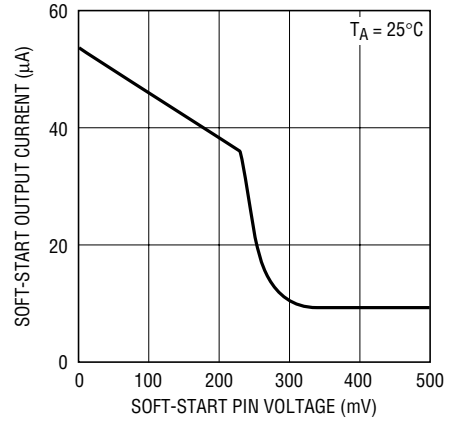
V_C Pin Short-Circuit Current Limit vs Temperature



Soft-Start Output Current vs Temperature



Soft-Start Output Current vs Soft-Start Pin Voltage



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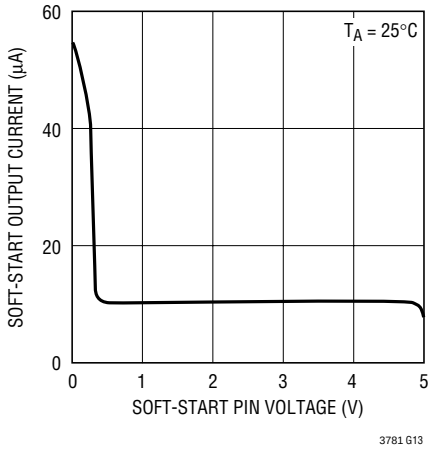
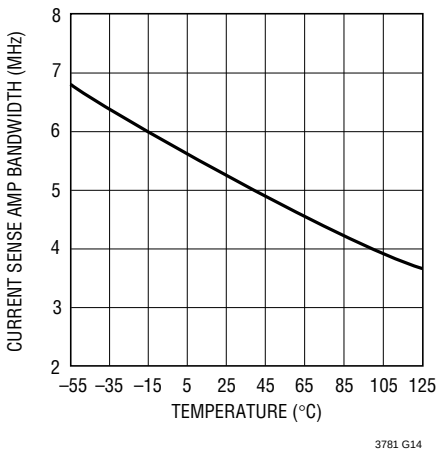
TYPICAL PERFORMANCE CHARACTERISTICS

Soft-Start Output Current vs Soft-Start Pin Voltage



Current Sense Amplifier Bandwidth vs Temperature



PIN FUNCTIONS

$\overline{\text{SHDN}}$ (Pin 1): Shutdown Pin. Pin voltages exceeding positive going threshold of 1.25V enables the LT3781. 150mV of input hysteresis resists mode switching instability.

The $\overline{\text{SHDN}}$ pin can be controlled by either a logic level input or with an analog signal. This shutdown feature is typically used for input supply undervoltage protection. A resistor divider from the converter input supply to the $\overline{\text{SHDN}}$ pin monitors that supply for control of system power-up sequencing, etc.

An 18V clamp on the V_{CC} pin is enabled during shutdown mode, preventing a trickle start circuit from pulling that pin above maximum operational levels. All other internal functions are disabled during shutdown.

OVLO (Pin 2): Overvoltage Shutdown Sense. Typically connected to input supply through a resistor divider. If pin voltage exceeds 1.25V, LT3781 switching function is disabled to protect boosted circuitry from exceeding absolute maximum voltage. 40mV of input hysteresis resists mode switching instability. Exceeding the OVLO threshold also triggers soft-start reset, resulting in a graceful recovery from an input transient event.

THERM (Pin 3): System Thermal Shutdown. Auxiliary shutdown pin that is typically used for system thermal protection. If pin voltage exceeds 1.25V, LT3781 switching function is disabled. 40mV of input hysteresis resists mode switching instability. Exceeding the THERM threshold also triggers soft-start reset, resulting in a graceful recovery.

SGND (Pin 4): Signal Ground Reference. Careful board layout techniques must be used to prevent corruption of signal ground reference. High-current switching paths must be oriented on the converter ground plane such that currents to/from the switches do not affect the integrity of the LT3781 signal ground reference.

$5V_{REF}$ (Pin 5): 5V Local Reference. Allows connection of external loads up to 20mA DC. Typically bypassed with 1µF ceramic capacitor to SGND. Reference output is current limit protected to a typical value of 45mA. If the load on the 5V reference exceeds the current limit value, LT3781 switching function is disabled and the soft-start function is reset.

FSET (Pin 6): Oscillator Timing Pin. Connect a resistor (R_{FSET}) from the $5V_{REF}$ pin to this pin and a capacitor (C_{FSET}) from this pin to ground.

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PIN FUNCTIONS

The LT3781 oscillator operates by monitoring the voltage on C_{FSET} as it is charged via R_{FSET}. When the voltage on the FSET pin reaches 2.5V, the oscillator rapidly discharges the capacitor with an average current of about 0.8mA. Once the voltage on the pin is reduced to 1.5V, the pin becomes high-impedance and the charging cycle repeats. The oscillator operates at twice the switching frequency of the controller.

Oscillator frequency f_{OSC} can be approximated by the relation:

$$f_{OSC} \cong \left\{0.5 \bullet 10^{-6} + C_{FSET}\left[\frac{R_{FSET}}{3} + \left(8 \bullet 10^{-4} + \frac{2}{R_{FSET}}\right)^{-1}\right]\right\}^{-1}$$

SYNC (Pin 7): Oscillator Synchronization Input Pin with TTL-Level Compatible Input. The SYNC input signal (at the desired synchronized operating frequency) controls both the internal oscillator (running at twice the SYNC frequency) and the output switch phase. If synchronization function is not desired, this pin may be floated or shorted to ground.

The LT3781 internal oscillator drives a toggle flip-flop that assures a ≤50% duty-cycle condition during oscillator free-run. The oscillator, therefore, runs at twice the operating frequency of the controller. The SYNC input decoder incorporates a frequency doubling circuit for oscillator synchronization, resetting the internal oscillator on both the rising and falling edges of the input signal.

The SYNC input decoder also differentiates transition phase and forces the toggle flip-flop to phase-lock with the SYNC input. A transition to logic high on the SYNC input signal corresponds to the initiation of a new switching cycle (primary switches turning on pending current control) and a transition to logic low forces a primary switch off state. As such, the maximum operating duty cycle is equal to the duty cycle of the SYNC signal. The SYNC input can therefore be used to reduce the maximum duty cycle of the controller by reducing the duty cycle of the SYNC input.

SS (Pin 8): Soft-Start. Connect a capacitor (C_{SS}) from this pin to ground.

The output voltage of the LT3781 error amplifier corresponds to the peak current sense amplifier output detected before resetting the switch outputs. The soft-start circuit forces the error amplifier output to a zero sense current for start-up. A 10μA current is forced from this pin onto an external capacitor. As the SS pin voltage ramps up, so does the LT3781 internally sensed current limit. This effectively forces the internal current limit to ramp from zero, allowing overall converter current to slowly increase until normal output regulation is achieved. This function reduces output overshoot on converter start-up. The soft-start functions incorporate a $1V_{BE}$ "dead zone" such that a zero-current condition is maintained on the V_C pin until the SS pin rises to $1V_{BE}$ above ground.

The SS pin voltage is reset to start-up condition during shutdown, undervoltage lockout, and overvoltage or overcurrent events, yielding a graceful converter output recovery from these events.

V_{FB} (Pin 9): Error Amplifier Inverting Input. Typically connected to a resistor divider from the output and compensation components to the V_C pin.

The V_{FB} pin is the converter output voltage feedback node. Input bias current of ~50nA forces pin high in the event of an open feedback path condition. The error amplifier is internally referenced to 1.25V.

Values for the V_{OUT} to V_{FB} feedback resistor (RFB1) and the V_{FB} to ground resistor (RFB2) can be calculated to program converter output voltage (V_{OUT}) via the following relation:

$$V_{OUT} = 1.25 \bullet (RFB1 + RFB2)/RFB2$$

V_C (Pin 10): Error Amplifier Output. The LT3781 error amplifier is a low impedance output inverting gain stage. The amplifier has ample current source capability to allow easy integration of isolation optocouplers that require bias currents up to 10mA. External DC loading of the V_C pin reduces the external current sourcing capacity of the $5V_{REF}$ pin by the same amount as the load on the V_C pin.

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PIN FUNCTIONS

The error amplifier is typically configured using a feedback RC network to realize an integrator circuit. This circuit creates the dominant pole for the converter regulation feedback loop. Integrator characteristics are dominated by the value of the capacitor connected from the V_C pin to the V_{FB} pin and the feedback resistor connected to the V_{FB} pin. Specific integrator characteristics can be configured to optimize transient response.

The error amplifier can also be configured as a transimpedance amplifier for use in secondary-side controller applications. (See the Applications Information section for configuration and compensation details)

SENSE (Pin 11): Current Sense Amplifier (CSA) Noninverting Input. Current is monitored via a ground referenced current sense resistor, typically in series with the source of the bottom side switch FET. Internal current limit circuitry provides for a maximum peak value of 150mV across the sense resistor during normal operation.

SG (Pin 12): Synchronous Switch Output Driver. This pin can be connected directly to gate of synchronous switch if small FETs are used (C_{GATE} < 5000pF), however, the use of a gate drive buffer is recommended for peak efficiencies.

The SG pin output is synchronized and out-of-phase with the BG output. The control timing of the SG output cause it to "lead" the primary switch path during turn-on by 150nS.

V_{CC} (Pin 13): IC Local Power Supply Input. Bypass with at a capacitor at least 10 times greater than C5V_{REF}. LT3781 incorporates undervoltage lockout that disables switching functions if V_{CC} is below 8.4V. The LT3781 supports operational V_{CC} power supply voltages from 9V to 18V (20V absolute maximum). An 18V clamp on the V_{CC} pin is enabled during shutdown mode, preventing a trickle start circuit from pulling that pin above maximum operational levels during IC shutdown.

PWRGND (Pin 14): Output Driver Ground Reference. Connect through low impedance trace to V_{IN} decoupling capacitor.

BG (Pin 15): Bottom Side Primary Switch/Forward Switch Output Driver. This pin can be connected directly to gate(s) of primary bottom side and forward switches if small FETs are used (C_{GATE} total < 5000pF), however, the use of a gate drive buffer is recommended for peak efficiencies.

The BG output is enabled at the start of each oscillator cycle in phase with the TG pin but is timed to "lag" the TG output during turn-on and "lead" the TG output during turn-off. These delays force the concentration of transitional losses onto the bottom side primary switch.

An adaptive blanking circuit disables the current sense function (via the SENSE pin) while the BG pin is below 5V.

BSTREF (Pin 18): V_{BST} Supply Reference. Typically connects to source of topside external power FET switch.

TG (Pin 19): Topside (Boosted) Primary Output Driver. This pin can be connected directly to gate of primary topside switch if small FETs are used (C_{GATE} < 5000pF), however, the use of a gate drive buffer is recommended for peak efficiencies.

V_{BST} (Pin 20): Topside Primary Driver Bootstrapped Supply. This "boosted" supply rail is referenced to the BSTREF pin.

Supply voltage is maintained by a bootstrap capacitor tied from the V_{BST} pin to the boosted supply reference (BSTREF) pin. The charge on the capacitor is refreshed each switch cycle through a Schottky diode connected from the V_{CC} supply (cathode) to the V_{BST} pin (anode). The bootstrap capacitor (C_{BOOST}) must be at least 100 times greater than the total load capacitance on the TG pin. A capacitor in the range of 0.1µF to 1.0µF is generally adequate for most applications. The bootstrap diode must have a reverse breakdown voltage greater than the converter V_{IN}. The LT3781 supports operational V_{BST} supply voltages up to 90V (absolute maximum) referenced to ground. Undervoltage Lockout disables the topside switch until V_{BST} – BSTREF > 7.0V for start-up protection of the topside switch.

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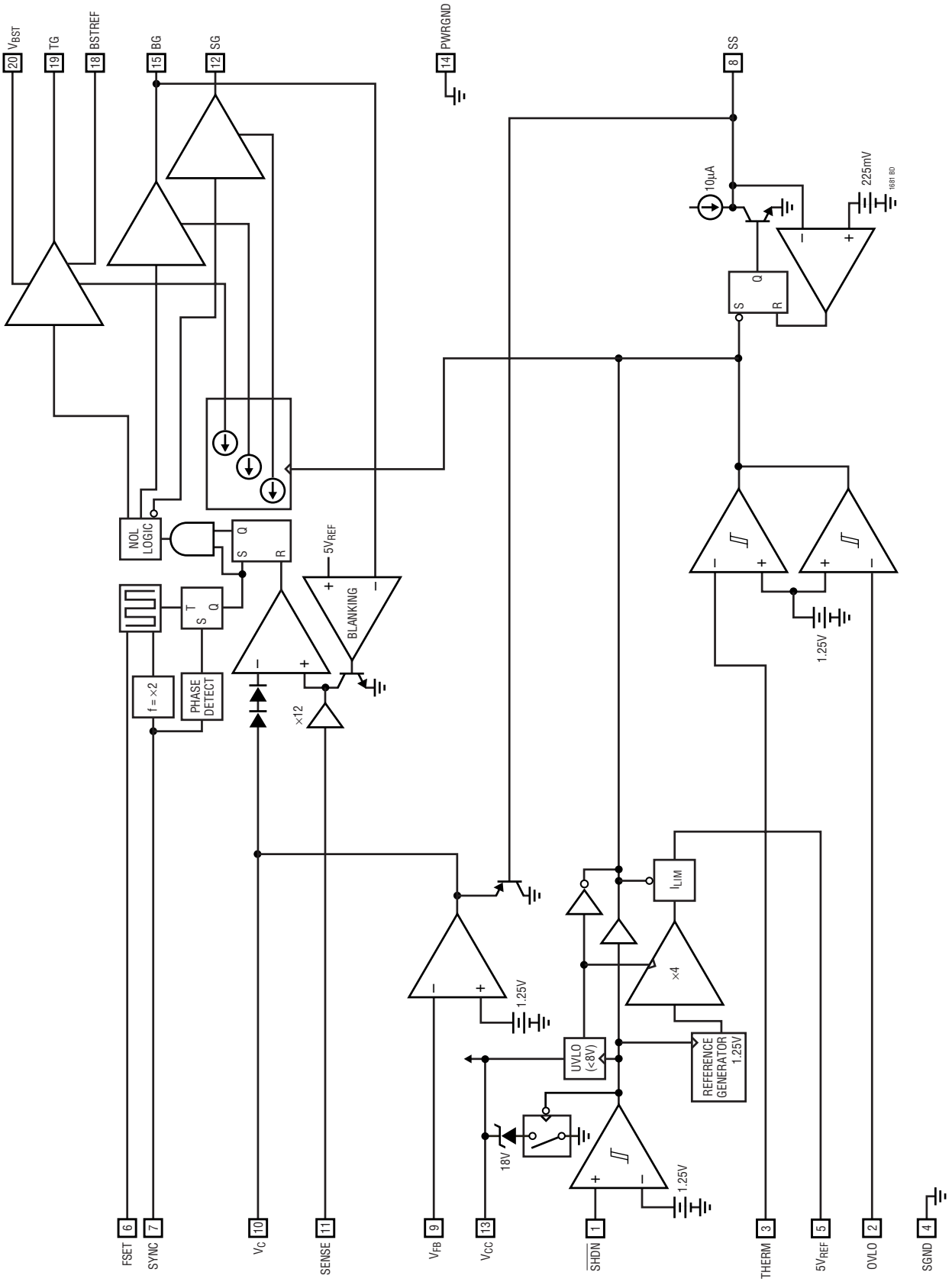
BLOCK DIAGRAM



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APPLICATIONS INFORMATION

Overview

The LT3781 is a high voltage, high current synchronous regulator controller, optimized for use with dual transistor forward topologies. The IC uses a constant frequency, current mode architecture, with internal logic that prevents operation over 50% duty cycle. A unique synchronization scheme allows the system clock to be synchronized up to an operational frequency of 350kHz, along with phase control for easy integration of multicontroller systems. A local precision 5V supply rail is available for external support circuitry and can be loaded up to 20mA.

Internal fault detection circuitry disables switching when a variety of system faults are detected such as: input supply overvoltage or undervoltage faults, excessive system temperature, and local supply overcurrent conditions. The LT3781 has a current-limit soft-start feature, which gradually increases the current drive capability of a converter system to yield a smooth start-up with minimal overshoot. The soft-start circuitry is also used for smooth recoveries from system fault conditions.

External FET switches are employed for the switch elements, and hearty switch drivers allow implementation of high current designs. An adaptive blanking scheme built into the LT3781 allows for correct current-sense blanking regardless of switch size. The LT3781 employs a voltage output error amplifier, providing superior integrator linearity and allowing easy high bandwidth integration of optocoupler feedback for fully isolated solutions.

Theory of Operation (See Block Diagram)

The LT3781 senses the output voltage of its associated converter via the V_{FB} pin. The difference between the voltage on this pin and an internal 1.25V reference is amplified to generate an error voltage on the V_C pin, which is used as a threshold for the current sense comparator. The current sense comparator gets its information from the SENSE pin, which monitors the voltage drop across an external current sense resistor. When the detected switch current increases to the level corresponding to the error voltage on the V_C pin, the switches are disabled until the next switch cycle.

During normal operation, the LT3781 internal oscillator runs at twice the switching frequency. The oscillator output toggles a T flip-flop, generating a 50% duty cycle pulse that is used internally as the system clock for the IC. When the output of this flip-flop transitions high, the primary switches are enabled. The primary side switches stay enabled until the transformer primary current, sensed via the SENSE pin connected to a ground-referenced resistor in series with the bottom side switch FET, is sufficient to trip the current sense comparator and, in turn, reset the RS latch. When the RS latch resets, the primary switches are disabled and the synchronous switch is enabled. The adaptive blanking circuit senses the bottom side gate voltage and prevents current sensing until the FET is fully enabled, preventing false triggering due to a turn-on transition glitch. If the current comparator threshold is not obtained when the flip-flop output transitions low, the RS latch is bypassed and the primary switches are disabled until the next flip-flop output transition, forcing a maximum switch duty cycle less than 50%.

System Fault Detection-The General Fault Condition (GFC)

The LT3781 contains circuitry for detecting internal and system faults. Detection of a fault triggers a “general fault condition”, or GFC. When a GFC is detected, the LT3781 disables switching and discharges the soft-start capacitor. When the GFC subsides, the LT3781 initiates a start-up cycle via the soft-start circuitry to assure a graceful recovery. Recovery from a GFC is gated by the soft-start capacitor discharge. The capacitor must be discharged to a threshold of 225mV before the GFC can be concluded. As the zero output current threshold of the SS pin is typically a transistor V_{BE}, or 0.7V, latching the GFC until a 225mV threshold is achieved assures a zero output current state in the event of a short-duration fault. A GFC is also triggered during system state change event, such as entering shutdown mode, to prevent any mode transition abnormalities.

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Events that trigger a GFC are:

a) Exceeding the current limit of the $5V_{REF}$ pin

b) Detecting an undervoltage condition on V_{CC}

c) Detecting an undervoltage condition on $5V_{REF}$

d) Pulling the $\overline{SHDN}$ pin below the shutdown threshold

e) Exceeding the 1.25V fault detector threshold on either the OVLO or THERM pins

OVLO and THERM pins is used to directly trigger a GFC. If either of these pins are not used, they can be disabled by connecting the pin to ground. The intention of the OVLO pin is to allow the monitoring of the input supply to protect from an overvoltage condition though the use of a resistor divider from the input supply. Monitoring of system temperature (THERM) is possible through use of a resistor divider using a thermistor as a divider component. The $5V_{REF}$ pin can provide the precision supply required for these applications. When these fault detection circuits are disabled during shutdown or V_{CC} pin UVLO conditions, a reduction in OVLO and THERM pin input impedance to ground will occur. To prevent excessive pin input currents, low impedance pull-up devices must not be used on these pins.

Undervoltage Lockout

The LT3781 maintains a low current operational mode when an undervoltage condition is detected on the V_{CC} supply pin, or when V_{CC} is below the undervoltage lockout (UVLO) threshold. During a UVLO condition on the V_{CC} pin, the LT3781 disables all internal functions with the exception of the shutdown and UVLO circuitry. The external $5V_{REF}$ supply is also disabled during this condition. Disabling of all switching control circuity reduces the LT3781 supply current to <1mA, making for efficient integration of trickle charging in systems that employ output feedback supply generation.

The function of the high side switch output (TG) is also gated by UVLO circuitry monitoring the bootstrap supply (V_{BST} – BSTREF). Switching of the TG pin is disabled until the voltage across the bootstrap supply is greater than 7.4V. This helps prevent the possibility of forcing the high side switch into a linear operational region, potentially causing excessive power dissipation due to inadequate gate drive during start-up.

Error Amplifer Configurations

The converter output voltage information is fed back to the LT3781 onto the V_{FB} pin where it is transformed into an output current control voltage by the error amplifier. The error amplifier is generally configured as an integrator and is used to create the dominant pole for the main converter feedback loop. The LT3781 error amplifier is a true high gain voltage amplifier. The amplifier noninverting input is internally referenced to 1.25V; the inverting input is the V_{FB} pin and the output is the V_C pin. Because both low frequency gain and integrator frequency characteristics can be controlled with external components, this amplifier allows far greater flexibility and precision compared with use of a transconductance error amplifier.

In a nonisolated converter configuration where a resistor divider is used to program the desired output voltage, the error amplifier can be configured as a simple active integrator, forming the system dominant pole (Figure 1). Placing a capacitor C_{ERR} from the V_{FB} pin to the V_C pin will set the single-pole crossover frequency at $(2\pi R_{FB}C_{ERR})^{-1}$. Additional poles and zeros can be added by increasing the complexity of the RC network.

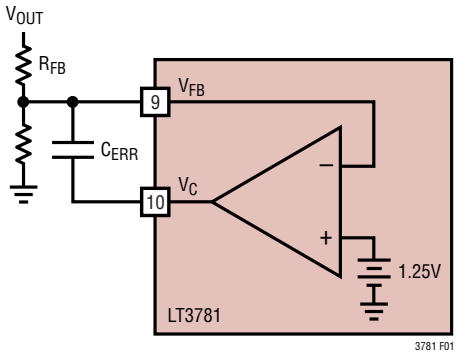

Figure 1. Nonisolated Error Amp Configuration

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Another common error amplifier configuration is for optocoupler use in fully isolated converters with secondary side control (Figure 2). In such a system, the dominant pole for the feedback loop is created at the secondary side controller, so the error amplifier needs only to translate the optocoupler information. The bandwidths of the optocoupler and amplifier should be as high as possible to simplify system compensation. This high bandwidth operation is accomplished by using the error amplifier as a transimpedance amplifier, with the optocoupler transistor emitter providing feedback information directly into the V_{FB} pin. A resistor from V_{FB} to ground provides the DC bias condition for the optocoupler. Connecting the optocoupler transistor collector to the local $5V_{REF}$ supply reduces Miller capacitance effects and maximizes the bandwidth of the optocoupler. Also, higher optocoupler current means higher bandwidth, and the $5V_{REF}$ supply can provide collector currents up to 10mA.

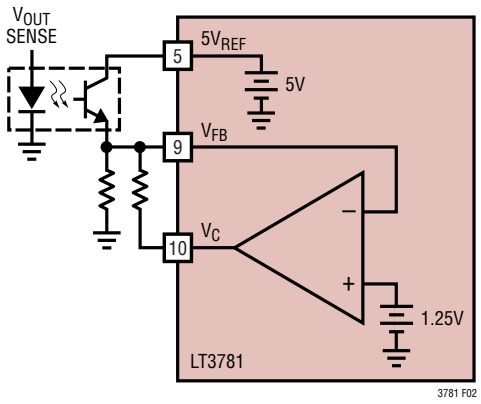

Figure 2. Optocoupler High-BW Configuration

Oscillator Frequency Programming and Synchronization

The LT3781 internal oscillator runs at twice the system switching frequency. The oscillator output toggles a T flip-flop, generating a 50% duty cycle pulse that is used internally as the system clock for the IC. Free-run frequency for the internal oscillator is programmed via an RC timing network connected to the FSET pin. A pull-up resistor R_{FSET}, connected from the $5V_{REF}$ pin to FSET, provides current to charge a timing capacitor C_{FSET} connected from the FSETpin to ground. The oscillator operates by allowing R_{FSET} to charge C_{FSET} up to 2.5V at which point R_{FSET} is pulled back toward ground by a 2.5K resistor internal to the LT3781. When the voltage across C_{FSET} is pulled down to 1.5V, the FSET pin becomes high impedance, once again allowing R_{FSET} to charge C_{FSET}.

Figure 3 is a plot of oscillator frequency vs C_{FSET} and R_{FSET} is shown below. Typical values for 300kHz operation (150kHz system frequency) are C_{FSET} = 150pF and R_{FSET} = 51kΩ.

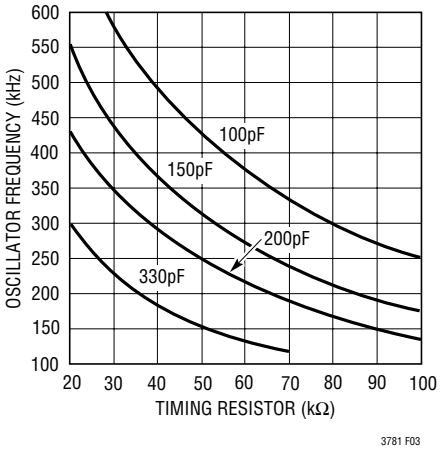

Figure 3. Oscillator Frequency vs. Timing Components

Due the relatively fast fall time of the oscillator waveform, the FSET pin is held at its 1.5V threshold by an internal low impedance clamp to reduce undershoot error. As a result, if this pin is externally forced low for any reason, external current limiting is required to prevent damage to the LT3781. Continuous source current from the FSET pin should not exceed 1mA. Putting a 2k resistor in series with any low impedance pull-down device will assure proper function and protect the IC from damage.

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Oscillator Synchronization

Synchronization of the LT3781 system clock is accomplished by driving a TTL level logic pulse train at the desired system switching frequency into the SYNC pin. In order to assure proper synchronization, each phase of the synchronization signal must be less than an oscillator free-run cycle.

The SYNC input pulse controls the phasing as well as the frequency of controller switching. The SYNC circuit functions by forcing the phase of the oscillator output flip-flop to match the phase of the SYNC pulse and prematurely ending the oscillator charge cycle on each transition edge. At the SYNC logic low-to-high transition, the LT3781 starts a switch-on cycle and the minimum switch-off period is forced during the SYNC logic low period. Because the SYNC logic low period corresponds directly to the minimum off time, the converter maximum duty cycle can be forced using the SYNC input. For example, a 30% duty cycle SYNC pulse forces 30% maximum duty cycle operation for the converter. Because the logic-low pulse width exceeds the logic-high pulse width in < 50% duty cycle operation, the oscillator free-run cycle time must be programmed to exceed the logic-low duration.

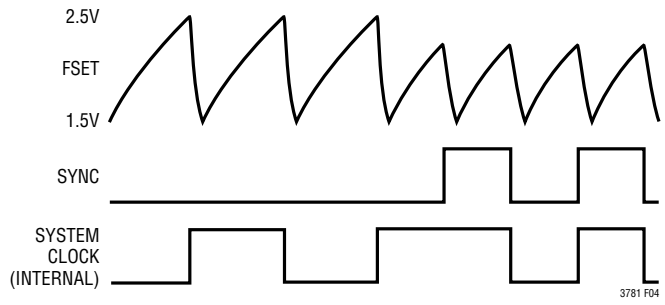

Figure 4. Oscillator/SYNC Waveforms

It is also possible to run the LT3781 in a SYNC-only mode by disabling the oscillator completely. Connecting a resistor divider from the $5V_{REF}$ pin to the FSET pin forcing a voltage within the charge range of 1.5V-2.5V will allow the oscillator to follow the SYNC input exclusively with no provision for free-run. Setting values to force a voltage as close to 2V as possible is recommended.

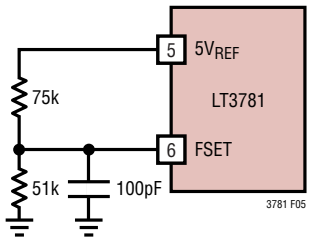

Figure 5. Oscillator Connection for SYNC-Only Mode Operation

Bootstrap Start

It is inefficient as well as impractical to power a controller IC from a high-voltage input supply. Using a linear preregulation scheme to provide the required V_{CC} voltage for the LT3781 would waste significant power, reducing converter efficiencies and creating additional thermal concerns. Self-biased power schemes take advantage of inherent converter efficiencies to significantly reduce losses associated with powering the controller. Bootstrapped power can be derived using auxiliary windings on the power transformer or inductor, rectified taps on switching nodes, or the converter output directly.

Start-up circuitry built into the LT3781 allows V_{CC} to increase from 0V to 14.5V before the converter is enabled. During this time, start-up current is less than 1mA. The trickle current required for charging the V_{CC} supply is typically generated with a resistor from the converter high voltage input. When combined with the V_{CC} bypass capacitor, the current through the start-up resistor creates a voltage ramp on V_{CC} whose slope governs the turn-on time of the converter. The low quiescent current of the LT3781 allows the input voltage to be trickled up with minimal power dissipation in the start-up resistor. At V_{CC} = 14.5V, the LT3781 internal circuitry is enabled and switching begins. If enough bootstrap power is fed back into V_{CC} to keep that supply voltage above 8.4V, then switching continues and a bootstrap start is accomplished. If the input voltage drops below 8.4V, the LT3781 is disabled and the switching regulator returns to the start-up low current state.

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Shutdown

The LT3781 SHDN pin will support TTL and CMOS logic signals and also analog inputs. The $\overline{SHDN}$ pin turn-on (rising) threshold is 1.25V with 150mV of hysteresis. A common use of the $\overline{SHDN}$ pin is for under voltage detection on the input supply. Driving the $\overline{SHDN}$ pin with a resistor-divider connected from the input supply to ground will prevent switching until the desired input supply voltage is achieved.

An 18V clamp on the V_{CC} pin is enabled during shutdown mode, preventing a trickle start circuit from pulling that pin above maximum operational levels.

The LT3781 enters an ultralow current shutdown mode when the $\overline{SHDN}$ pin is below 350mV. During this mode, total supply current drops to a typical value of 16µA. When $\overline{SHDN}$ rises above 350mV, the IC will draw increasing amounts of supply current until just before the 1.25V turn-on threshold is achieved, when the supply current reaches 75µA.

The shutdown function can be disabled by connecting the $\overline{SHDN}$ pin to V_{CC}. This pin is internally clamped to 2.5V through a 20k series input resistance and can therefore draw almost 1mA when tied directly to the V_{CC} supply. This additional current can be minimized by making the connection through an external series resistor (100k is typically used).

Soft-Start

The LT3781 current control pin (V_C) limits sensed current to zero at voltage less than 1.4V through full current limit at V_C = 3.2V, yielding 1.8V over the full regulation range. The voltage on the V_C pin is internally forced to be less than or equal to SS + 0.7V. As such, the SS pin has a "dead zone" between 0V and 0.7V, where a zero sensed current condition is maintained. At SS voltages above 0.7V, the sensed current limit threshold on the V_C pin may rise as needed up to the SS maintained current limit value. Once the SS pin rises to the V_C pin maximum value less 0.7V, or 2.5V, the SS circuit has no effect.

The SS pin sources a typical current of 10µA. Placing a capacitor (C_{SS}) from the SS pin to ground will cause the voltage on the SS pin to ramp up at a controlled rate, allowing a graceful increase of maximum converter output current during a start-up condition. The start-up delay time to full available current limit is:

$$t_{SS} = 2.5 \bullet 10^5 \bullet C_{SS} \text{ (sec)}$$

The LT3781 internally pulls the SS pin below the zero current threshold during any fault condition to assure graceful recovery. The SS circuit also acts as a fault control latch to assure a full-range recovery from a short duration fault. Once a fault condition is detected, the LT3781 will suspend switching until the SS pin has discharged to approximately 225mV.

Layout Considerations-Grounding

The LT3781 is typically used in high current converter designs that involve substantial switching transients. The switch drivers on the IC are designed to drive large capacitances and, as such, generate significant transient currents. Careful consideration must be made regarding input and local power supply bypassing to avoid corrupting the ground references used by the error amplifier and current sense circuitry.

Effective grounding of the two-transistor synchronous forward topology where the LT3781 is used is inherently difficult. The situation is complicated further by the number of bypass elements that must be considered.

Typically, high current paths and transients from the input supply and any local drive supplies must be kept isolated from SGND, to which sensitive circuits such as the error amp reference and the current sense circuits, as well as the local $5V_{REF}$ supply, are referred. By virtue of the topologies used in LT3781 applications, the large currents from the primary switches, as well as the switch drive transients, pass through the sense resistor to ground. This defines the ground connection of the sense resistor as the reference point for both SGND and PGND. In nonisolated applications where SGND is the output reference, we now have a condition where every bypass capacitor in the converter is referenced to the same point.

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Effective grounding can be achieved by considering the return current paths from the sense resistor to each respective bypass capacitor. Don't be tempted to run small traces to separate the grounds. A power ground plane is important as always in high power converters, but bypass elements must be oriented such that transient currents in the return paths of V_{IN} and V_{CC} do not mix. Care must be taken to keep these transients away from the SGND reference. An effective approach is to use a 2-layer ground plane, reserving an entire layer for SGND. The $5V_{REF}$ and nonisolated converter output bypasses can then be directly connected to the SGND plane.

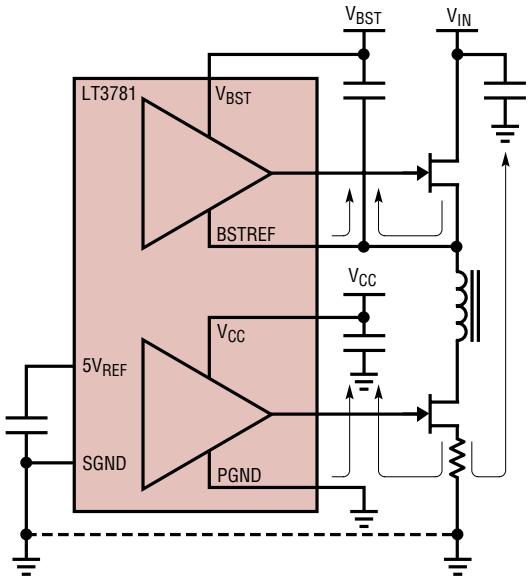

Figure 6. High-Current Transient Return Paths

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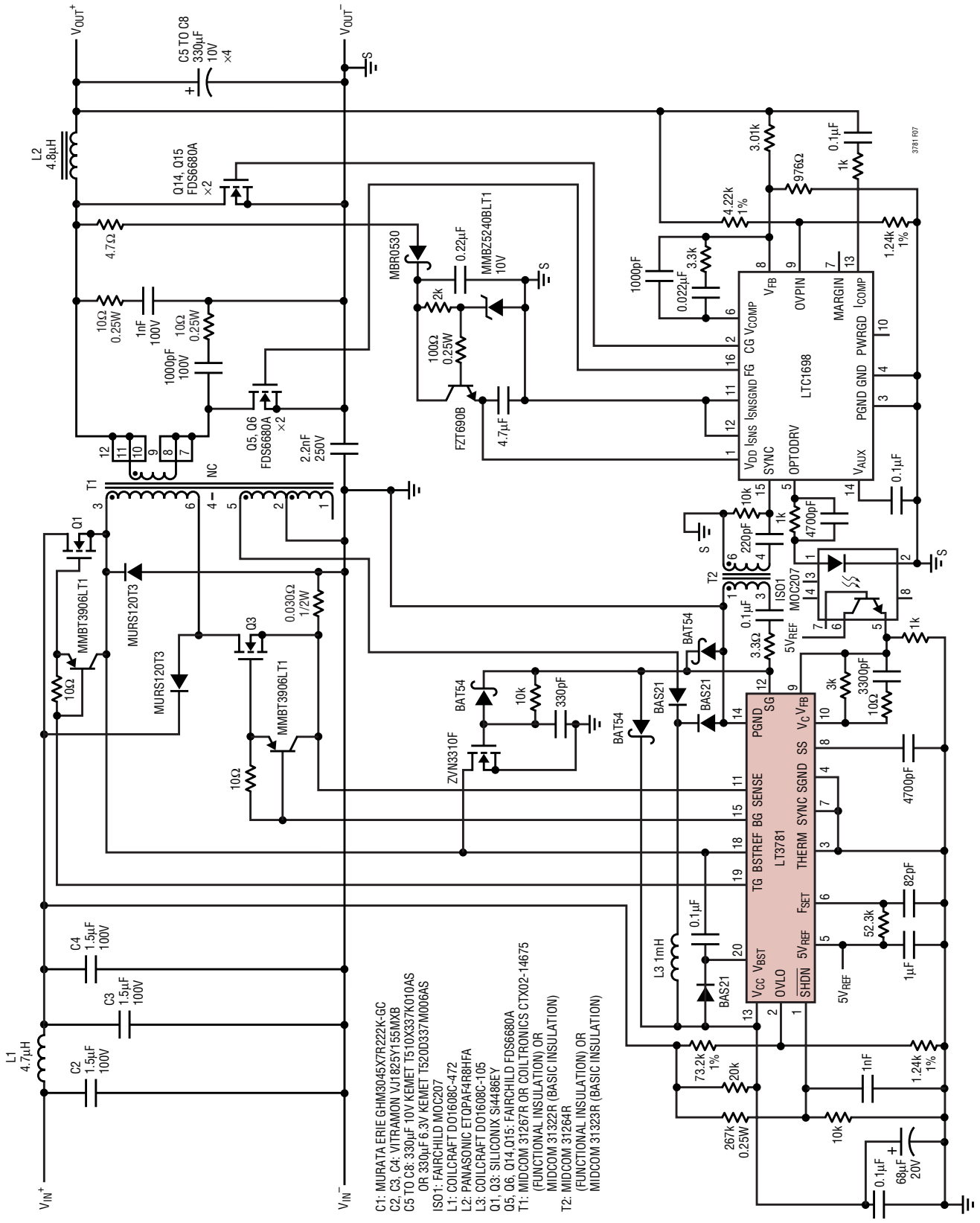

Figure 7. 36V to 72V DC in to 5V/10A Isolated Synchronous Forward Converter

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TYPICAL APPLICATIONS

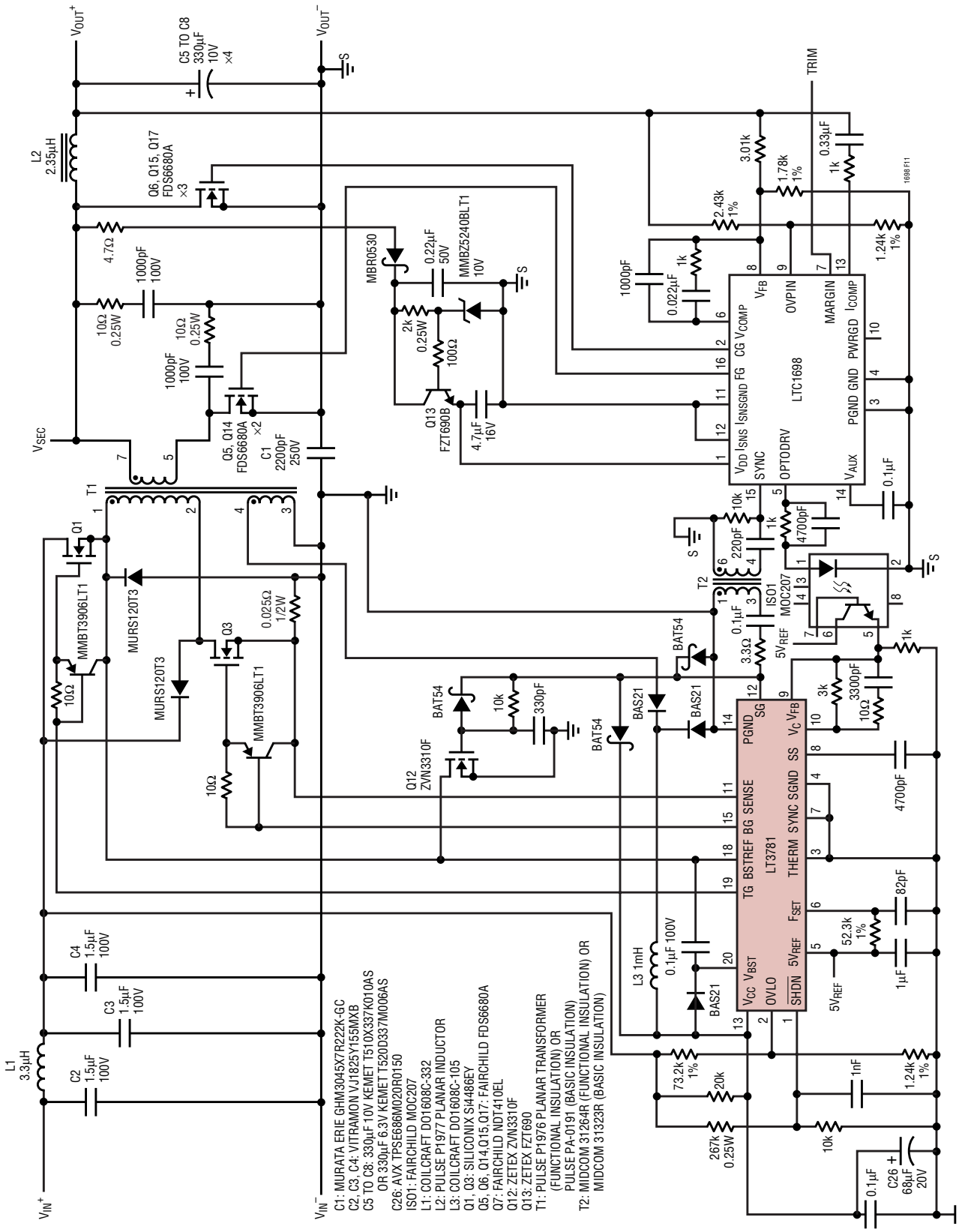

Figure 8. 36V to 72V DC in to 3.3V/20A Isolated Synchronous Forward Converter

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TYPICAL APPLICATIONS

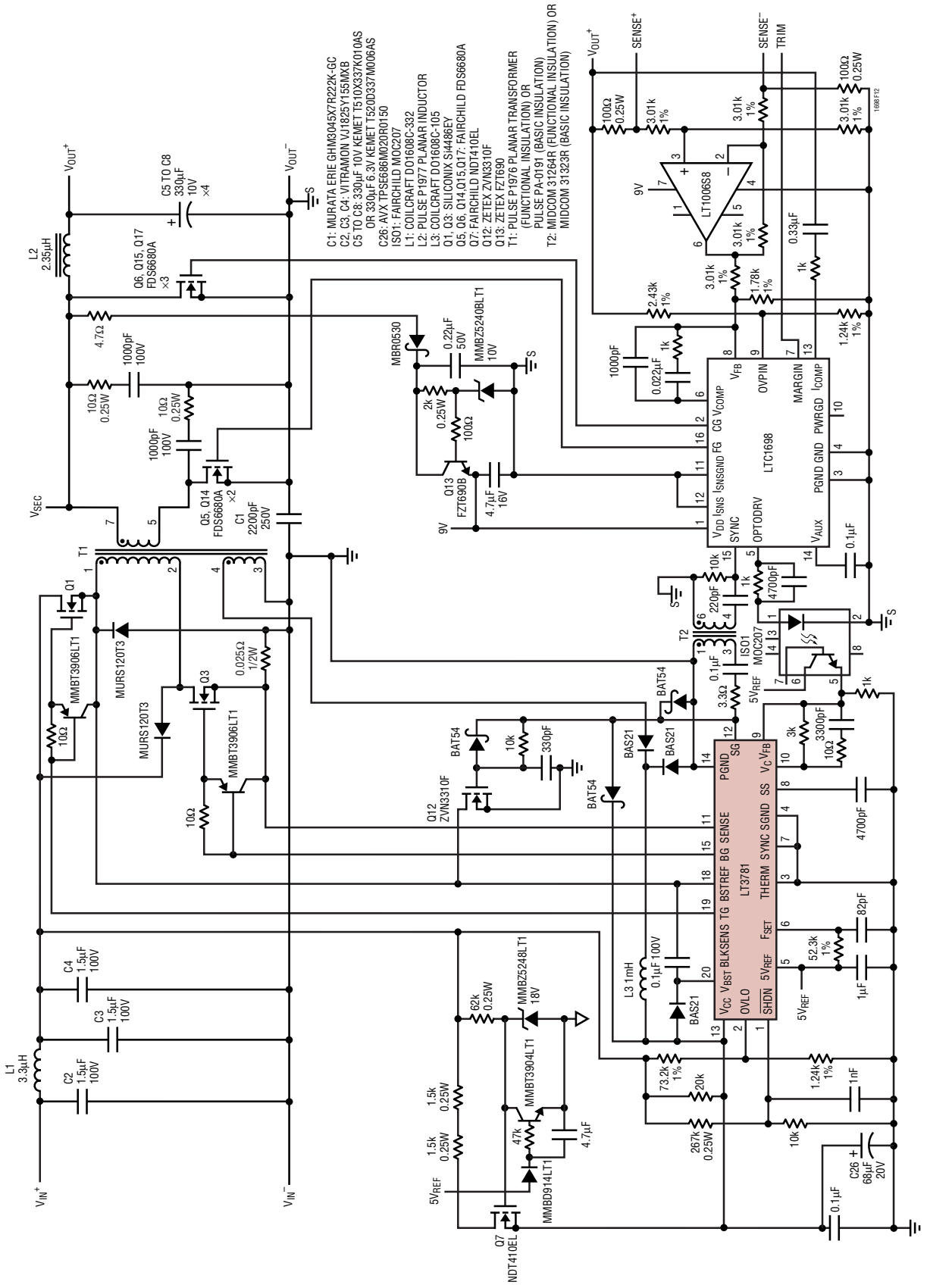

Figure 9. 36V to 72V DC in to 3.3V/20A Isolated Synchronous Forward Converter with Fast Start and Differential Sense

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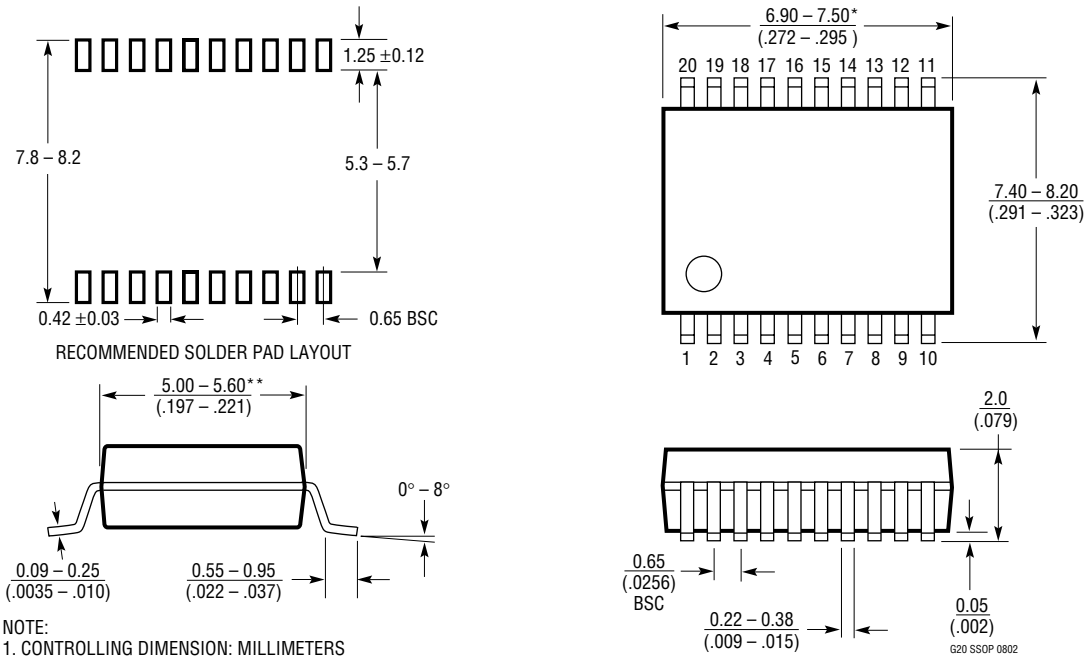
PACKAGE DESCRIPTION

G Package
20-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

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RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1158	Half-Bridge N-Channel MOSFET Driver	Current Limit Protection, 100% of Duty Cycle
LT1160	Half-Bridge N-Channel MOSFET Driver	Up to 60V Input Supply, No Shoot-Through
LT1162	Dual Half-Bridge N-Channel MOSFET Driver	V_{IN} to 60V, Good for Full-Bridge Applications
LT1336	Half-Bridge N-Channel MOSFET Driver	Smooth Operation at High Duty Cycle (95% to 100%)
LT1339	High Power Synchronous DC/DC Controller	60V Dual N-Channel MOSFET Controller
LTC®1530	High Power Step-Down Switching Regulator Controller	Excellent for 5V to 3.x Up to 50A
LTC1625	No R_{SENSE}™ Synchronous Controller	97% Efficient, $1.19V \le V_{IN} \le 36V$, $1.19V \le V_{OUT} \le V_{IN}$
LT1640	Negative Voltage Hot Swap™ Controller	Allows Safe Board Insertion and Removal from a Live –48V Backplane, Operates from –10V to –80V
LT1680	High Power DC/DC Current Mode Step-Up Controller	High Side Current Sense, Up to 60V Input
LT1681	Dual Transistor Synchronous Foward Controller	Operation up to 72V Maximum
LTC1696	Overvoltage Protection Controller in ThinSOT™ Package	±2% Overvoltage Threshold Protection Accuracy, Gate Drive for SCR Crowbar or External N-Channel MOSFET Disconnect, Monitors Two Output Voltages
LTC1698	Secondary Synchronous Rectifier Controller	Use with the LT1681, Isolated Power Supplies, Contains Voltage Merging, Optocoupler Driver, Synchronization Circuit with the Primary Side
LTC1735	Synchronous Step-Down Controller	Current Mode, $3.5V \le V_{IN} \le 36V$, $0.5V \le V_{OUT} \le 5V$
LTC1922-1	Synchronous Phase Modulated Full-Bridge Controller	50W to 2kW Power Supply Design, Adaptive Direct Sense ZVS
LTC1929	2-Phase 42A Synchronous Controller	Minimizes C_{IN} and C_{OUT}, $4V \le V_{IN} \le 36V$, 300kHz
LT3710	Secondary Side Synchronous Post Regulator	Generates Auxiliary Output in Isolated DC/DC Converters, Programmable Current Limit Protection, 0.8V ±1.5% Reference
LTC3728	550kHz, Dual 2-Phase Synchronous Controller	High Frequency Reduces Size of Inductors, Minimum C_{IN}, $4V \le V_{IN} \le 36V$, $I_{OUT1, 2}$ up to 20A

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