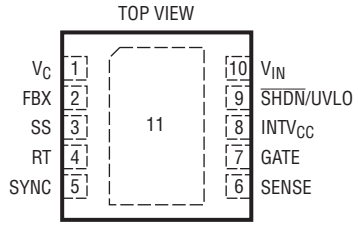
ABSOLUTE MAXIMUM RATINGS (Note 1)

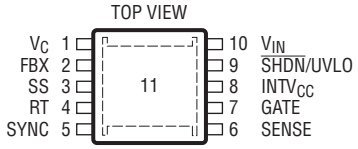
V_{IN}, $\overline{SHDN}$/UVLO (Note 7) 100V
$INTV_{CC}$ ..... V_{IN} + 0.3V, 20V
GATE ..... $INTV_{CC}$ + 0.3V
SYNC 8V
V_C, SS 3V
RT 1.5V
SENSE ..... ±0.3V
FBX ..... –6V to 6V

Operating Junction Temperature Range (Notes 2, 8)
LT3758E/LT3758AE ..... –40°C to 125°C
LT3758I/LT3758AI ..... –40°C to 125°C
LT3758H/LT3758AH ..... –40°C to 150°C
LT3758MP/LT3758AMP ..... –55°C to 150°C
Storage Temperature Range
DFN ..... –65°C to 125°C
MSOP ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSOP ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3758EDD#PBF	LT3758EDD#TRPBF	LDNK	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3758IDD#PBF	LT3758IDD#TRPBF	LDNK	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3758EMSE#PBF	LT3758EMSE#TRPBF	LTDNM	10-Lead (3mm × 3mm) Plastic MSOP	–40°C to 125°C
LT3758IMSE #PBF	LT3758IMSE#TRPBF	LTDNM	10-Lead (3mm × 3mm) Plastic MSOP	–40°C to 125°C
LT3758HMSE#PBF	LT3758HMSE#TRPBF	LTDNM	10-Lead (3mm × 3mm) Plastic MSOP	–40°C to 150°C
LT3758MPMSE #PBF	LT3758MPMSE#TRPBF	LTDNM	10-Lead (3mm × 3mm) Plastic MSOP	–55°C to 150°C
LT3758AEDD#PBF	LT3758AEDD#TRPBF	LGGS	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3758AIDD#PBF	LT3758AIDD#TRPBF	LGGS	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3758AEMSE#PBF	LT3758AEMSE#TRPBF	LTGGK	10-Lead (3mm × 3mm) Plastic MSOP	–40°C to 125°C
LT3758AIMSE#PBF	LT3758AIMSE#TRPBF	LTGGK	10-Lead (3mm × 3mm) Plastic MSOP	–40°C to 125°C
LT3758AHMSE#PBF	LT3758AHMSE#TRPBF	LTGGK	10-Lead (3mm × 3mm) Plastic MSOP	–40°C to 150°C
LT3758AMPMSE#PBF	LT3758AMPMSE#TRPBF	LTGGK	10-Lead (3mm × 3mm) Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, $\overline{SHDN}$/UVLO = 24V, SENSE = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Range			5.5		100	V
V_{IN} Shutdown I_Q	$\overline{SHDN}$/UVLO = 0V $\overline{SHDN}$/UVLO = 1.15V			0.1	1 6	µA µA
V_{IN} Operating I_Q	V_C = 0.3V, R_T = 41.2k			1.75	2.2	mA
V_{IN} Operating I_Q with Internal LDO Disabled	V_C = 0.3V, R_T = 41.2k, $INTV_{CC}$ = 7.5V			350	400	µA
SENSE Current Limit Threshold		●	100	110	120	mV
SENSE Input Bias Current	Current Out of Pin			–65		µA
Error Amplifier						
FBX Regulation Voltage ($V_{FBX(REG)}$)	FBX > 0V (Note 3) FBX < 0V (Note 3)	● ●	1.569 –0.816	1.6 –0.800	1.631 –0.784	V V
FBX Overvoltage Lockout	FBX > 0V (Note 4) FBX < 0V (Note 4)		6 7	8 11	10 14	% %
FBX Pin Input Current	FBX = 1.6V (Note 3) FBX = –0.8V (Note 3)		 –10	70	100 10	nA nA
Transconductance g_m ($\Delta I_{VC}/\Delta FBX$)	(Note 3)			230		µS
V_C Output Impedance	(Note 3)			5		MΩ
V_{FBX} Line Regulation ($\Delta V_{FBX}/[\Delta V_{IN} \bullet V_{FBX(REG)}]$)	FBX > 0V, 5.5V < V_{IN} < 100V (Notes 3, 6) FBX < 0V, 5.5V < V_{IN} < 100V (Notes 3, 6)			0.006 0.005	0.025 0.03	%/V %/V
V_C Current Mode Gain ($\Delta V_{VC}/\Delta V_{SENSE}$)				5.5		V/V
V_C Source Current	V_C = 1.5V			–15		µA
V_C Sink Current	FBX = 1.7V FBX = –0.85V			12 11		µA µA
Oscillator						
Switching Frequency	R_T = 41.2k to GND, FBX = 1.6V R_T = 140k to GND, FBX = 1.6V R_T = 10.5k to GND, FBX = 1.6V		270	300 100 1000	330	kHz kHz kHz
RT Voltage	FBX = 1.6V			1.2		V
Minimum Off-Time				220		ns
Minimum On-Time				220		ns
SYNC Input Low					0.4	
SYNC Input High			1.5			
SS Pull-Up Current	SS = 0V, Current Out of Pin			–10		µA
Low Dropout Regulator						
$INTV_{CC}$ Regulation Voltage		●	7	7.2	7.4	V
$INTV_{CC}$ Undervoltage Lockout Threshold	Falling $INTV_{CC}$ UVLO Hysteresis		4.3	4.5 0.5	4.7	V V
$INTV_{CC}$ Overvoltage Lockout Threshold				17.5		V
$INTV_{CC}$ Current Limit	V_{IN} = 100V V_{IN} = 20V		11	16 50	22	mA mA
$INTV_{CC}$ Load Regulation ($\Delta V_{INTVCC}/V_{INTVCC}$)	0 < I_{INTVCC} < 10mA, V_{IN} = 8V		–1	–0.4		%
$INTV_{CC}$ Line Regulation ($\Delta V_{INTVCC}/[\Delta V_{IN} \bullet V_{INTVCC}]$)	8V < V_{IN} < 100V			0.005	0.02	%/V
Dropout Voltage ($V_{IN} - V_{INTVCC}$)	V_{IN} = 6V, I_{INTVCC} = 10mA			500		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V, $\overline{SHDN}$/UVLO = 24V, SENSE = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Current in Shutdown	$\overline{SHDN}$/UVLO = 0V, $INTV_{CC}$ = 8V			16		µA
$INTV_{CC}$ Voltage to Bypass Internal LDO					7.5	V
Logic Inputs						
$\overline{SHDN}$/UVLO Threshold Voltage Falling	V_{IN} = $INTV_{CC}$ = 8V	●	1.17	1.22	1.27	V
$\overline{SHDN}$/UVLO Input Low Voltage	I_{VIN} Drops Below 1µA				0.4	V
$\overline{SHDN}$/UVLO Pin Bias Current Low	$\overline{SHDN}$/UVLO = 1.15V		1.7	2	2.5	µA
$\overline{SHDN}$/UVLO Pin Bias Current High	$\overline{SHDN}$/UVLO = 1.33V			10	100	nA
Gate Driver						
t_r Gate Driver Output Rise Time	C_L = 3300pF (Note 5), $INTV_{CC}$ = 7.5V			22		ns
t_f Gate Driver Output Fall Time	C_L = 3300pF (Note 5), $INTV_{CC}$ = 7.5V			20		ns
Gate Output Low (V_{OL})					0.05	V
Gate Output High (V_{OH})			$INTV_{CC}$ –0.05			V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3758E/LT3758AE are guaranteed to meet performance specifications from the 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3758I/LT3758AI are guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3758H/LT3758AH are guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The LT3758MP/LT3758AMP are 100% tested and guaranteed over the full –55°C to 150°C operating junction temperature range.

Note 3: The LT3758/LT3758A are tested in a feedback loop which servos V_{FBX} to the reference voltages (1.6V and –0.8V) with the V_C pin forced to 1.3V.

Note 4: FBX overvoltage lockout is measured at $V_{FBX(OVERVOLTAGE)}$ relative to regulated $V_{FBX(REG)}$.

Note 5: Rise and fall times are measured at 10% and 90% levels.

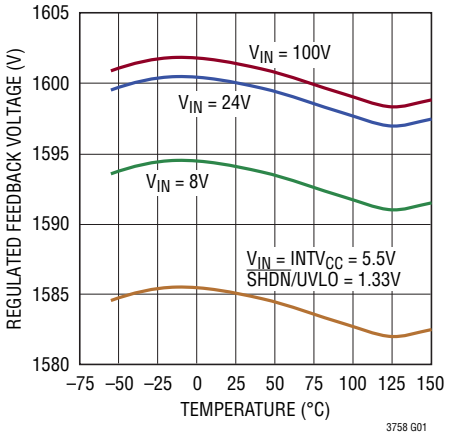
Note 6: $\overline{SHDN}$/UVLO = 1.33V when V_{IN} = 5.5V.

Note 7: For V_{IN} below 6V, the $\overline{SHDN}$/UVLO pin must not exceed V_{IN}.

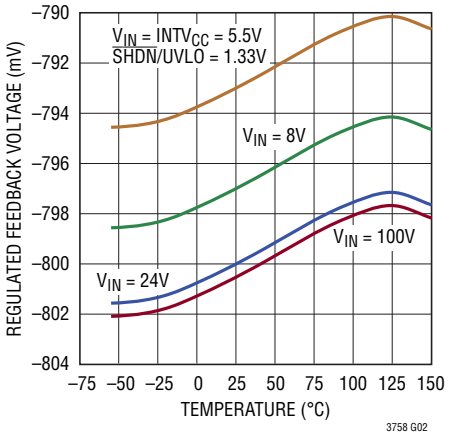
Note 8: The LT3758/LT3758A include overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

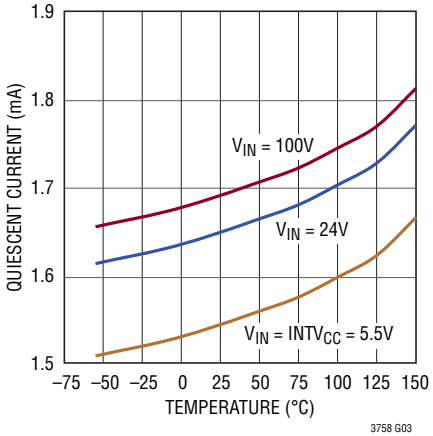
Positive Feedback Voltage vs Temperature, V_{IN}



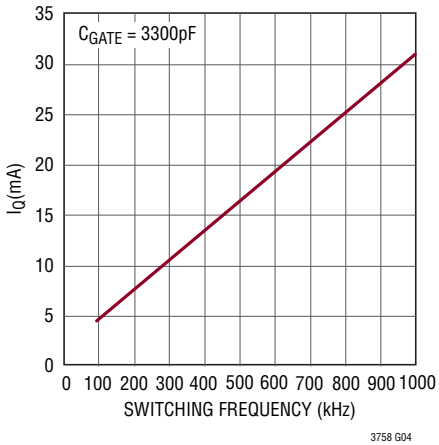
Negative Feedback Voltage vs Temperature, V_{IN}



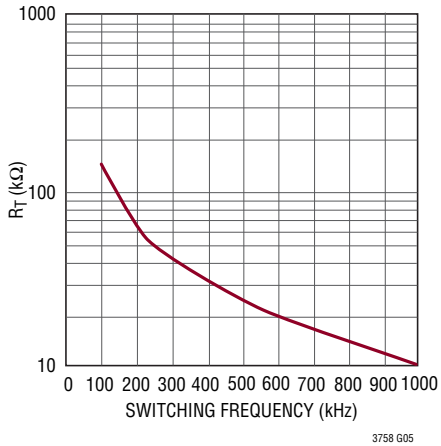
Quiescent Current vs Temperature, V_{IN}



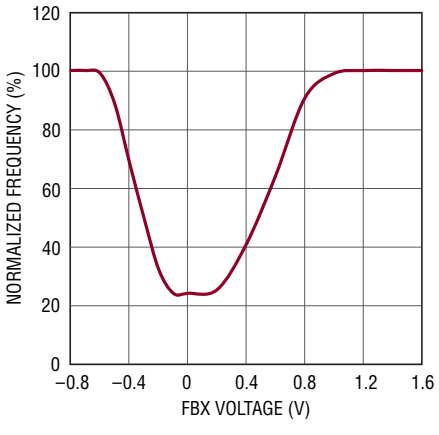
Dynamic Quiescent Current vs Switching Frequency



R_T vs Switching Frequency

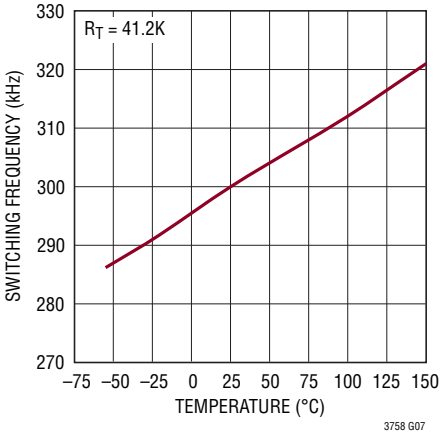


Normalized Switching Frequency vs FBX

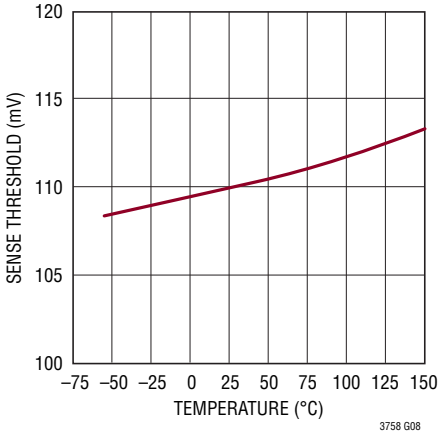


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

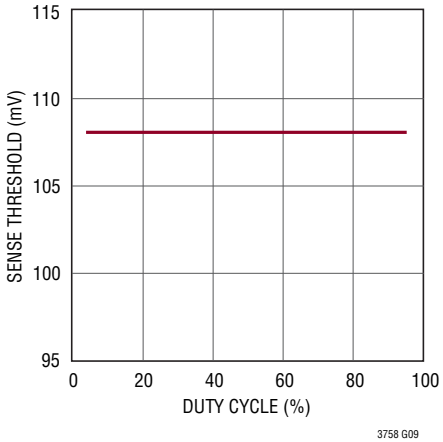
Switching Frequency vs Temperature



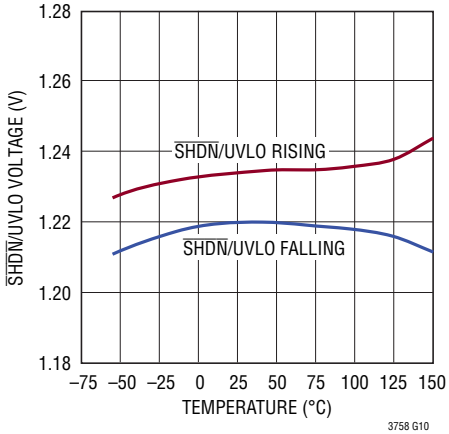
SENSE Current Limit Threshold vs Temperature



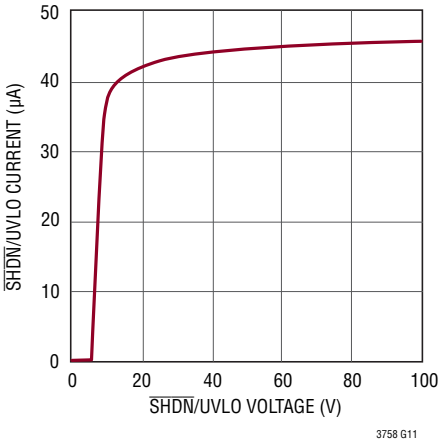
SENSE Current Limit Threshold vs Duty Cycle



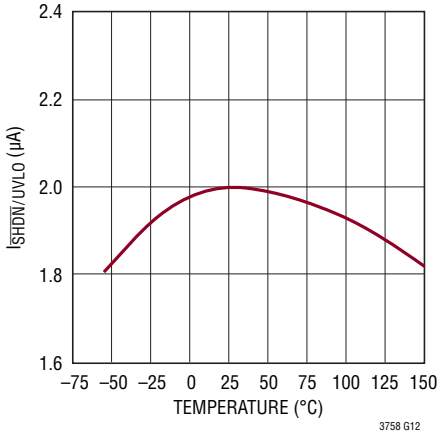
$\overline{SHDN}$/UVLO Threshold vs Temperature



$\overline{SHDN}$/UVLO Current vs Voltage

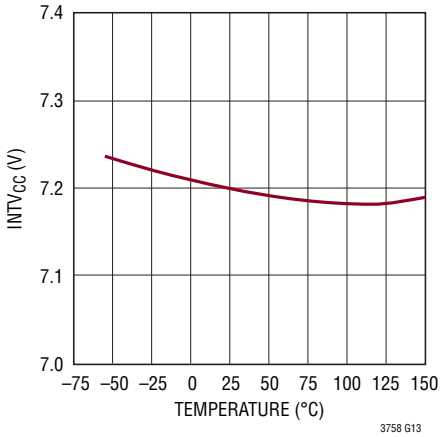


$\overline{SHDN}$/UVLO Hysteresis Current vs Temperature

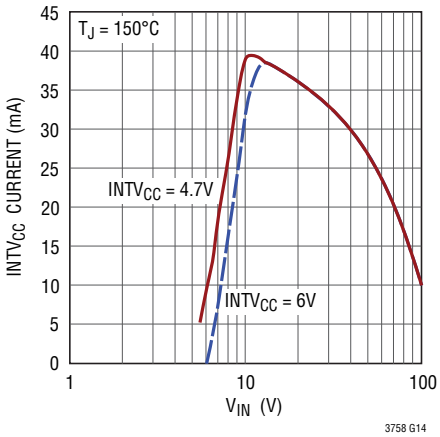


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

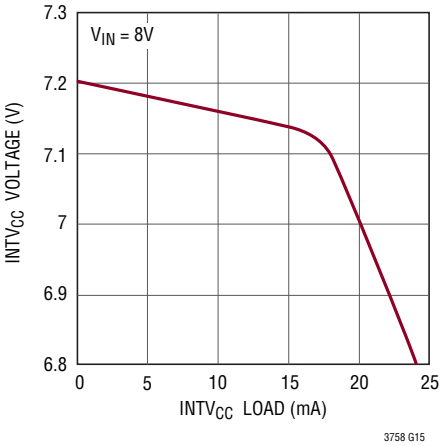
$INTV_{CC}$ vs Temperature



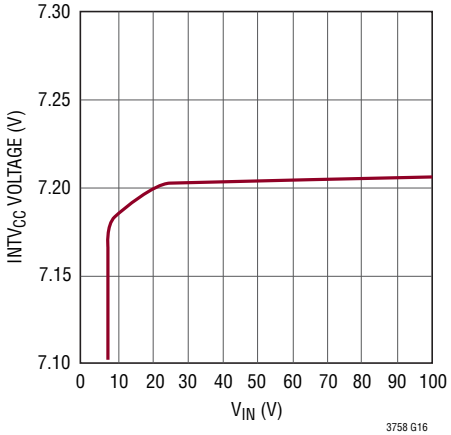
$INTV_{CC}$ Minimum Output Current vs V_{IN}



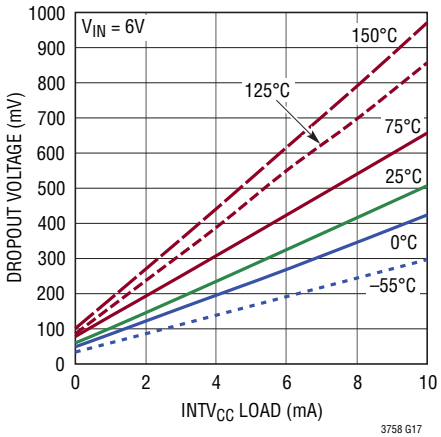
$INTV_{CC}$ Load Regulation



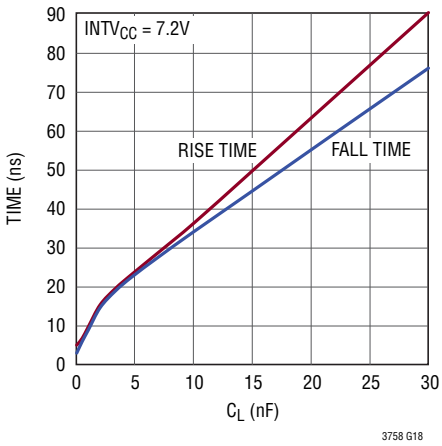
$INTV_{CC}$ Line Regulation



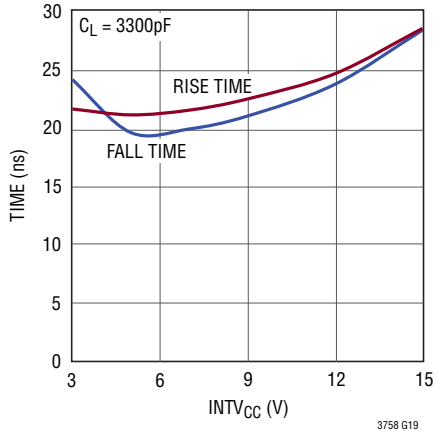
$INTV_{CC}$ Dropout Voltage vs Current, Temperature



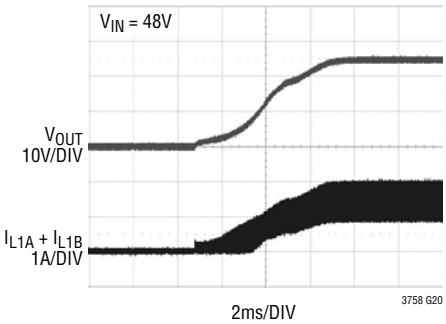
Gate Drive Rise and Fall Time vs C_L



Gate Drive Rise and Fall Time vs $INTV_{CC}$

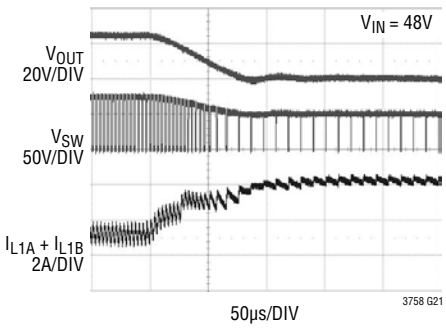


Typical Start-Up Waveforms



SEE TYPICAL APPLICATION: 18V TO 72V INPUT, 24V OUTPUT SEPIC CONVERTER

FBX Frequency Foldback Waveforms During Overcurrent



SEE TYPICAL APPLICATION: 18V TO 72V INPUT, 24V OUTPUT SEPIC CONVERTER

PIN FUNCTIONS

V_C (Pin 1): Error Amplifier Compensation Pin. Used to stabilize the voltage loop with an external RC network.

FBX (Pin 2): Positive and Negative Feedback Pin. Receives the feedback voltage from the external resistor divider across the output. Also modulates the switching frequency during start-up and fault conditions when FBX is close to GND.

SS (Pin 3): Soft-Start Pin. This pin modulates compensation pin voltage (V_C) clamp. The soft-start interval is set with an external capacitor. The pin has a 10µA (typical) pull-up current source to an internal 2.5V rail. The soft-start pin is reset to GND by an undervoltage condition at $\overline{SHDN}$/UVLO, an $INTV_{CC}$ undervoltage or overvoltage condition or an internal thermal lockout.

RT (Pin 4): Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND. Do not leave this pin open.

SYNC (Pin 5): Frequency Synchronization Pin. Used to synchronize the switching frequency to an outside clock. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than the SYNC pulse frequency. Tie the SYNC pin to GND if this feature is not used. SYNC is bypassed when FBX is close to GND.

SENSE (Pin 6): The Current Sense Input for the Control Loop. Kelvin connect this pin to the positive terminal of the switch current sense resistor in the source of the NFET. The negative terminal of the current sense resistor should be connected to GND plane close to the IC.

GATE (Pin 7): N-Channel MOSFET Gate Driver Output. Switches between $INTV_{CC}$ and GND. Driven to GND when IC is shut down, during thermal lockout or when $INTV_{CC}$ is above or below the overvoltage or UV thresholds, respectively.

$INTV_{CC}$ (Pin 8): Regulated Supply for Internal Loads and Gate Driver. Supplied from V_{IN} and regulated to 7.2V (typical). $INTV_{CC}$ must be bypassed with a minimum of 4.7µF capacitor placed close to pin. $INTV_{CC}$ can be connected directly to V_{IN}, if V_{IN} is less than 17.5V. $INTV_{CC}$ can also be connected to a power supply whose voltage is higher than 7.5V, and lower than V_{IN}, provided that supply does not exceed 17.5V.

$\overline{SHDN}$/UVLO (Pin 9): Shutdown and Undervoltage Detect Pin. An accurate 1.22V (nominal) falling threshold with externally programmable hysteresis detects when power is okay to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 2µA pull-down current. An undervoltage condition resets sort-start. Tie to 0.4V, or less, to disable the device and reduce V_{IN} quiescent current below 1µA.

V_{IN} (Pin 10): Input Supply Pin. Must be locally bypassed with a 0.22µF, or larger, capacitor placed close to the pin.

Exposed Pad (Pin 11): Ground. This pin also serves as the negative terminal of the current sense resistor. The exposed pad must be soldered directly to the local ground plane.

BLOCK DIAGRAM

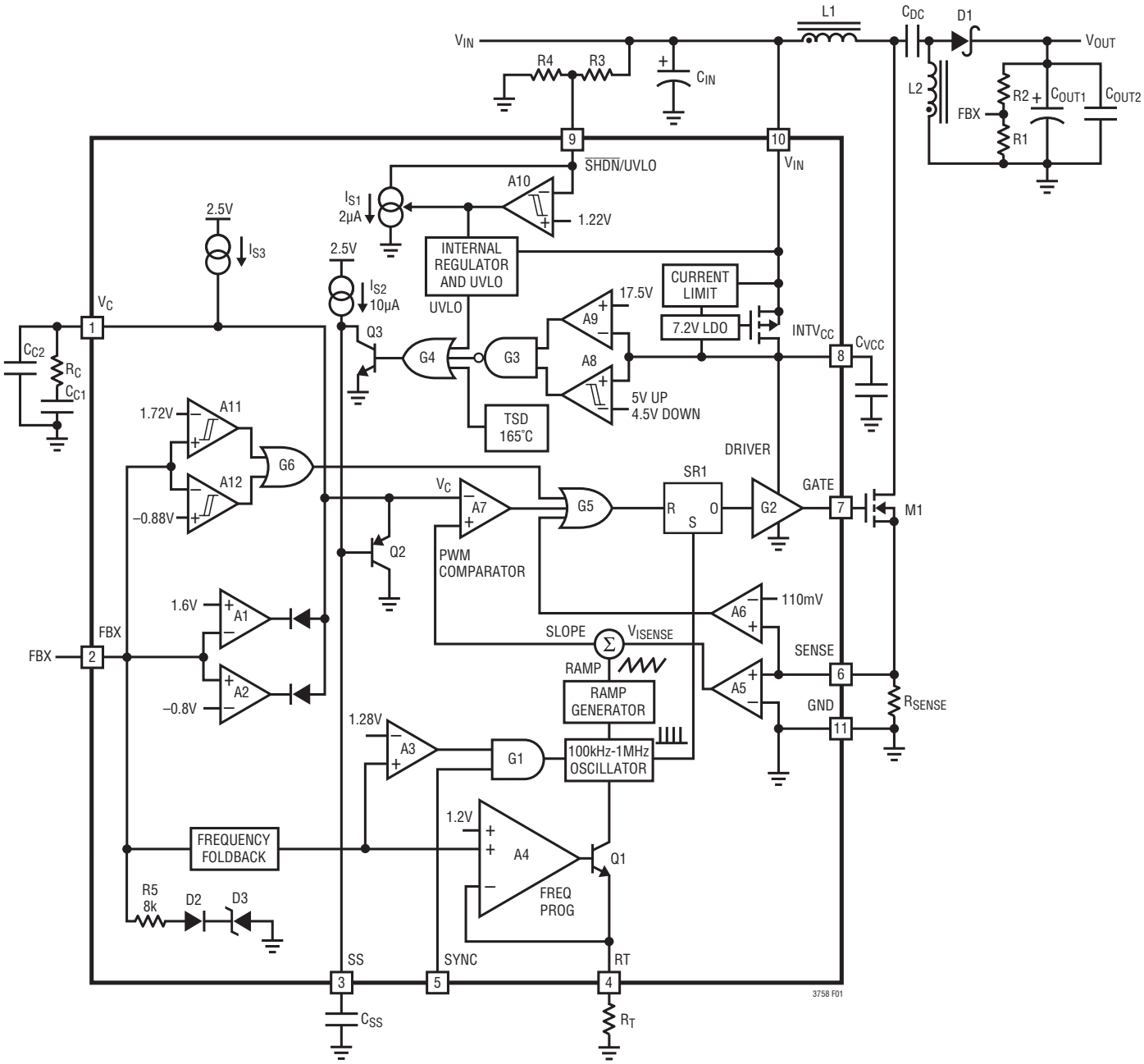


Figure 1. LT3758 Block Diagram Working as a SEPIC Converter

APPLICATIONS INFORMATION

Main Control Loop

The LT3758 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram in Figure 1.

The start of each oscillator cycle sets the SR latch (SR1) and turns on the external power MOSFET switch M1 through driver G2. The switch current flows through the external current sensing resistor R_{SENSE} and generates a voltage proportional to the switch current. This current sense voltage V_{ISENSE} (amplified by A5) is added to a stabilizing slope compensation ramp and the resulting sum (SLOPE) is fed into the positive terminal of the PWM comparator A7. When SLOPE exceeds the level at the negative input of A7 (V_C pin), SR1 is reset, turning off the power switch. The level at the negative input of A7 is set by the error amplifier A1 (or A2) and is an amplified version of the difference between the feedback voltage (FBX pin) and the reference voltage (1.6V or –0.8V, depending on the configuration). In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation.

The LT3758 has a switch current limit function. The current sense voltage is input to the current limit comparator A6. If the SENSE pin voltage is higher than the sense current limit threshold $V_{SENSE(MAX)}$ (110mV, typical), A6 will reset SR1 and turn off M1 immediately.

The LT3758 is capable of generating either positive or negative output voltage with a single FBX pin. It can be configured as a boost, flyback or SEPIC converter to generate positive output voltage, or as an inverting converter to generate negative output voltage. When configured as a SEPIC converter, as shown in Figure 1, the FBX pin is pulled up to the internal bias voltage of 1.6V by a voltage divider (R1 and R2) connected from V_{OUT} to GND. Comparator A2 becomes inactive and comparator A1 performs the inverting amplification from FBX to V_C. When the LT3758 is in an inverting configuration, the FBX pin is pulled down to –0.8V by a voltage divider connected from V_{OUT} to GND. Comparator A1 becomes inactive and comparator A2 performs the noninverting amplification from FBX to V_C.

The LT3758 has overvoltage protection functions to protect the converter from excessive output voltage overshoot during start-up or recovery from a short-circuit condition. An overvoltage comparator A11 (with 20mV hysteresis) senses when the FBX pin voltage exceeds the positive regulated voltage (1.6V) by 8% and provides a reset pulse. Similarly, an overvoltage comparator A12 (with 10mV hysteresis) senses when the FBX pin voltage exceeds the negative regulated voltage (–0.8V) by 11% and provides a reset pulse. Both reset pulses are sent to the main RS latch (SR1) through G6 and G5. The power MOSFET switch M1 is actively held off for the duration of an output overvoltage condition.

Programming Turn-On and Turn-Off Thresholds with the $\overline{SHDN}$/UVLO Pin

The $\overline{SHDN}$/UVLO pin controls whether the LT3758 is enabled or is in shutdown state. A micropower 1.22V reference, a comparator A10 and a controllable current source I_{S1} allow the user to accurately program the supply voltage at which the IC turns on and off. The falling value can be accurately set by the resistor dividers R3 and R4. When $\overline{SHDN}$/UVLO is above 0.4V, and below the 1.22V threshold, the small pull-down current source I_{S1} (typical 2µA) is active.

The purpose of this current is to allow the user to program the rising hysteresis. The Block Diagram of the comparator and the external resistors is shown in Figure 1. The typical falling threshold voltage and rising threshold voltage can be calculated by the following equations:

$$V_{VIN,FALLING} = 1.22 \bullet \frac{(R3+R4)}{R4}$$

$$V_{VIN,RISING} = 2\mu A \bullet R3 + V_{IN,FALLING}$$

For applications where the $\overline{SHDN}$/UVLO pin is only used as a logic input, the $\overline{SHDN}$/UVLO pin can be connected directly to the input voltage V_{IN} through a 1k resistor for always-on operation.

APPLICATIONS INFORMATION

$INTV_{CC}$ Regulator Bypassing and Operation

An internal, low dropout (LDO) voltage regulator produces the 7.2V $INTV_{CC}$ supply which powers the gate driver, as shown in Figure 1. The LT3758 contains an undervoltage lockout comparator A8 and an overvoltage lockout comparator A9 for the $INTV_{CC}$ supply. The $INTV_{CC}$ undervoltage (UV) threshold is 4.5V (typical), with 0.5V hysteresis, to ensure that the MOSFETs have sufficient gate drive voltage before turning on. The logic circuitry within the LT3758 is also powered from the internal $INTV_{CC}$ supply.

The $INTV_{CC}$ overvoltage threshold is set to be 17.5V (typical) to protect the gate of the power MOSFET. When $INTV_{CC}$ is below the UV threshold, or above the overvoltage threshold, the GATE pin will be forced to GND and the soft-start operation will be triggered.

The $INTV_{CC}$ regulator must be bypassed to ground immediately adjacent to the IC pins with a minimum of 4.7µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

In an actual application, most of the IC supply current is used to drive the gate capacitance of the power MOSFET. The on-chip power dissipation can be a significant concern when a large power MOSFET is being driven at a high frequency and the V_{IN} voltage is high. It is important to limit the power dissipation through selection of MOSFET and/or operating frequency so the LT3758 does not exceed its maximum junction temperature rating. The junction temperature T_J can be estimated using the following equations:

$$T_J = T_A + P_{IC} \bullet \theta_{JA}$$

T_A = ambient temperature

θ_{JA} = junction-to-ambient thermal resistance

P_{IC} = IC power consumption

$= V_{IN} \bullet (I_Q + I_{DRIVE})$

$I_Q = V_{IN}$ operation $I_Q = 1.6mA$

I_{DRIVE} = average gate drive current = $f \bullet Q_G$

f = switching frequency

Q_G = power MOSFET total gate charge

The LT3758 uses packages with an Exposed Pad for enhanced thermal conduction. With proper soldering to the Exposed Pad on the underside of the package and a full copper plane underneath the device, thermal resistance (θ_{JA}) will be about 43°C/W for the DD package and 40°C/W for the MSE package. For an ambient board temperature of T_A = 70°C and maximum junction temperature of 125°C, the maximum I_{DRIVE} ($I_{DRIVE(MAX)}$) of the DD package can be calculated as:

$$I_{DRIVE(MAX)} = \frac{(T_J - T_A)}{(\theta_{JA} \bullet V_{IN})} - I_Q = \frac{1.28W}{V_{IN}} - 1.6mA$$

The LT3758 has an internal $INTV_{CC}$ I_{DRIVE} current limit function to protect the IC from excessive on-chip power dissipation. The I_{DRIVE} current limit decreases as the V_{IN} increases (see the $INTV_{CC}$ Minimum Output Current vs V_{IN} graph in the Typical Performance Characteristics section). If I_{DRIVE} reaches the current limit, $INTV_{CC}$ voltage will fall and may trigger the soft-start.

Based on the preceding equation and the $INTV_{CC}$ Minimum Output Current vs V_{IN} graph, the user can calculate the maximum MOSFET gate charge the LT3758 can drive at a given V_{IN} and switch frequency. A plot of the maximum Q_G vs V_{IN} at different frequencies to guarantee a minimum 4.7V $INTV_{CC}$ is shown in Figure 2.

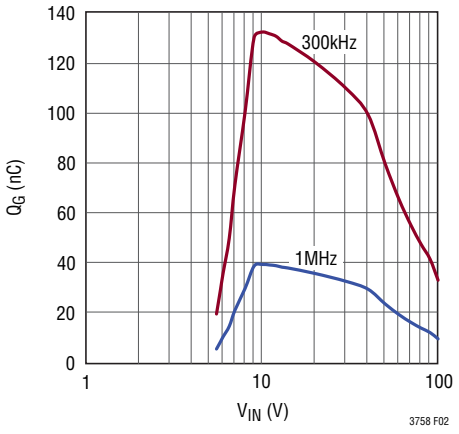


Figure 2. Recommended Maximum Q_G vs V_{IN} at Different Frequencies to Ensure $INTV_{CC}$ Higher Than 4.7V

APPLICATIONS INFORMATION

As illustrated in Figure 2, a trade-off between the operating frequency and the size of the power MOSFET may be needed in order to maintain a reliable IC junction temperature. Prior to lowering the operating frequency, however, be sure to check with power MOSFET manufacturers for their most recent low Q_G, low $R_{DS(ON)}$ devices. Power MOSFET manufacturing technologies are continually improving, with newer and better performance devices being introduced almost yearly.

An effective approach to reduce the power consumption of the internal LDO for gate drive is to tie the $INTV_{CC}$ pin to an external voltage source high enough to turn off the internal LDO regulator.

If the input voltage V_{IN} does not exceed the absolute maximum rating of both the power MOSFET gate-source voltage (V_{GS}) and the $INTV_{CC}$ overvoltage lockout threshold voltage (17.5V), the $INTV_{CC}$ pin can be shorted directly to the V_{IN} pin. In this condition, the internal LDO will be turned off and the gate driver will be powered directly from the input voltage V_{IN}. With the $INTV_{CC}$ pin shorted to V_{IN}, however, a small current (around 16µA) will load the $INTV_{CC}$ in shutdown mode. For applications that require the lowest shutdown mode input supply current, do not connect the $INTV_{CC}$ pin to V_{IN}.

In SEPIC or flyback applications, the $INTV_{CC}$ pin can be connected to the output voltage V_{OUT} through a blocking diode, as shown in Figure 3, if V_{OUT} meets the following conditions:

1. $V_{OUT} < V_{IN}$ (pin voltage)
2. $V_{OUT} < 17.5V$
3. V_{OUT} < maximum V_{GS} rating of power MOSFET

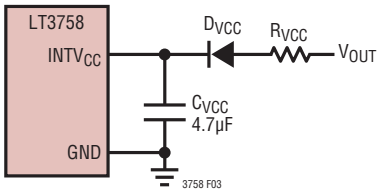


Figure 3. Connecting $INTV_{CC}$ to V_{OUT}

A resistor R_{VCC} can be connected, as shown in Figure 3, to limit the inrush current from V_{OUT}. Regardless of whether or not the $INTV_{CC}$ pin is connected to an external voltage source, it is always necessary to have the driver circuitry bypassed with a 4.7µF low ESR ceramic capacitor to ground immediately adjacent to the $INTV_{CC}$ and GND pins.

Operating Frequency and Synchronization

The choice of operating frequency may be determined by on-chip power dissipation, otherwise it is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing gate drive current and MOSFET and diode switching losses. However, lower frequency operation requires a physically larger inductor. Switching frequency also has implications for loop compensation. The LT3758 uses a constant-frequency architecture that can be programmed over a 100kHz to 1000kHz range with a single external resistor from the RT pin to ground, as shown in Figure 1. The RT pin must have an external resistor to GND for proper operation of the LT3758. A table for selecting the value of R_T for a given operating frequency is shown in Table 1.

Table 1. Timing Resistor (R_T) Value

SWITCHING FREQUENCY (kHz)	R_T (kΩ)
100	140
200	63.4
300	41.2
400	30.9
500	24.3
600	19.6
700	16.5
800	14
900	12.1
1000	10.5

The operating frequency of the LT3758 can be synchronized to an external clock source. By providing a digital clock signal into the SYNC pin, the LT3758 will operate at the SYNC clock frequency. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. It is recommended the SYNC pulse have a minimum pulse width of 200ns. Tie the SYNC pin to GND if this feature is not used.

APPLICATIONS INFORMATION

Duty Cycle Consideration

Switching duty cycle is a key variable defining converter operation. As such, its limits must be considered. Minimum on-time is the smallest time duration that the LT3758 is capable of turning on the power MOSFET. This time is generally about 220ns (typical) (see Minimum On-Time in the Electrical Characteristics table). In each switching cycle, the LT3758 keeps the power switch off for at least 220ns (typical) (see Minimum Off-Time in the Electrical Characteristics table).

The minimum on-time and minimum off-time and the switching frequency define the minimum and maximum switching duty cycles a converter is able to generate:

Minimum duty cycle = minimum on-time • frequency

Maximum duty cycle = 1 – (minimum off-time • frequency)

Programming the Output Voltage

The output voltage V_{OUT} is set by a resistor divider, as shown in Figure 1. The positive and negative V_{OUT} are set by the following equations:

$$V_{OUT,POSITIVE} = 1.6V \bullet \left(1 + \frac{R2}{R1}\right)$$

$$V_{OUT,NEGATIVE} = -0.8V \bullet \left(1 + \frac{R2}{R1}\right)$$

The resistors R1 and R2 are typically chosen so that the error caused by the current flowing into the FBX pin during normal operation is less than 1% (this translates to a maximum value of R1 at about 158k).

In the applications where V_{OUT} is pulled up by an external positive power supply, the FBX pin is also pulled up through the R2 and R1 network. Make sure the FBX does not exceed its absolute maximum rating (6V). The R5, D2, and D3 in Figure 1 provide a resistive clamp in the positive direction. To ensure FBX is lower than 6V, choose sufficiently large R1 and R2 to meet the following condition:

$$6V \bullet \left(1 + \frac{R2}{R1}\right) + 3.5V \bullet \frac{R2}{8k\Omega} > V_{OUT(MAX)}$$

where $V_{OUT(MAX)}$ is the maximum V_{OUT} that is pulled up by an external power supply.

Soft-Start

The LT3758 contains several features to limit peak switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition. The primary purpose of these features is to prevent damage to external components or the load.

High peak switch currents during start-up may occur in switching regulators. Since V_{OUT} is far from its final value, the feedback loop is saturated and the regulator tries to charge the output capacitor as quickly as possible, resulting in large peak currents. A large surge current may cause inductor saturation or power switch failure.

The LT3758 addresses this mechanism with the SS pin. As shown in Figure 1, the SS pin reduces the power MOSFET current by pulling down the V_C pin through Q2. In this way the SS allows the output capacitor to charge gradually toward its final value while limiting the start-up peak currents. The typical start-up waveforms are shown in the Typical Performance Characteristics section. The inductor current I_L slewing rate is limited by the soft-start function.

Besides start-up (with $\overline{SHDN}$/UVLO), soft-start can also be triggered by the following faults:

1. $INTV_{CC} > 17.5V$
2. $INTV_{CC} < 4.5V$
3. Thermal lockout

Any of these three faults will cause the LT3758 to stop switching immediately. The SS pin will be discharged by Q3. When all faults are cleared and the SS pin has been discharged below 0.2V, a 10µA current source I_{S2} starts charging the SS pin, initiating a soft-start operation.

The soft-start interval is set by the soft-start capacitor selection according to the equation:

$$T_{SS} = C_{SS} \bullet \frac{1.25V}{10\mu A}$$

APPLICATIONS INFORMATION

FBX Frequency Foldback

When V_{OUT} is very low during start-up or a GND fault on the output, the switching regulator must operate at low duty cycles to maintain the power switch current within the current limit range, since the inductor current decay rate is very low during switch off time. The minimum on-time limitation may prevent the switcher from attaining a sufficiently low duty cycle at the programmed switching frequency. So, the switch current will keep increasing through each switch cycle, exceeding the programmed current limit. To prevent the switch peak currents from exceeding the programmed value, the LT3758 contains a frequency foldback function to reduce the switching frequency when the FBX voltage is low (see the Normalized Switching Frequency vs FBX graph in the Typical Performance Characteristics section).

During frequency foldback, external clock synchronization is disabled to prevent interference with frequency reducing operation.

Thermal Lockout

If LT3758 die temperature reaches 165°C (typical), the part will go into thermal lockout. The power switch will be turned off. A soft-start operation will be triggered. The part will be enabled again when the die temperature has dropped by 5°C (nominal).

Loop Compensation

Loop compensation determines the stability and transient performance. The LT3758/LT3758A use current mode control to regulate the output which simplifies loop compensation. The LT3758A improves the no-load to heavy load transient response, when compared to the LT3758. New internal circuits ensure that the transient from not switching to switching at high current can be made in a few cycles. The optimum values depend on the converter topology, the component values and the operating conditions (including the input voltage, load current, etc.). To compensate the feedback loop of the LT3758/LT3758A, a series resistor-capacitor network is usually connected from the V_C pin to GND. Figure 1 shows the typical V_C compensation network. For most applications, the capacitor should be in the range of 470pF to 22nF, and the resistor should be in the range of 5k to 50k. A small capacitor is often connected in parallel with the RC compensation network to attenuate the V_C voltage ripple induced from the output voltage ripple through the internal error amplifier. The parallel capacitor usually ranges in value from 10pF to 100pF. A practical approach to design the compensation network is to start with one of the circuits in this data sheet that is similar to your application, and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature.

SENSE Pin Programming

For control and protection, the LT3758 measures the power MOSFET current by using a sense resistor (R_{SENSE}) between GND and the MOSFET source. Figure 4 shows a typical waveform of the sense voltage (V_{SENSE}) across the sense resistor. It is important to use Kelvin traces between the SENSE pin and R_{SENSE}, and to place the IC GND as close as possible to the GND terminal of the R_{SENSE} for proper operation.

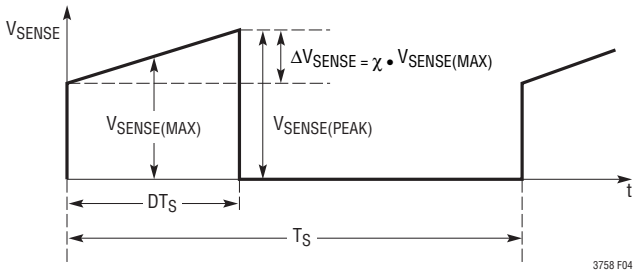


Figure 4. The Sense Voltage During a Switching Cycle

APPLICATIONS INFORMATION

Due to the current limit function of the SENSE pin, R_{SENSE} should be selected to guarantee that the peak current sense voltage $V_{SENSE(PEAK)}$ during steady state normal operation is lower than the SENSE current limit threshold (see the Electrical Characteristics table). Given a 20% margin, $V_{SENSE(PEAK)}$ is set to be 80mV. Then, the maximum switch ripple current percentage can be calculated using the following equation:

$$\chi = \frac{\Delta V_{SENSE}}{80mV - 0.5 \bullet \Delta V_{SENSE}}$$

χ is used in subsequent design examples to calculate inductor value. ΔV_{SENSE} is the ripple voltage across R_{SENSE}.

The LT3758 switching controller incorporates 100ns timing interval to blank the ringing on the current sense signal immediately after M1 is turned on. This ringing is caused by the parasitic inductance and capacitance of the PCB trace, the sense resistor, the diode, and the MOSFET. The 100ns timing interval is adequate for most of the LT3758 applications. In the applications that have very large and long ringing on the current sense signal, a small RC filter can be added to filter out the excess ringing. Figure 5 shows the RC filter on the SENSE pin. It is usually sufficient to choose 22Ω for R_{FLT} and 2.2nF to 10nF for C_{FLT}. Keep R_{FLT}'s resistance low. Remember that there is 65µA (typical) flowing out of the SENSE pin. Adding R_{FLT} will affect the SENSE current limit threshold:

$$V_{SENSE\_ILIM} = 110mV - 65\mu A \bullet R_{FLT}$$

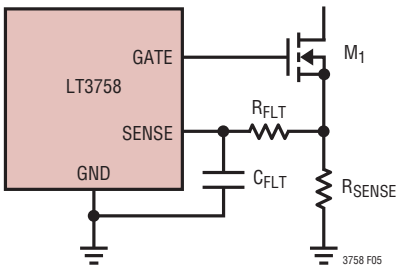


Figure 5. The RC Filter on the SENSE Pin

APPLICATION CIRCUITS

The LT3758 can be configured as different topologies. The first topology to be analyzed will be the boost converter, followed by the flyback, SEPIC and inverting converters.

Boost Converter: Switch Duty Cycle and Frequency

The LT3758 can be configured as a boost converter for the applications where the converter output voltage is higher than the input voltage. Remember that boost converters are not short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability. For applications requiring a step-up converter that is short-circuit protected, please refer to the Applications Information section covering SEPIC converters.

The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

in continuous conduction mode (CCM).

For a boost converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

Discontinuous conduction mode (DCM) provides higher conversion ratios at a given frequency at the cost of reduced efficiencies and higher switching currents.

Boost Converter: Inductor and Sense Resistor Selection

For the boost topology, the maximum average inductor current is:

$$I_{L(MAX)} = I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

Then, the ripple current can be calculated by:

$$\Delta I_L = \chi \bullet I_{L(MAX)} = \chi \bullet I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

APPLICATIONS INFORMATION

The constant χ in the preceding equation represents the percentage peak-to-peak ripple current in the inductor, relative to $I_{L(MAX)}$.

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_L provides fast transient response and allows the use of low inductances, but results in higher input current ripple and greater core losses. It is recommended that χ fall within the range of 0.2 to 0.6.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value of the boost converter can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

The peak and RMS inductor current are:

$$I_{L(PEAK)} = I_{L(MAX)} \bullet \left(1 + \frac{\chi}{2}\right)$$

$$I_{L(RMS)} = I_{L(MAX)} \bullet \sqrt{1 + \frac{\chi^2}{12}}$$

Based on these equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

Set the sense voltage at $I_{L(PEAK)}$ to be the minimum of the SENSE current limit threshold with a 20% margin. The sense resistor value can then be calculated to be:

$$R_{SENSE} = \frac{80mV}{I_{L(PEAK)}}$$

Boost Converter: Power MOSFET Selection

Important parameters for the power MOSFET include the drain-source voltage rating (V_{DS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$), the gate to source and gate to drain charges (Q_{GS} and Q_{GD}), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistances ($R_{\theta JC}$ and $R_{\theta JA}$).

The power MOSFET will see full output voltage, plus a diode forward voltage, and any additional ringing across its drain-to-source during its off-time. It is recommended to choose a MOSFET whose B_{VDSS} is higher than V_{OUT} by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the MOSFET in a boost converter is:

$$P_{FET} = I^2_{L(MAX)} \bullet R_{DS(ON)} \bullet D_{MAX} + 2 \bullet V^2_{OUT} \bullet I_{L(MAX)} \bullet C_{RSS} \bullet f/1A$$

The first term in the preceding equation represents the conduction losses in the device, and the second term, the switching loss. C_{RSS} is the reverse transfer capacitance, which is usually specified in the MOSFET characteristics.

For maximum efficiency, $R_{DS(ON)}$ and C_{RSS} should be minimized. From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A + P_{FET} \bullet \theta_{JA} = T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

Boost Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desirable. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage plus any additional ringing across its anode-to-cathode during the on-time. The average forward current in normal operation is equal to the output current, and the peak current is equal to:

$$I_{D(PEAK)} = I_{L(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{L(MAX)}$$

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than V_{OUT} by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

APPLICATIONS INFORMATION

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Boost Converter: Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct output capacitors for a given output ripple voltage. The effect of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform for a typical boost converter is illustrated in Figure 6.

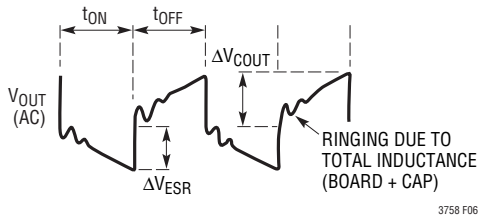


Figure 6. The Output Ripple Waveform of a Boost Converter

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step ΔV_{ESR} and the charging/discharging ΔV_{COUT}. For the purpose of simplicity, we will choose 2% for the maximum output ripple, to be divided equally between ΔV_{ESR} and ΔV_{COUT}. This percentage ripple will change, depending on the requirements of the application, and the following equations can easily be modified. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \leq \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet V_{OUT} \bullet f}$$

The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 6. The RMS ripple current rating of the output capacitor can be determined using the following equation:

$$I_{RMS(COUT)} \geq I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1-D_{MAX}}}$$

Multiple capacitors are often paralleled to meet ESR requirements. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the required RMS current rating. Additional ceramic capacitors in parallel are commonly used to reduce the effect of parasitic inductance in the output capacitor, which reduces high frequency switching noise on the converter output.

Boost Converter: Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input, and the input current waveform is continuous. The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \Delta I_L$$

FLYBACK CONVERTER APPLICATIONS

The LT3758 can be configured as a flyback converter for the applications where the converters have multiple outputs, high output voltages or isolated outputs. Figure 7 shows a simplified flyback converter.

The flyback converter has a very low parts count for multiple outputs, and with prudent selection of turns ratio, can have high output/input voltage conversion ratios with a desirable duty cycle. However, it has low efficiency due to the high peak currents, high peak voltages and consequent power loss. The flyback converter is commonly used for an output power of less than 50W.

APPLICATIONS INFORMATION

The flyback converter can be designed to operate either in continuous or discontinuous mode. Compared to continuous mode, discontinuous mode has the advantage of smaller transformer inductances and easy loop compensation, and the disadvantage of higher peak-to-average current and lower efficiency.

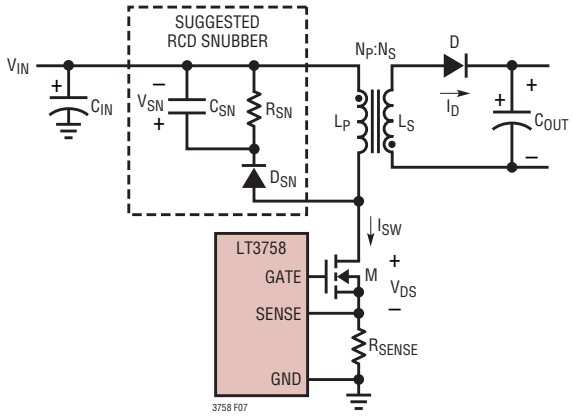


Figure 7. A Simplified Flyback Converter

Flyback Converter: Switch Duty Cycle and Turns Ratio

The flyback converter conversion ratio in the continuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{1-D}$$

Where N_S/N_P is the second to primary turns ratio.

Figure 8 shows the waveforms of the flyback converter in discontinuous mode operation. During each switching period T_S, three subintervals occur: DT_S, $D2T_S$, $D3T_S$. During DT_S, M is on, and D is reverse-biased. During $D2T_S$, M is off, and L_S is conducting current. Both L_P and L_S currents are zero during $D3T_S$.

The flyback converter conversion ratio in the discontinuous mode operation is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{N_S}{N_P} \bullet \frac{D}{D2}$$

According to the preceding equations, the user has relative freedom in selecting the switch duty cycle or turns ratio to suit a given application. The selections of the duty cycle and the turns ratio are somewhat iterative processes, due to the number of variables involved. The user can choose either a duty cycle or a turns ratio as the start point. The following trade-offs should be considered when selecting the switch duty cycle or turns ratio, to optimize the converter performance. A higher duty cycle affects the flyback converter in the following aspects:

- Lower MOSFET RMS current $I_{SW(RMS)}$, but higher MOSFET V_{DS} peak voltage
- Lower diode peak reverse voltage, but higher diode RMS current $I_{D(RMS)}$
- Higher transformer turns ratio (N_P/N_S)

The choice,

$$\frac{D}{D+D2} = \frac{1}{3}$$

(for discontinuous mode operation with a given D3) gives the power MOSFET the lowest power stress (the product of RMS current and peak voltage). The choice,

$$\frac{D}{D+D2} = \frac{2}{3}$$

(for discontinuous mode operation with a given D3) gives the diode the lowest power stress (the product of RMS current and peak voltage). An extreme high or low duty cycle results in high power stress on the MOSFET or diode, and reduces efficiency. It is recommended to choose a duty cycle between 20% and 80%.

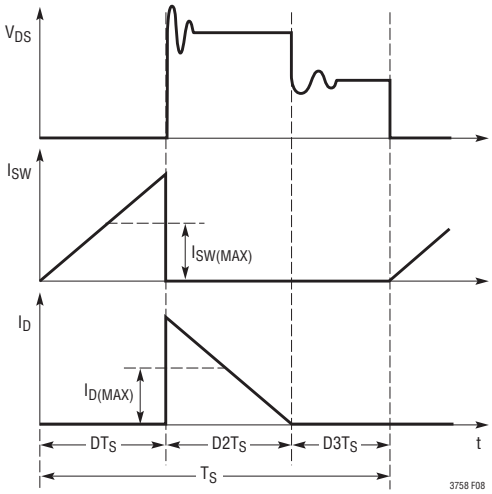


Figure 8. Waveforms of the Flyback Converter in Discontinuous Mode Operation

APPLICATIONS INFORMATION

Flyback Converter: Transformer Design for Discontinuous Mode Operation

The transformer design for discontinuous mode of operation is chosen as presented here. According to Figure 8, the minimum D3 ($D3_{MIN}$) occurs when the the converter has the minimum V_{IN} and the maximum output power (P_{OUT}). Choose $D3_{MIN}$ to be equal to or higher than 10% to guarantee the converter is always in discontinuous mode operation. Choosing higher D3 allows the use of low inductances but results in higher switch peak current. The user can choose a D_{MAX} as the start point. Then, the maximum average primary currents can be calculated by the following equation:

$$I_{LP(MAX)} = I_{SW(MAX)} = \frac{P_{OUT(MAX)}}{D_{MAX} \bullet V_{IN(MIN)} \bullet \eta}$$

where η is the converter efficiency.

If the flyback converter has multiple outputs, $P_{OUT(MAX)}$ is the sum of all the output power.

The maximum average secondary current is:

$$I_{LS(MAX)} = I_{D(MAX)} = \frac{I_{OUT(MAX)}}{D2}$$

where

$D2 = 1 - D_{MAX} - D3$

the primary and secondary RMS currents are:

$$I_{LP(RMS)} = 2 \bullet I_{LP(MAX)} \bullet \sqrt{\frac{D_{MAX}}{3}}$$

$$I_{LS(RMS)} = 2 \bullet I_{LS(MAX)} \bullet \sqrt{\frac{D2}{3}}$$

According to Figure 8, the primary and secondary peak currents are:

$$I_{LP(PEAK)} = I_{SW(PEAK)} = 2 \bullet I_{LP(MAX)}$$

$$I_{LS(PEAK)} = I_{D(PEAK)} = 2 \bullet I_{LS(MAX)}$$

The primary and second inductor values of the flyback converter transformer can be determined using the following equations:

$$L_P = \frac{D^2_{MAX} \bullet V^2_{IN(MIN)} \bullet \eta}{2 \bullet P_{OUT(MAX)} \bullet f}$$

$$L_S = \frac{D2^2 \bullet (V_{OUT} + V_D)}{2 \bullet I_{OUT(MAX)} \bullet f}$$

The primary to second turns ratio is:

$$\frac{N_P}{N_S} = \sqrt{\frac{L_P}{L_S}}$$

Flyback Converter: Snubber Design

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to occur after the MOSFET turn-off. This is increasingly prominent at higher load currents, where more stored energy must be dissipated. In some cases a snubber circuit will be required to avoid overvoltage breakdown at the MOSFET's drain node. There are different snubber circuits, and Application Note 19 is a good reference on snubber design. An RCD snubber is shown in Figure 7.

The snubber resistor value (R_{SN}) can be calculated by the following equation:

$$R_{SN} = 2 \bullet \frac{V^2_{SN} - V_{SN} \bullet V_{OUT} \bullet \frac{N_P}{N_S}}{I^2_{SW(PEAK)} \bullet L_{LK} \bullet f}$$

where V_{SN} is the snubber capacitor voltage. A smaller V_{SN} results in a larger snubber loss. A reasonable V_{SN} is 2 to 2.5 times of:

$$\frac{V_{OUT} \bullet N_P}{N_S}$$

APPLICATIONS INFORMATION

L_{LK} is the leakage inductance of the primary winding, which is usually specified in the transformer characteristics. L_{LK} can be obtained by measuring the primary inductance with the secondary windings shorted. The snubber capacitor value (C_{CN}) can be determined using the following equation:

$$C_{CN} = \frac{V_{SN}}{\Delta V_{SN} \bullet R_{CN} \bullet f}$$

where ΔV_{SN} is the voltage ripple across C_{CN}. A reasonable ΔV_{SN} is 5% to 10% of V_{SN}. The reverse voltage rating of D_{SN} should be higher than the sum of V_{SN} and $V_{IN(MAX)}$.

Flyback Converter: Sense Resistor Selection

In a flyback converter, when the power switch is turned on, the current flowing through the sense resistor (I_{SENSE}) is:

$$I_{SENSE} = I_{LP}$$

Set the sense voltage at $I_{LP(PEAK)}$ to be the minimum of the SENSE current limit threshold with a 20% margin. The sense resistor value can then be calculated to be:

$$R_{SENSE} = \frac{80mV}{I_{LP(PEAK)}}$$

Flyback Converter: Power MOSFET Selection

For the flyback configuration, the MOSFET is selected with a V_{DC} rating high enough to handle the maximum V_{IN}, the reflected secondary voltage and the voltage spike due to the leakage inductance. Approximate the required MOSFET V_{DC} rating using:

$$BV_{DSS} > V_{DS(PEAK)}$$

where

$$V_{DS(PEAK)} = V_{IN(MAX)} + V_{SN}$$

The power dissipated by the MOSFET in a flyback converter is:

$$P_{FET} = I^2_{M(RMS)} \bullet R_{DS(ON)} + 2 \bullet V^2_{DS(PEAK)} \bullet I_{L(MAX)} \bullet C_{RSS} \bullet f/1A$$

The first term in this equation represents the conduction losses in the device, and the second term, the switching loss. C_{RSS} is the reverse transfer capacitance, which is usually specified in the MOSFET characteristics.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A + P_{FET} \bullet \theta_{JA} = T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

Flyback Converter: Output Diode Selection

The output diode in a flyback converter is subject to large RMS current and peak reverse voltage stresses. A fast switching diode with a low forward drop and a low reverse leakage is desired. Schottky diodes are recommended if the output voltage is below 100V.

Approximate the required peak repetitive reverse voltage rating V_{RRM} using:

$$V_{RRM} > \frac{N_S}{N_P} \bullet V_{IN(MAX)} + V_{OUT}$$

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ to be used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

Flyback Converter: Output Capacitor Selection

The output capacitor of the flyback converter has a similar operation condition as that of the boost converter. Refer to the Boost Converter: Output Capacitor Selection section for the calculation of C_{OUT} and ESR_{COUT}.

The RMS ripple current rating of the output capacitors in discontinuous operation can be determined using the following equation:

$$I_{RMS(COUT),DISCONTINUOUS} \geq I_{O(MAX)} \bullet \sqrt{\frac{4-(3 \bullet D2)}{3 \bullet D2}}$$

APPLICATIONS INFORMATION

Flyback Converter: Input Capacitor Selection

The input capacitor in a flyback converter is subject to a large RMS current due to the discontinuous primary current. To prevent large voltage transients, use a low ESR input capacitor sized for the maximum RMS current. The RMS ripple current rating of the input capacitors in discontinuous operation can be determined using the following equation:

$$I_{RMS(CIN),DISCONTINUOUS} \geq \frac{P_{OUT(MAX)}}{V_{IN(MIN)} \bullet \eta} \bullet \sqrt{\frac{4-(3 \bullet D_{MAX})}{3 \bullet D_{MAX}}}$$

SEPIC CONVERTER APPLICATIONS

The LT3758 can be configured as a SEPIC (single-ended primary inductance converter), as shown in Figure 1. This topology allows for the input to be higher, equal, or lower than the desired output voltage. The conversion ratio as a function of duty cycle is:

$$\frac{V_{OUT}+V_D}{V_{IN}} = \frac{D}{1-D}$$

in continuous conduction mode (CCM).

In a SEPIC converter, no DC path exists between the input and output. This is an advantage over the boost converter for applications requiring the output to be disconnected from the input source when the circuit is in shutdown.

Compared to the flyback converter, the SEPIC converter has the advantage that both the power MOSFET and the output diode voltages are clamped by the capacitors (C_{IN}, C_{DC} and C_{OUT}), therefore, there is less voltage ringing across the power MOSFET and the output diodes. The SEPIC converter requires much smaller input capacitors than those of the flyback converter. This is due to the fact that, in the SEPIC converter, the inductor L1 is in series with the input, and the ripple current flowing through the input capacitor is continuous.

SEPIC Converter: Switch Duty Cycle and Frequency

For a SEPIC converter operating in CCM, the duty cycle of the main switch can be calculated based on the output voltage (V_{OUT}), the input voltage (V_{IN}) and the diode forward voltage (V_D).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT}+V_D}{V_{IN(MIN)}+V_{OUT}+V_D}$$

SEPIC Converter: Inductor and Sense Resistor Selection

As shown in Figure 1, the SEPIC converter contains two inductors: L1 and L2. L1 and L2 can be independent, but can also be wound on the same core, since identical voltages are applied to L1 and L2 throughout the switching cycle.

For the SEPIC topology, the current through L1 is the converter input current. Based on the fact that, ideally, the output power is equal to the input power, the maximum average inductor currents of L1 and L2 are:

$$I_{L1(MAX)} = I_{IN(MAX)} = I_{O(MAX)} \bullet \frac{D_{MAX}}{1-D_{MAX}}$$

$$I_{L2(MAX)} = I_{O(MAX)}$$

In a SEPIC converter, the switch current is equal to I_{L1} + I_{L2} when the power switch is on, therefore, the maximum average switch current is defined as:

$$I_{SW(MAX)} = I_{L1(MAX)} + I_{L2(MAX)} = I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

and the peak switch current is:

$$I_{SW(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

The constant χ in the preceding equations represents the percentage peak-to-peak ripple current in the switch, relative to $I_{SW(MAX)}$, as shown in Figure 9. Then, the switch ripple current ΔI_{SW} can be calculated by:

$$\Delta I_{SW} = \chi \bullet I_{SW(MAX)}$$

The inductor ripple currents ΔI_{L1} and ΔI_{L2} are identical:

$$\Delta I_{L1} = \Delta I_{L2} = 0.5 \bullet \Delta I_{SW}$$

The inductor ripple current has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode).

APPLICATIONS INFORMATION

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher input current ripple and greater core losses. It is recommended that χ falls in the range of 0.2 to 0.6.

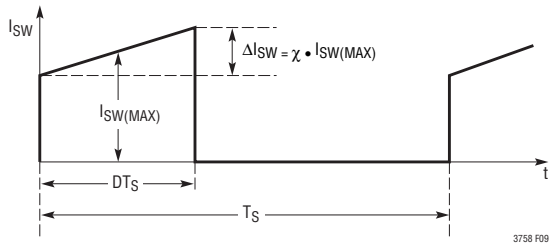


Figure 9. The Switch Current Waveform of the SEPIC Converter

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor, the inductor value (L1 and L2 are independent) of the SEPIC converter can be determined using the following equation:

$$L1 = L2 = \frac{V_{IN(MIN)}}{0.5 \bullet \Delta I_{SW} \bullet f} \bullet D_{MAX}$$

For most SEPIC applications, the equal inductor values will fall in the range of 1µH to 100µH.

By making L1 = L2, and winding them on the same core, the value of inductance in the preceding equation is replaced by 2L, due to mutual inductance:

$$L = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f} \bullet D_{MAX}$$

This maintains the same ripple current and energy storage in the inductors. The peak inductor currents are:

$$I_{L1(PEAK)} = I_{L1(MAX)} + 0.5 \bullet \Delta I_{L1}$$

$$I_{L2(PEAK)} = I_{L2(MAX)} + 0.5 \bullet \Delta I_{L2}$$

The RMS inductor currents are:

$$I_{L1(RMS)} = I_{L1(MAX)} \bullet \sqrt{1 + \frac{\chi_{L1}^2}{12}}$$

where

$$\chi_{L1} = \frac{\Delta I_{L1}}{I_{L1(MAX)}}$$

$$I_{L2(RMS)} = I_{L2(MAX)} \bullet \sqrt{1 + \frac{\chi_{L2}^2}{12}}$$

where

$$\chi_{L2} = \frac{\Delta I_{L2}}{I_{L2(MAX)}}$$

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

In a SEPIC converter, when the power switch is turned on, the current flowing through the sense resistor (I_{SENSE}) is the switch current.

Set the sense voltage at $I_{SENSE(PEAK)}$ to be the minimum of the SENSE current limit threshold with a 20% margin. The sense resistor value can then be calculated to be:

$$R_{SENSE} = \frac{80\,mV}{I_{SW(PEAK)}}$$

SEPIC Converter: Power MOSFET Selection

For the SEPIC configuration, choose a MOSFET with a V_{DC} rating higher than the sum of the output voltage and input voltage by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the MOSFET in a SEPIC converter is:

$$P_{FET} = I^2_{SW(MAX)} \bullet R_{DS(ON)} \bullet D_{MAX}$$

$$+ 2 \bullet (V_{IN(MIN)} + V_{OUT})^2 \bullet I_{L(MAX)} \bullet C_{RSS} \bullet f/1A$$

The first term in this equation represents the conduction losses in the device, and the second term, the switching loss. C_{RSS} is the reverse transfer capacitance, which is usually specified in the MOSFET characteristics.

For maximum efficiency, $R_{DS(ON)}$ and C_{RSS} should be minimized. From a known power dissipated in the power

APPLICATIONS INFORMATION

MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A + P_{FET} \bullet \theta_{JA} = T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

SEPIC Converter: Output Diode Selection

To maximize efficiency, a fast switching diode with a low forward drop and low reverse leakage is desirable. The average forward current in normal operation is equal to the output current, and the peak current is equal to:

$$I_{D(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet I_{O(MAX)} \bullet \frac{1}{1 - D_{MAX}}$$

It is recommended that the peak repetitive reverse voltage rating V_{RRM} is higher than $V_{OUT} + V_{IN(MAX)}$ by a safety margin (a 10V safety margin is usually sufficient).

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{\theta JA}$$

The $R_{\theta JA}$ used in this equation normally includes the $R_{\theta JC}$ for the device, plus the thermal resistance from the board, to the ambient temperature in the enclosure. T_J must not exceed the diode maximum junction temperature rating.

SEPIC Converter: Output and Input Capacitor Selection

The selections of the output and input capacitors of the SEPIC converter are similar to those of the boost converter. Please refer to the Boost Converter: Output Capacitor Selection and Boost Converter: Input Capacitor Selection sections.

SEPIC Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 1) should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{V_{OUT} + V_D}{V_{IN(MIN)}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

INVERTING CONVERTER APPLICATIONS

The LT3758 can be configured as a dual-inductor inverting topology, as shown in Figure 10. The V_{OUT} to V_{IN} ratio is:

$$\frac{V_{OUT} - V_D}{V_{IN}} = -\frac{D}{1 - D}$$

in continuous conduction mode (CCM).

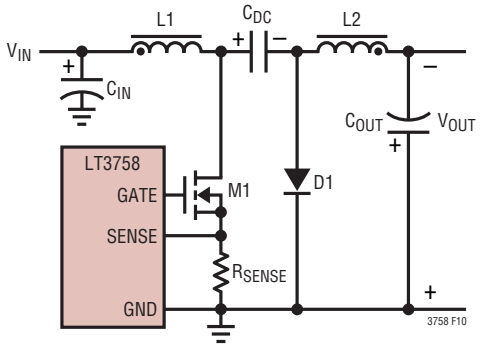


Figure 10. A Simplified Inverting Converter

Inverting Converter: Switch Duty Cycle and Frequency

For an inverting converter operating in CCM, the duty cycle of the main switch can be calculated based on the negative output voltage (V_{OUT}) and the input voltage (V_{IN}).

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_D}{V_{OUT} - V_D - V_{IN(MIN)}}$$

APPLICATIONS INFORMATION

Inverting Converter: Inductor, Sense Resistor, Power MOSFET, Output Diode and Input Capacitor Selections

The selections of the inductor, sense resistor, power MOSFET, output diode and input capacitor of an inverting converter are similar to those of the SEPIC converter. Please refer to the corresponding SEPIC converter sections.

Inverting Converter: Output Capacitor Selection

The inverting converter requires much smaller output capacitors than those of the boost, flyback and SEPIC converters for similar output ripples. This is due to the fact that, in the inverting converter, the inductor L2 is in series with the output, and the ripple current flowing through the output capacitors are continuous. The output ripple voltage is produced by the ripple current of L2 flowing through the ESR and bulk capacitance of the output capacitor:

$$\Delta V_{OUT(P-P)} = \Delta I_{L2} \bullet \left(ESR_{COUT} + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

After specifying the maximum output ripple, the user can select the output capacitors according to the preceding equation.

The ESR can be minimized by using high quality X5R or X7R dielectric ceramic capacitors. In many applications, ceramic capacitors are sufficient to limit the output voltage ripple.

The RMS ripple current rating of the output capacitor needs to be greater than:

$$I_{RMS(COUT)} > 0.3 \bullet \Delta I_{L2}$$

Inverting Converter: Selecting the DC Coupling Capacitor

The DC voltage rating of the DC coupling capacitor (C_{DC}, as shown in Figure 10) should be larger than the maximum input voltage minus the output voltage (negative voltage):

$$V_{CDC} > V_{IN(MAX)} - V_{OUT}$$

C_{DC} has nearly a rectangular current waveform. During the switch off-time, the current through C_{DC} is I_{IN}, while approximately $-I_O$ flows during the on-time. The RMS rating of the coupling capacitor is determined by the following equation:

$$I_{RMS(CDC)} > I_{O(MAX)} \bullet \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

A low ESR and ESL, X5R or X7R ceramic capacitor works well for C_{DC}.

Board Layout

The high speed operation of the LT3758 demands careful attention to board layout and component placement. The Exposed Pad of the package is the only GND terminal of the IC, and is important for thermal management of the IC. Therefore, it is crucial to achieve a good electrical and thermal contact between the Exposed Pad and the ground plane of the board. For the LT3758 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible.

To prevent radiation and high frequency resonance problems, proper layout of the components connected to the IC is essential, especially the power paths with higher di/dt. The following high di/dt loops of different topologies should be kept as tight as possible to reduce inductive ringing:

- In boost configuration, the high di/dt loop contains the output capacitor, the sensing resistor, the power MOSFET and the Schottky diode.
- In flyback configuration, the high di/dt primary loop contains the input capacitor, the primary winding, the power MOSFET and the sensing resistor. The high di/dt secondary loop contains the output capacitor, the secondary winding and the output diode.
- In SEPIC configuration, the high di/dt loop contains the power MOSFET, sense resistor, output capacitor, Schottky diode and the coupling capacitor.
- In inverting configuration, the high di/dt loop contains power MOSFET, sense resistor, Schottky diode and the coupling capacitor.

APPLICATIONS INFORMATION

Check the stress on the power MOSFET by measuring its drain-to-source voltage directly across the device terminals (reference the ground of a single scope probe directly to the source pad on the PC board). Beware of inductive ringing, which can exceed the maximum specified voltage rating of the MOSFET. If this ringing cannot be avoided, and exceeds the maximum rating of the device, either choose a higher voltage device or specify an avalanche-rated power MOSFET.

The small-signal components should be placed away from high frequency switching nodes. For optimum load regulation and true remote sensing, the top of the output voltage sensing resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LT3758 in order to keep the high impedance FBX node short.

Figure 11 shows the suggested layout of the 10V to 40V input, 48V output boost converter in the Typical Applications section.

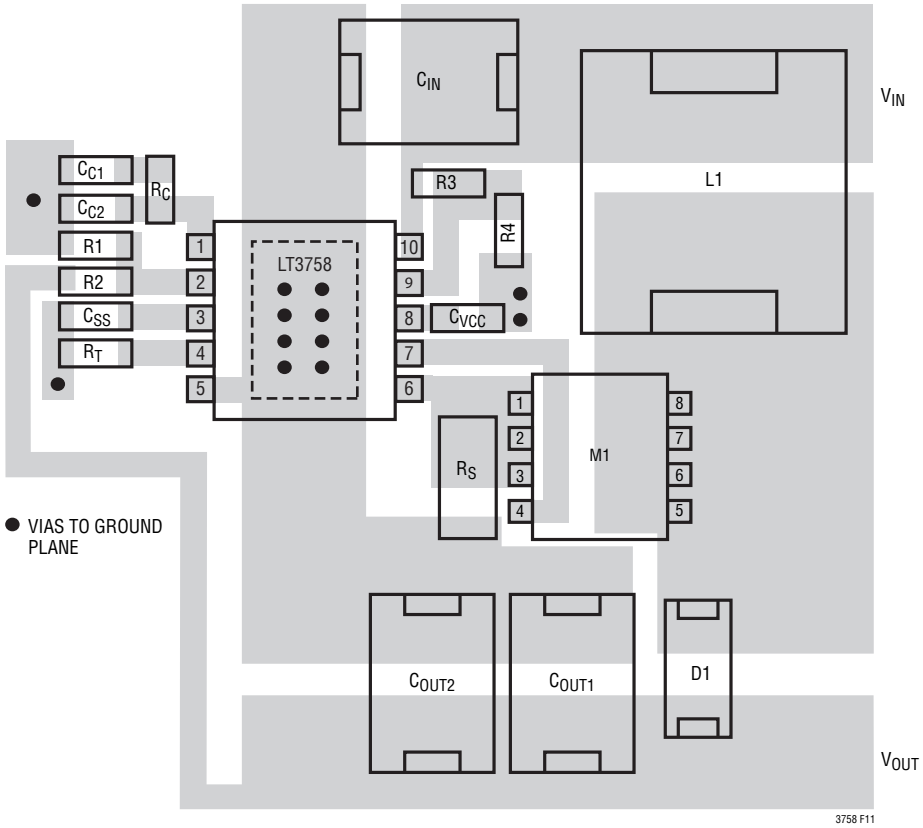


Figure 11. Suggested Layout of the 10V to 40V Input, 48V Output Boost Converter in the Typical Applications Section

APPLICATIONS INFORMATION

Recommended Component Manufacturers

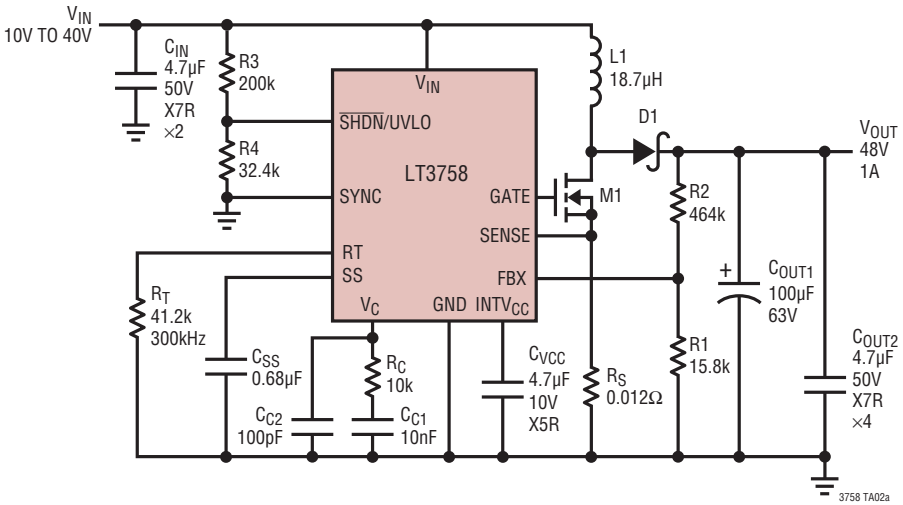
Some of the recommended component manufacturers are listed in Table 2.

Table 2. Recommended Component Manufacturers

VENDOR	COMPONENTS	WEB ADDRESS
AVX	Capacitors	avx.com
BH Electronics	Inductors, Transformers	bhelectronics.com
Coilcraft	Inductors	coilcraft.com
Cooper Bussmann	Inductors	bussmann.com
Diodes, Inc	Diodes	diodes.com
Fairchild	MOSFETs	fairchildsemi.com
General Semiconductor	Diodes	generalsemiconductor.com
International Rectifier	MOSFETs, Diodes	irf.com
IRC	Sense Resistors	irctt.com
Kemet	Tantalum Capacitors	kemet.com
Magnetics Inc	Toroid Cores	mag-inc.com
Microsemi	Diodes	microsemi.com
Murata-Erie	Inductors, Capacitors	murata.co.jp
Nichicon	Capacitors	nichicon.com
On Semiconductor	Diodes	onsemi.com
Panasonic	Capacitors	panasonic.com
Pulse	Inductors	pulseeng.com
Sanyo	Capacitors	sanyo.co.jp
Sumida	Inductors	sumida.com
Taiyo Yuden	Capacitors	t-yuden.com
TDK	Capacitors, Inductors	component.tdk.com
Thermalloy	Heat Sinks	aavidthermalloy.com
Tokin	Capacitors	nec-tokinamerica.com
Toko	Inductors	tokoam.com
United Chemi-Con	Capacitors	chemi-com.com
Vishay/Dale	Resistors	vishay.com
Vishay/Siliconix	MOSFETs	vishay.com
Würth Elektronik	Inductors	we-online.com
Vishay/Sprague	Capacitors	vishay.com
Zetex	Small-Signal Discretes	zetex.com

TYPICAL APPLICATIONS

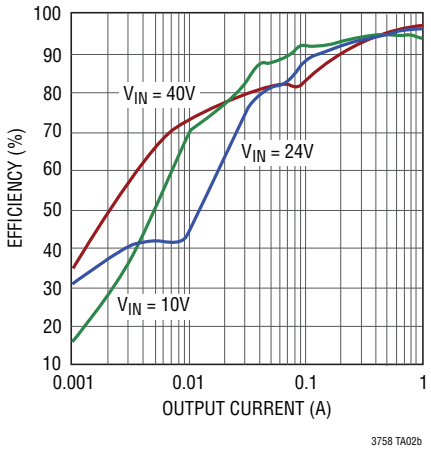
10V to 40V Input, 48V Output Boost Converter



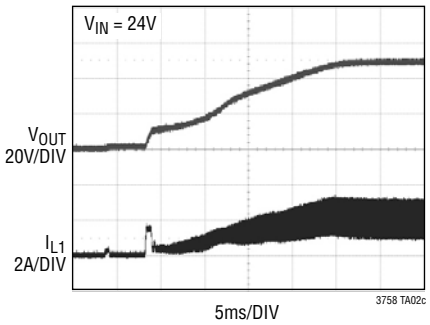
CIN, COUT2: MURATA GRM32ER71H475KA88L
COUT1: PANASONIC ECG EEV-TG1J101UP

D1: VISHAY SILICONIX 30BQ060
L1: PULSE PB2020.223
M1: VISHAY SILICONIX SI7460DP

Efficiency vs Output Current

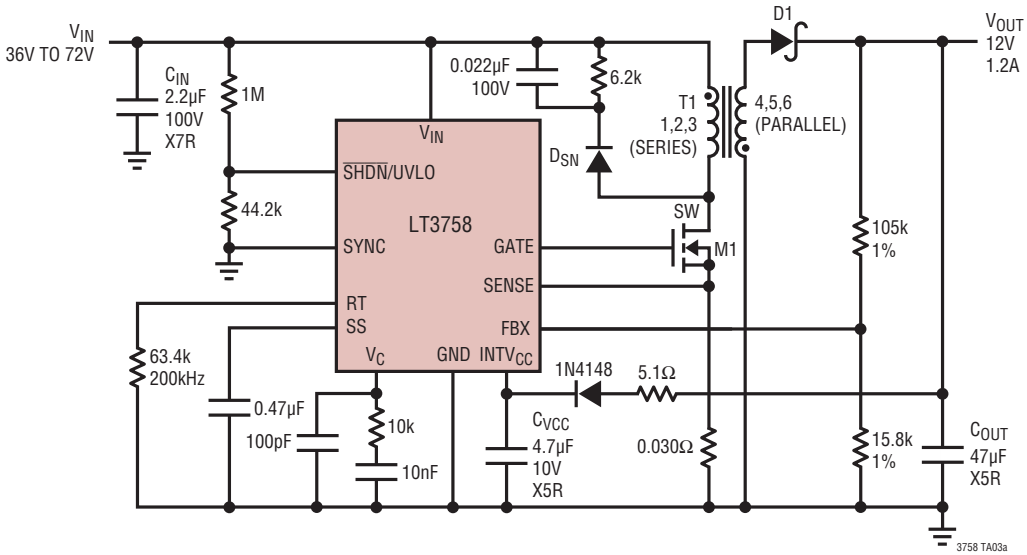


Start-Up Waveforms



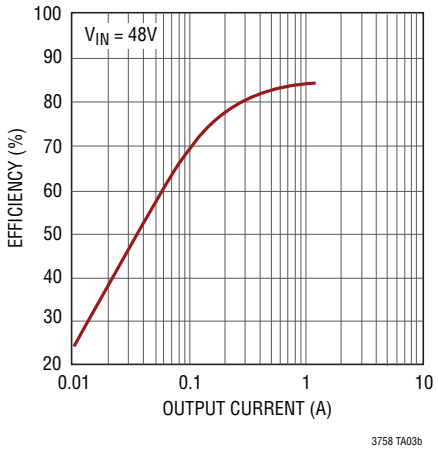
TYPICAL APPLICATIONS

12V Output Nonisolated Flyback Power Supply

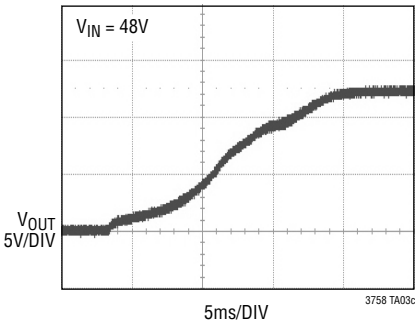


CIN: MURATA GRM32ER72A225KA35L
T1: COILTRONICS VP2-0066
M1: VISHAY SILICONIX SI4848DY
D1: ON SEMICONDUCTOR MBRS360T3G
DSN: VISHAY SILICONIX ES1D
COUT: MURATA GRM32ER61C476ME15L

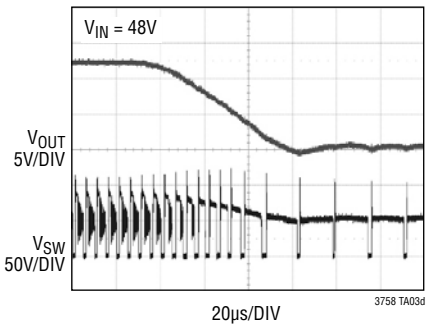
Efficiency vs Output Current



Start-Up Waveform

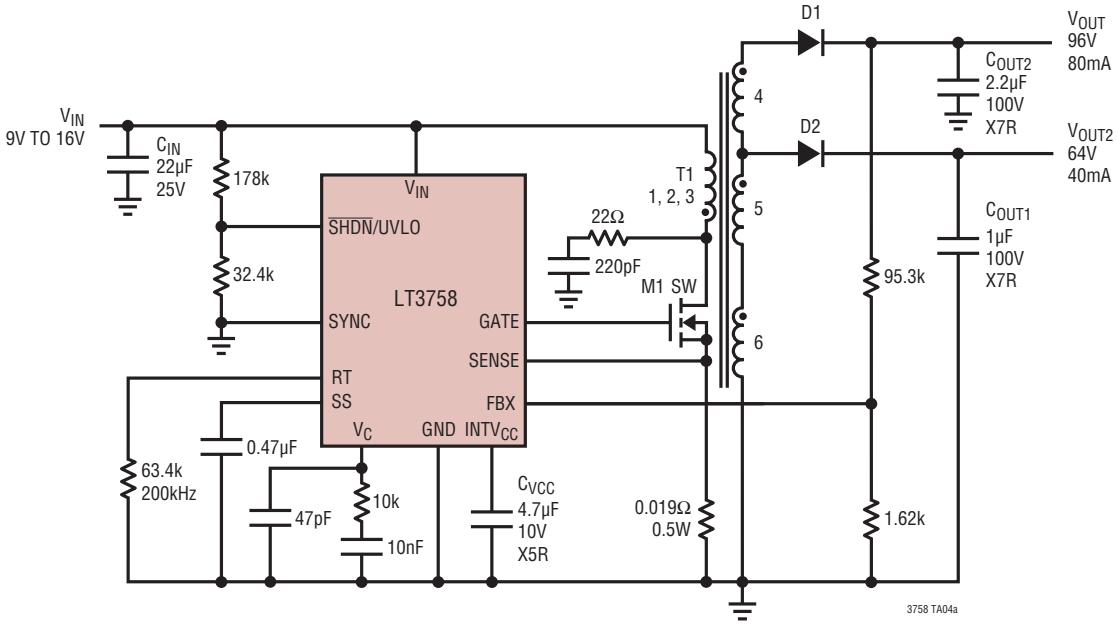


Frequency Foldback Waveforms When Output Short-Circuit



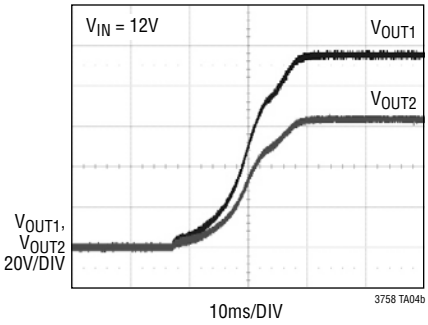
TYPICAL APPLICATIONS

VFD (Vacuum Fluorescent Display) Flyback Power Supply



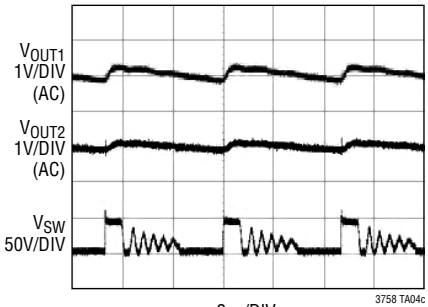
C_{IN}: MURATA GRM32ER61E226KE15L
C_{OUT1}: MURATA GRM31CR72A105K01L
C_{OUT2}: MURATA GRM32ER72A225KA35L
D1: VISHAY SILICONIX ES1D
D2: VISHAY SILICONIX ES1C
M1: VISHAY SILICONIX Si4100DY
T1: COILTRONICS VP1-0102
(*PRIMARY = 3 WINDINGS IN PARALLEL)

Start-Up Waveforms



10ms/DIV

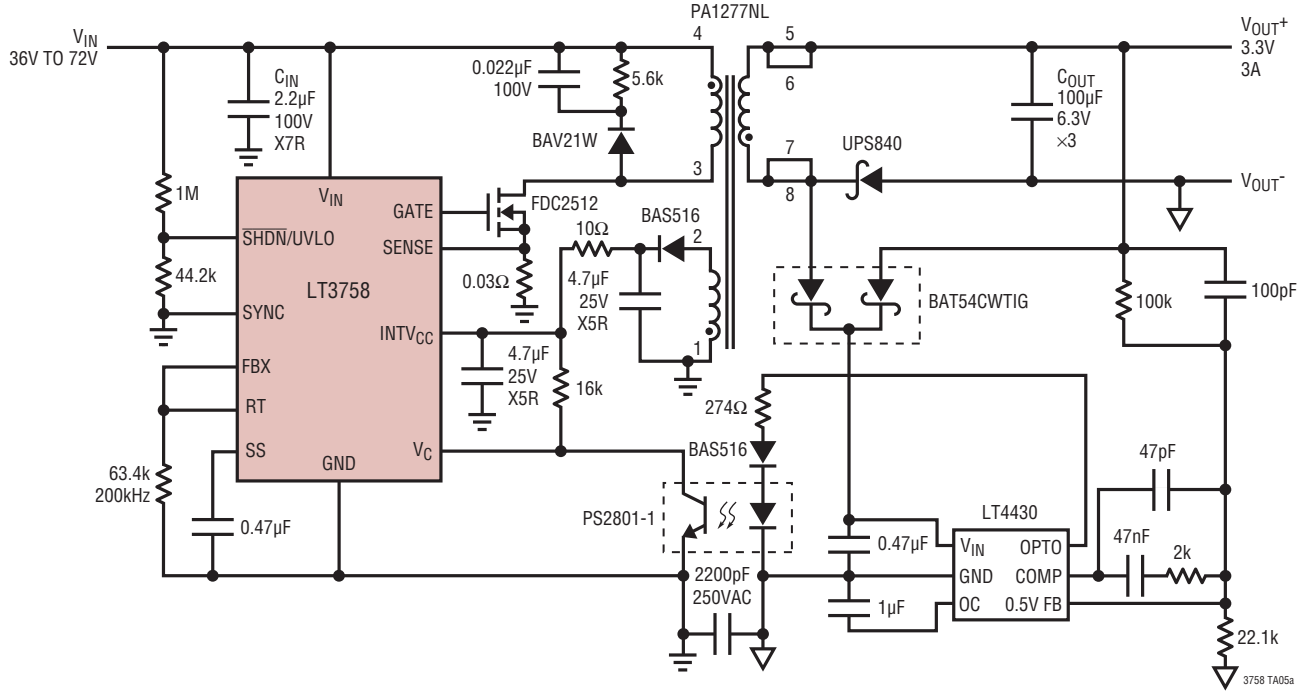
Switching Waveforms



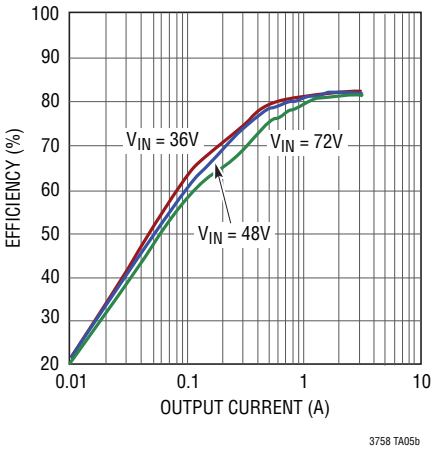
2µs/DIV

TYPICAL APPLICATIONS

36V to 72V Input, 3.3V Output Isolated Telecom Power Supply

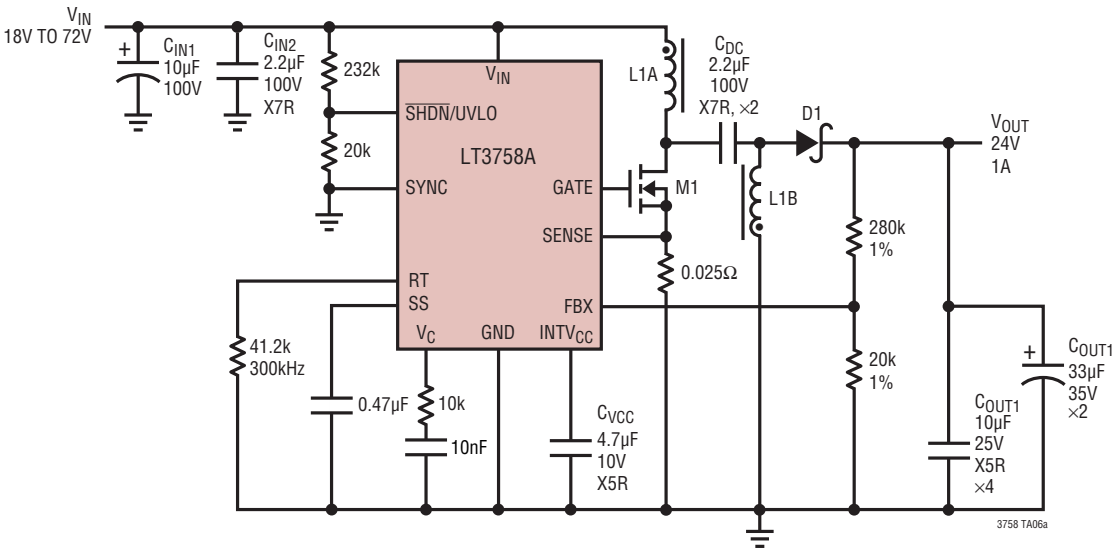


Efficiency vs Output Current



TYPICAL APPLICATIONS

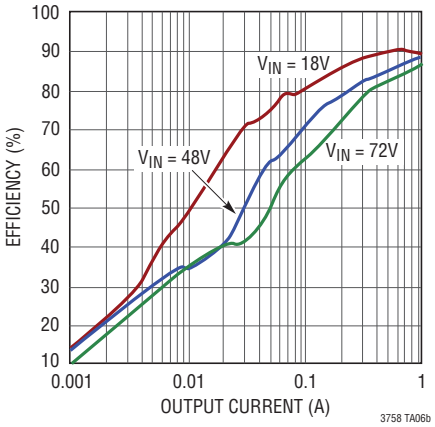
18V to 72V Input, 24V Output SEPIC Converter



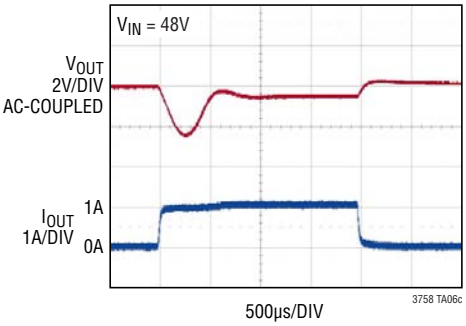
C_{IN1}: PANASONIC EEE2AA100UP
C_{IN2}, C_{DC}: TAIYO YUDEN HMK325B7225KN-T
C_{OUT1}: MURATA GRM31CR61E106KA12L
C_{OUT2}: KEMET T495X336K035AS

L1A, L1B: COILTRONICS DRQ127-470
M1: FAIRCHILD SEMICONDUCTOR FDMS2572
D1: ON SEMICONDUCTOR MBRS3100T3G

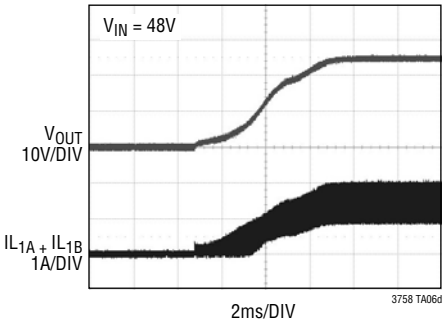
Efficiency vs Output Current



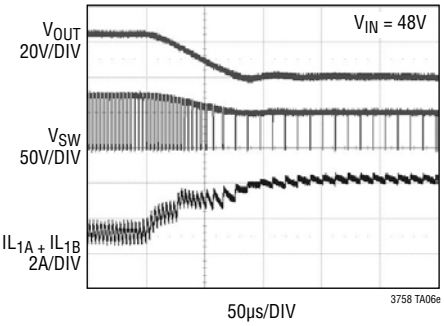
Load Step Waveform



Start-Up Waveform

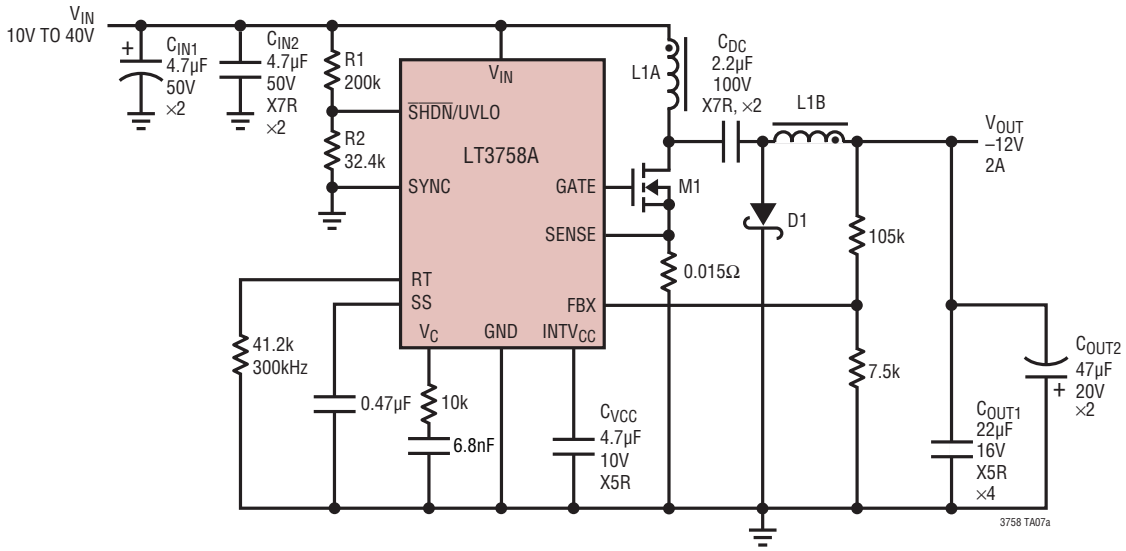


Frequency Foldback Waveforms When Output Short-Circuit



TYPICAL APPLICATIONS

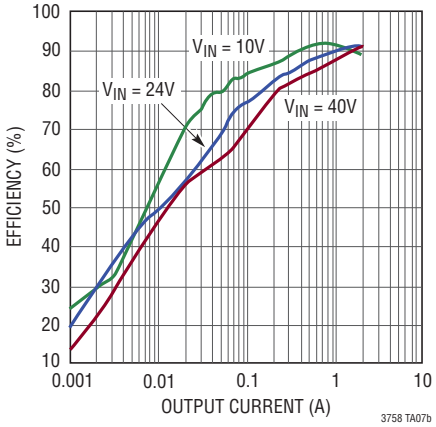
10V to 40V Input, –12V Output Inverting Converter



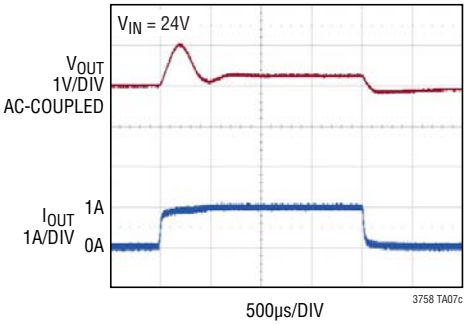
C_{IN1}: KEMET T495X475K050AS
C_{IN2}, C_{DC}: MURATA GRM32ER71H475KA88L
C_{OUT1}: MURATA GRM32ER61C226KE20
C_{OUT2}: KEMET T495X476K020AS

D1: VISHAY SILICONIX 30BQ060
L1A, L1B: COILTRONICS DRQ127-150
M1: VISHAY SILICONIX SI7850DP

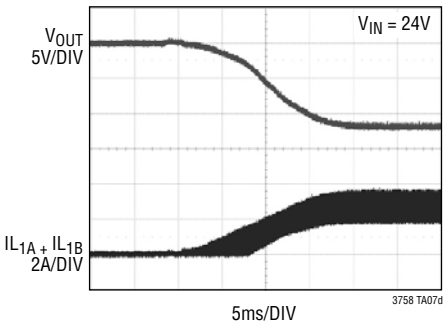
Efficiency vs Output Current



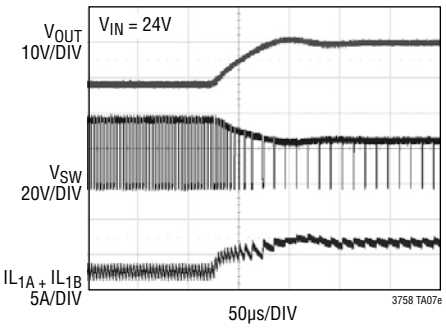
Load Step Waveforms



Start-Up Waveforms

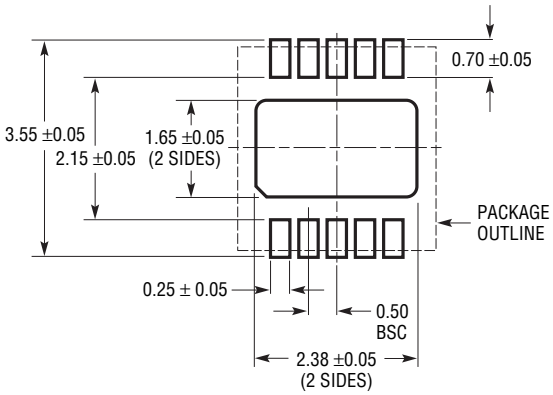


Frequency Foldback Waveforms When Output Short-Circuit

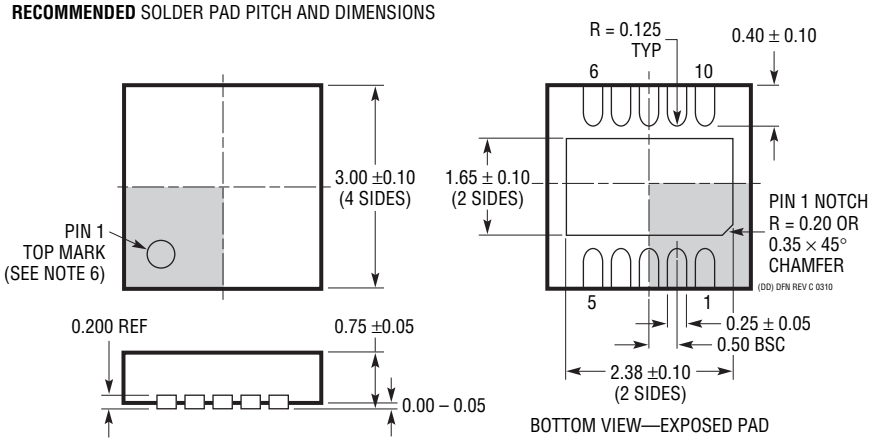


PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

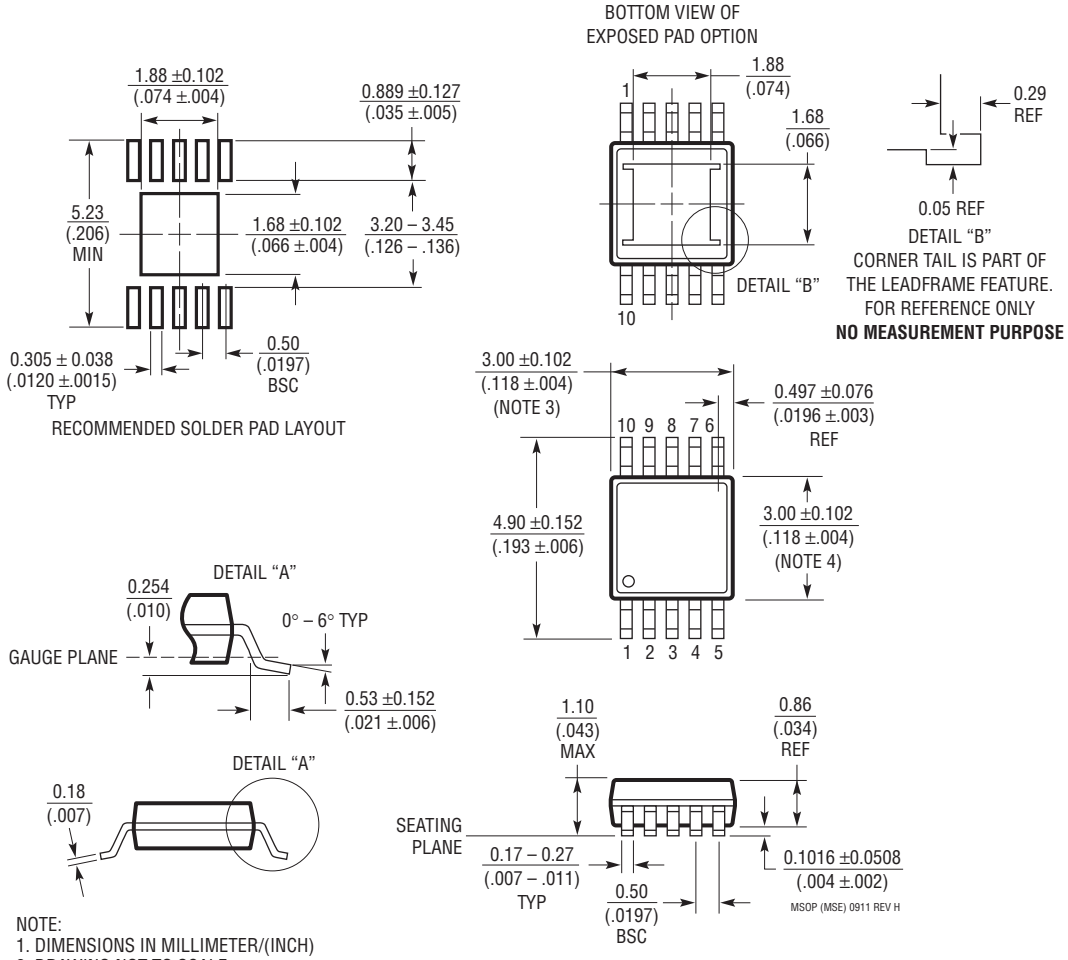


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev H)



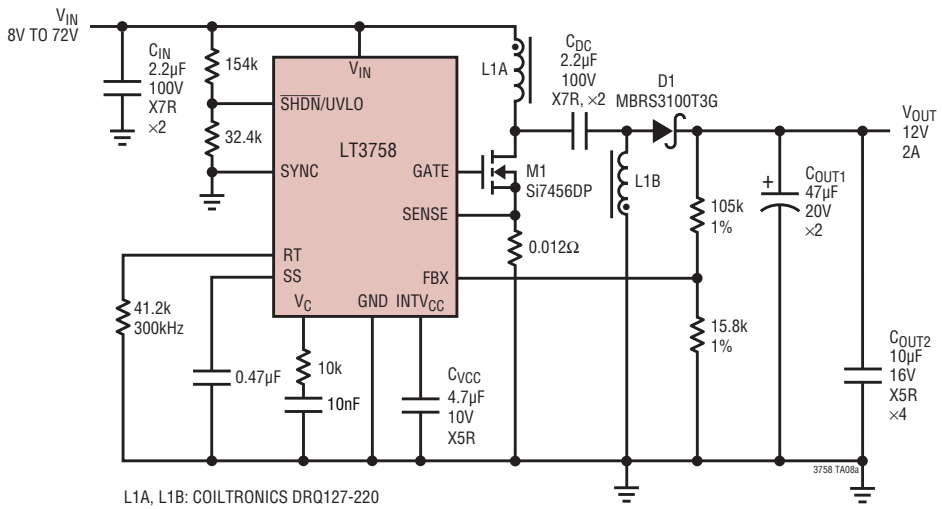
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/10	Deleted Bullet from Features and Last Line of Description	1
		Updated All Sections to Include H-Grade and Military Grade	2 to 7
		Deleted Vendor Telephone Information from Table 2 in Applications Information Section	26
		Revised TA04 and TA04c in Typical Applications	29
		Replaced Related Parts List	36
B	5/10	Revised last sentence of SYNC Pin description	8
		Updated Block Diagram	9
		Revised value in last sentence of Programming Turn-on and Turn-off Thresholds in the SHDN/UVLO Pin Section	10
		Revised penultimate sentence of Operating Frequency and Synchronization section	13
C	5/11	Revised MP-grade temperature range in Absolute Maximum Ratings and Order Information	2
		Revised Note 2	4
		Revised formula in Applications Information	19
D	07/12	Added LT3758A version	Throughout
		Updated Block Diagram	9
		Updated Programming the Output Voltage section	13
		Updated Loop Compensation section	14
		Updated the schematic and Load Step Waveforms in the Typical Applications section	31, 32

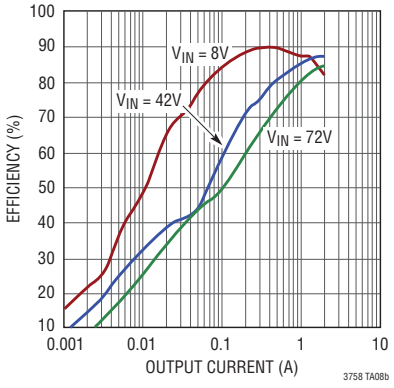
TYPICAL APPLICATIONS

8V to 72V Input, 12V Output SEPIC Converter



L1A, L1B: COILTRONICS DRQ127-220

Efficiency vs Output Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3757A	Boost, Flyback, SEPIC and Inverting Controller	2.9V ≤ V_{IN} ≤ 40V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3759	Boost, SEPIC and Inverting Controller	1.6V ≤ V_{IN} ≤ 42V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, MSOP-12E Packages
LT3957A	Boost, Flyback, SEPIC and Inverting Controller with 5A, 40V Switch	3V ≤ V_{IN} ≤ 40V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN Package
LT3958	Boost, Flyback, SEPIC and Inverting Controller with 3.3A, 84V Switch	5V ≤ V_{IN} ≤ 80V, Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, 5mm × 6mm QFN Package
LT3573/LT3574/ LT3575	40V Isolated Flyback Converters	Monolithic No-Opto Flybacks with Integrated 1.25A/0.65A/2.5A Switch
LT3511/LT3512	100V Isolated Flyback Converters	Monolithic No-Opto Flybacks with Integrated 240mA/420mA Switch
LT3798	Offline Isolated No Opto-Coupler Flyback Controller with Active PFC	V_{IN} and V_{OUT} Limited Only by External Components, MSOP-16 Package
LT3799/LT3799-1	Offline Isolated Flyback LED Controllers with Active PFC	V_{IN} and V_{OUT} Limited Only by External Components, MSOP-16 Package