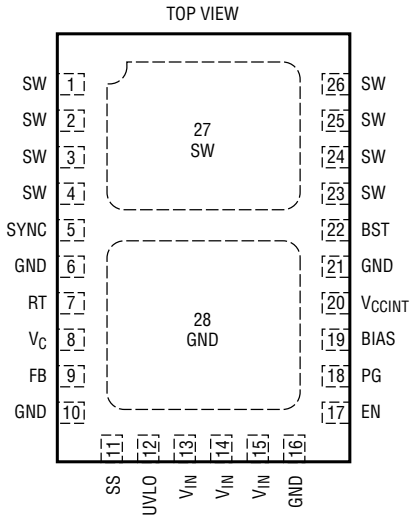
ABSOLUTE MAXIMUM RATINGS

(Note 1)

EN, UVLO, V_{IN} Voltage (Note 2) 60V
BST Voltage 55V
BST Voltage Above SW Voltage 30V
BIAS, PG Voltage 30V
FB, RT, SS, SYNC, V_C, V_{CCINT} Voltage 6V
Operating Junction Temperature Range (Notes 3 and 4)
LT3690E .....–40°C to 125°C
LT3690I .....–40°C to 125°C
LT3690H .....–40°C to 150°C
LT3690MP .....–55°C to 150°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UFE PACKAGE
26-LEAD (4mm × 6mm) PLASTIC QFN

θ_{JA} = 40°C/W, θ_{JC} = 2.7°C/W
EXPOSED PAD (PIN 27) IS SW, MUST BE SOLDERED TO PCB
EXPOSED PAD (PIN 28) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3690EUFE#PBF	LT3690EUFE#TRPBF	3690	26-Lead (4mm × 6mm) Plastic QFN	–40°C to 125°C
LT3690IUFE#PBF	LT3690IUFE#TRPBF	3690	26-Lead (4mm × 6mm) Plastic QFN	–40°C to 125°C
LT3690HUFE#PBF	LT3690HUFE#TRPBF	3690	26-Lead (4mm × 6mm) Plastic QFN	–40°C to 150°C
LT3690MPUFE#PBF	LT3690MPUFE#TRPBF	3690	26-Lead (4mm × 6mm) Plastic QFN	–55°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V unless otherwise noted (Notes 3, 7).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Fixed Undervoltage Lockout		●		3.0	3.9	V
V_{IN} Overvoltage Lockout OVLO	V_{IN} Rising	●	36	38.2	40	V
Quiescent Current from V_{IN}	V_{EN} = 0.2V			0.1	1	µA
	V_{BIAS} = 3V, V_{FB} = 0.85V Not Switching	●		35	60	µA
	V_{BIAS} = 0V, V_{FB} = 0.85V Not Switching			110	150	µA
Quiescent Current from BIAS Pin	V_{EN} = 0.2V			0.1	1	µA
	V_{BIAS} = 3V, V_{FB} = 0.85V Not Switching	●		70	110	µA
	V_{BIAS} = 0V, V_{FB} = 0.85V Not Switching			–3	–10	µA
Boost Schottky Diode Drop (V_{BIAS} – V_{BST})	I_{BIAS} = 200mA			820	950	mV
BST Voltage (Note 5) (V_{BST} – V_{SW})	Minimum BOOST Voltage Above SW, I_{SW} = 4A	●		1.6	2.3	V
BST Pin Current	I_{SW} = 4A			70	140	mA
BST Pin Leakage	V_{SW} = 12V, V_{BIAS} = 0V			0.1	6	µA
HS Switch Drop (V_{IN} – V_{SW})	I_{SW} = 4A			370	600	mV
HS Switch Current Limit (Note 6)			5.5	6.6	8	A
HS Switch Leakage Current	V_{SW} = 0V			0.1	2	µA
HS Minimum Switch Off-Time		●			210	ns
LS Switch Off Voltage Drop	I_{SW} = 4A			700	850	mV
LS Switch On-Resistance	I_{SW} = 4A, V_{CCINT} = 5V			30	60	mΩ
LS Switch On-Resistance	I_{SW} = 4A, V_{CCINT} = 4V			30	90	mΩ
LS Switch Current Threshold			4	5	6.5	A
LS Switch Leakage Current	V_{EN} = 0V, V_{SW} = 12V, V_{BST} = 12V			0.1	10	µA
	V_{EN} = 0V, V_{SW} = 12V, V_{BST} = 12V, T_J = 125°C				95	µA
V_{CCINT} Pin Output Voltage	I_{VCCINT} = 0µA		4.3	4.9	5.3	V
V_{CCINT} Pin Output Voltage	I_{VCCINT} = –10mA		4.2	4.8	5.3	V
EN Input Current	V_{EN} = 12V			8	15	µA
	V_{EN} = 2.5V			2.5	6	µA
EN Input Voltage, Enable			1.5			V
EN Input Voltage, Disable					0.4	V
UVLO Threshold Voltage			1.1		1.33	V
UVLO Pin Current	V_{UVLO} = 1.33V			–2.0	–3.8	µA
UVLO Pin Current	V_{UVLO} = 1.1V			0.1	1	µA
UVLO Pin Current Hysteresis	I_{UVLO} at 1.1V – I_{UVLO} at 1.33V		1.2	2	2.8	µA
Pull-Up Current at SS Pin	V_{SS} = 0.8V		–1.2	–2	–2.8	µA
Tracking Offset (V_{SS} – V_{FB})	V_{SS} = 0.4V		–4	7	15	mV
SYNC Input Voltage High			0.8			V
SYNC Input Voltage Low					0.4	V
SYNC Input Resistance to GND			150	300	600	kΩ
SYNC Input Frequency			0.17		1.5	MHz
Feedback Reference Voltage		 ●	792 786	800 800	808 814	mV mV
FB Pin Bias Current Flows Out of Pin	V_{FB} = 800mV	●		–8	–40	nA
FB Voltage Line Regulation	3.6V < V_{IN} < 36V			0.001	0.01	%/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V unless otherwise noted (Notes 3, 7).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PG Threshold as Percentage of V_{FB}	V_{FB} Rising		88	90	92	%
PG Hysteresis				12		mV
PG Sink Current	V_{PG} = 0.3V	●	100	500		µA
PG Leakage	V_{PG} = 5V			0.1	1	µA
Error Amplifier Transconductance				400		µA/V
Error Amp Voltage Gain				60		dB
V_C Source Current				–50		µA
V_C Sink Current				50		µA
V_C Pin to Switch Current Gain Transconductance				4.6		A/V
V_C Switching Threshold				0.7		V
V_C Clamp Voltage				2.0		V
Programmable Switching Frequency	R_T = 10kΩ		1.32	1.5	1.68	MHz
	R_T = 24.9kΩ		660	750	840	kHz
	R_T = 180kΩ		122	138	154	kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Absolute maximum voltage at the EN, UVLO and V_{IN} pins is 36V for continuous operation. For non-repetitive 1 second transients while T_J < 125°C, the absolute maximum voltage is 60V.

Note 3: The LT3690E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3690I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3690H is guaranteed over the full –40°C to 150°C operating junction temperature range. The LT3690MP is guaranteed over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetime. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

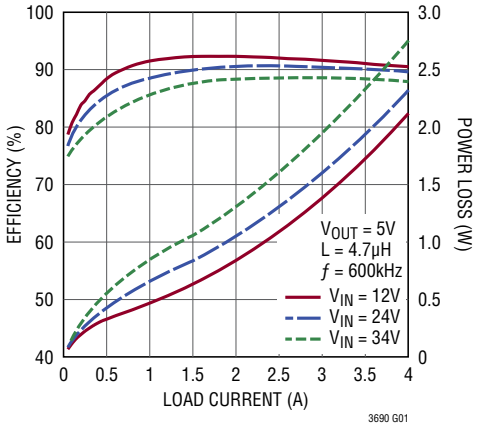
Note 5: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the switch.

Note 6: Current limit guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles. Current limit reduced when feedback voltage is below the reference voltage.

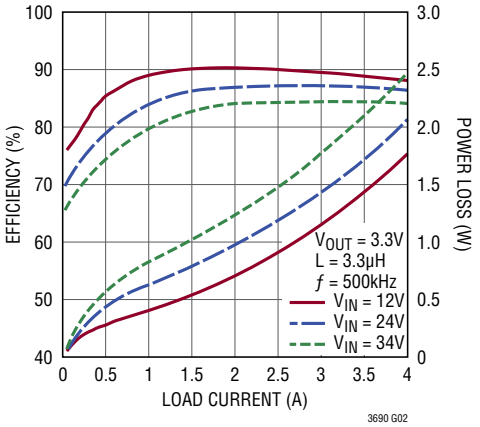
Note 7: The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. Negative magnitudes are shown as maximum.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

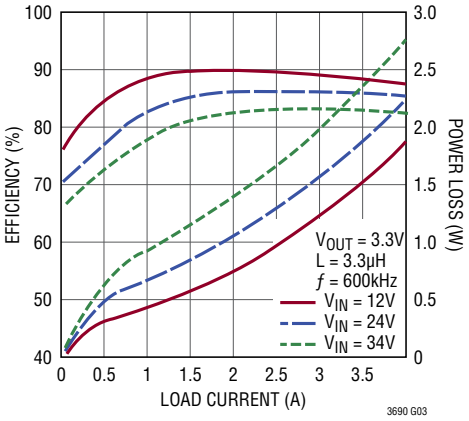
Efficiency and Power Loss



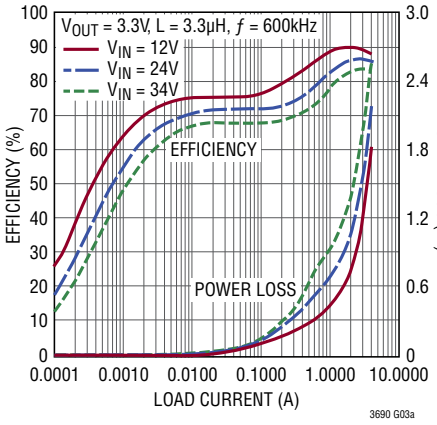
Efficiency and Power Loss



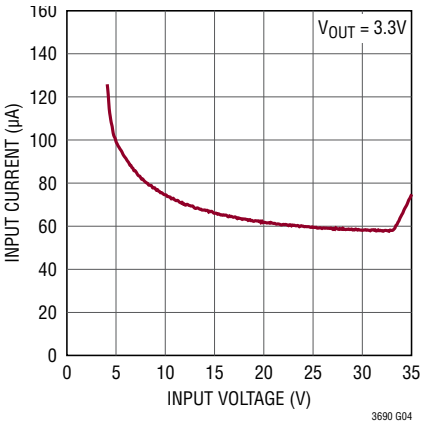
Efficiency and Power Loss



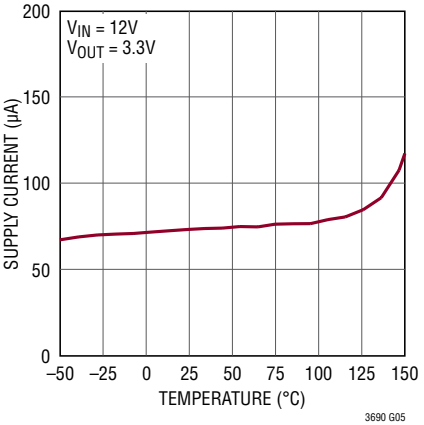
Efficiency and Power Loss



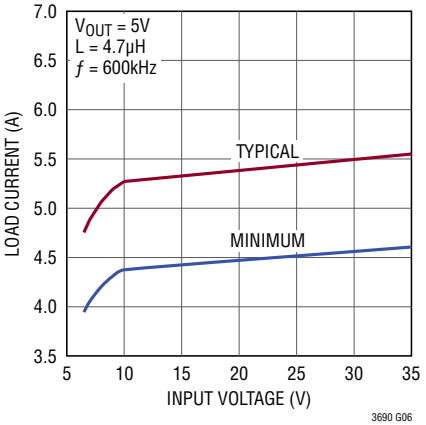
No Load Supply Current vs V_{IN}



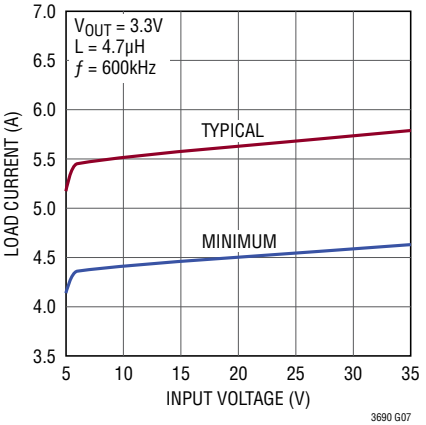
No Load Supply Current vs Temperature



Maximum Load Current vs V_{IN}

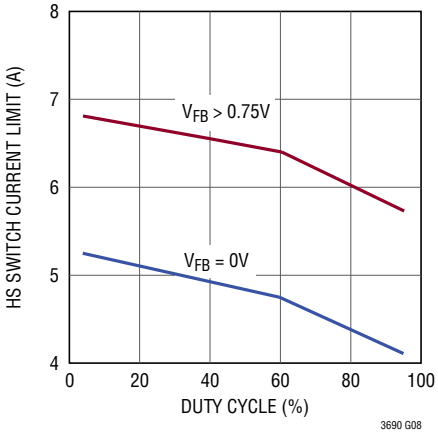


Maximum Load Current vs V_{IN}

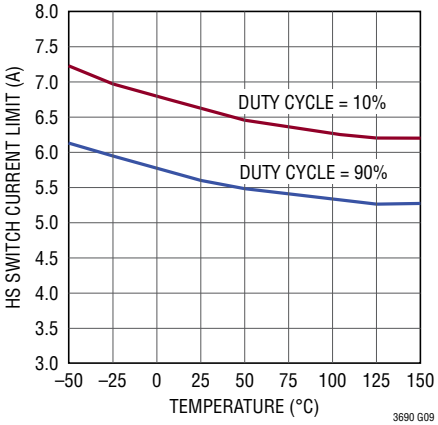


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

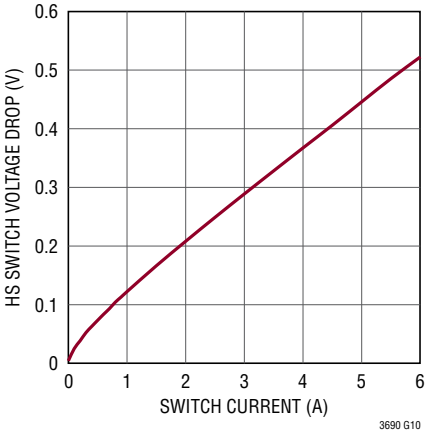
Switch Current Limit vs Duty Cycle



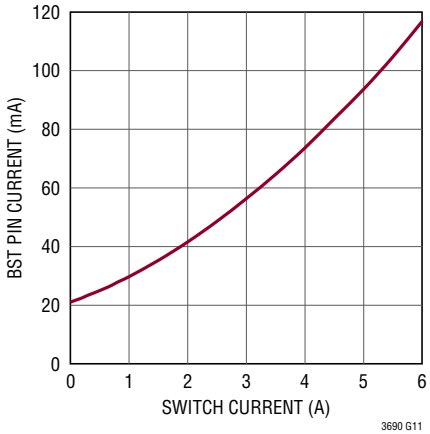
Switch Current Limit vs Temperature



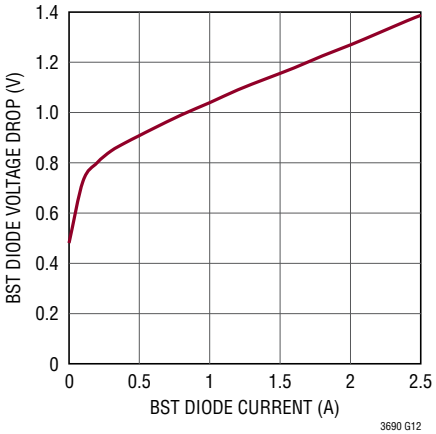
Switch Voltage Drop vs I_{SW}



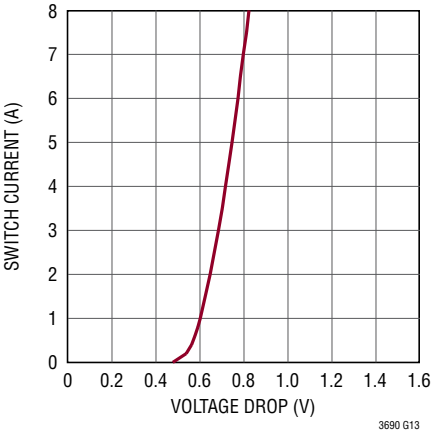
BST Pin Current vs I_{SW}



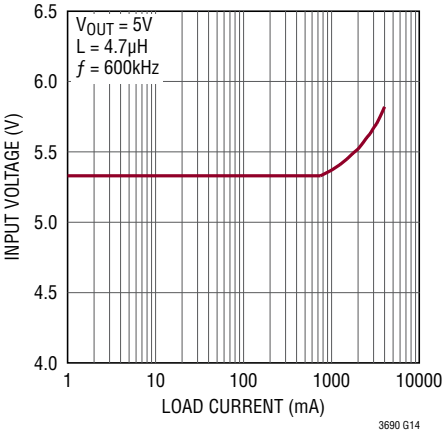
Boost Diode Drop ($V_{BIAS} – V_{BST}$) vs I_{BST}



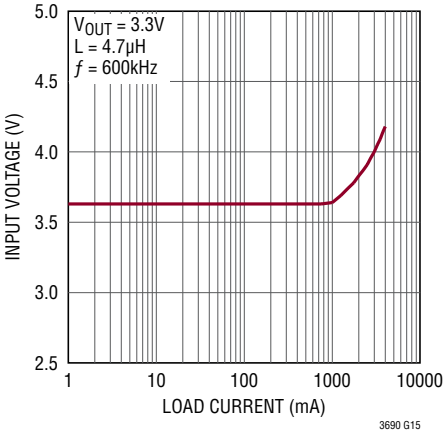
Catch Diode Voltage Drop ($V_{GND} – V_{SW}$) vs I_{SW}



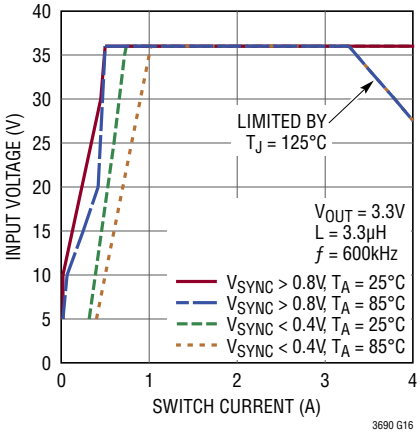
Minimum Input Voltage vs Load Current



Minimum Input Voltage vs Load Current

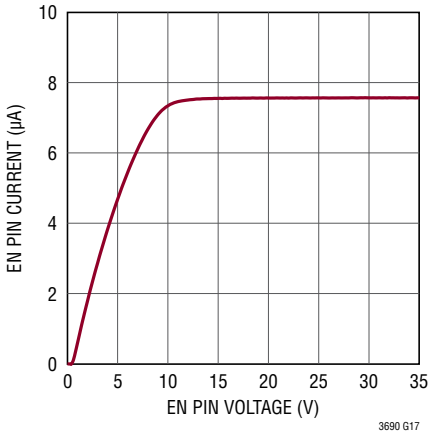


Maximum V_{IN} for Fixed Frequency

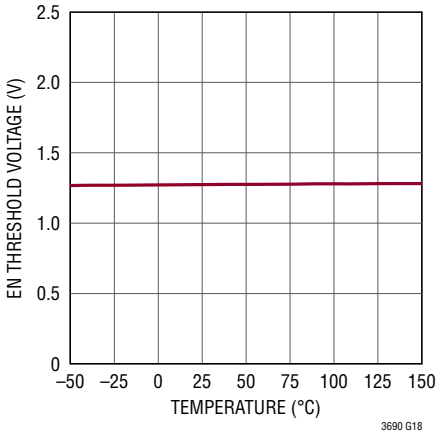


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

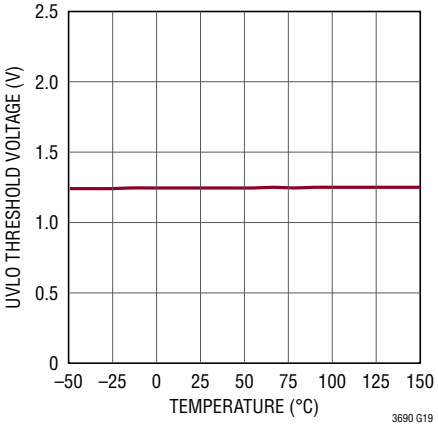
EN Pin Current vs V_{EN}



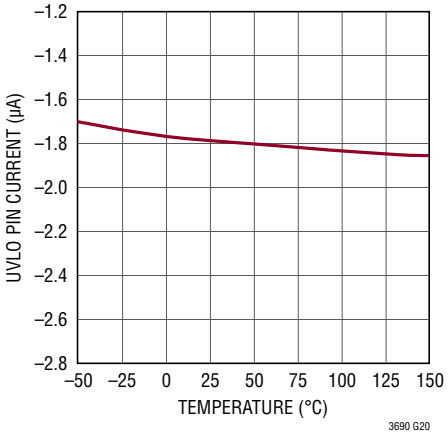
EN Threshold Voltage vs Temperature



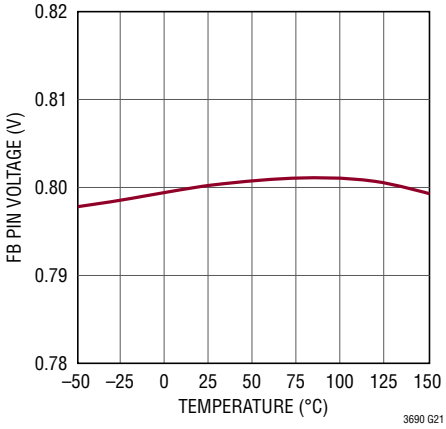
UVLO Threshold Voltage vs Temperature



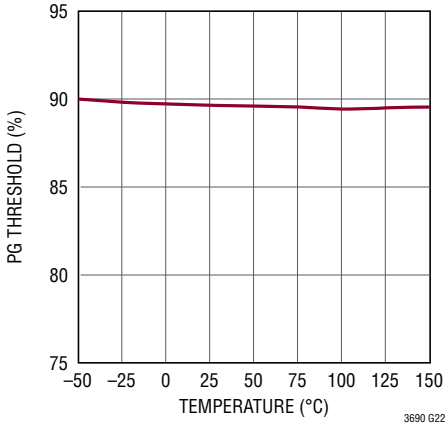
UVLO Pin Current vs Temperature (V_{UVLO} = 1.33V)



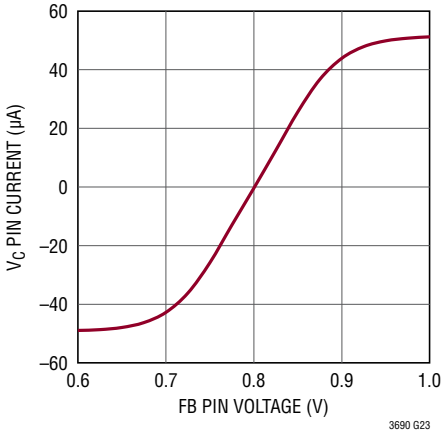
Feedback Voltage vs Temperature



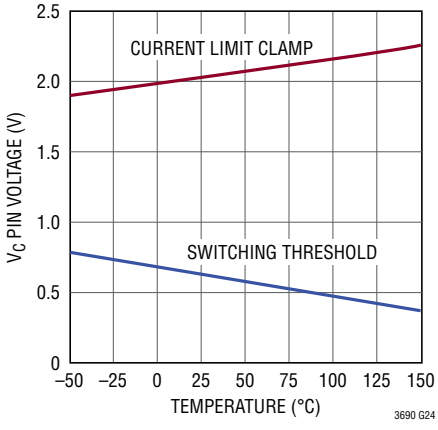
Power Good Threshold vs Temperature



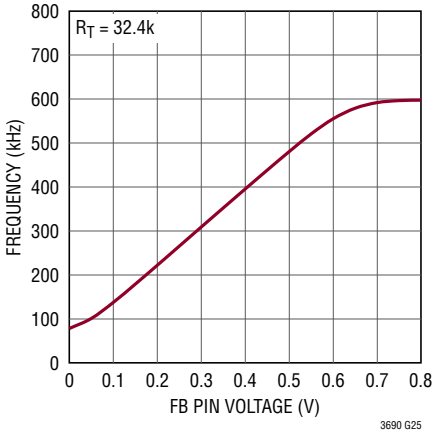
Error Amp Output Current vs V_{FB}



V_C Voltages vs Temperature

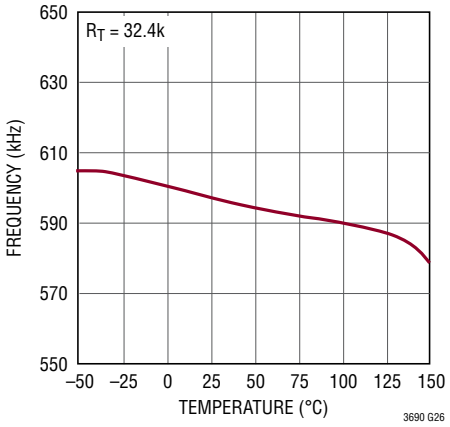


Frequency Foldback vs V_{FB}

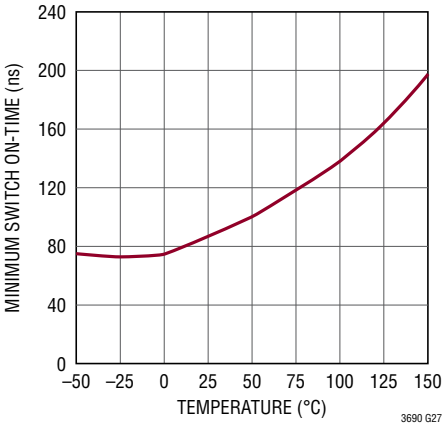


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

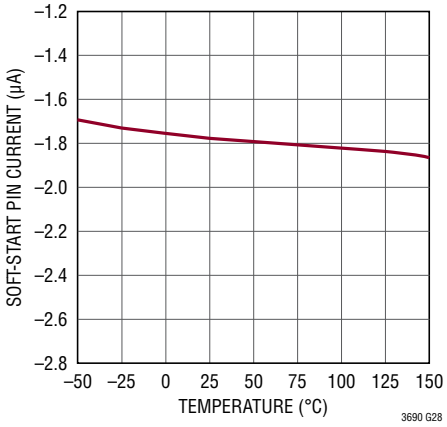
Switching Frequency vs Temperature



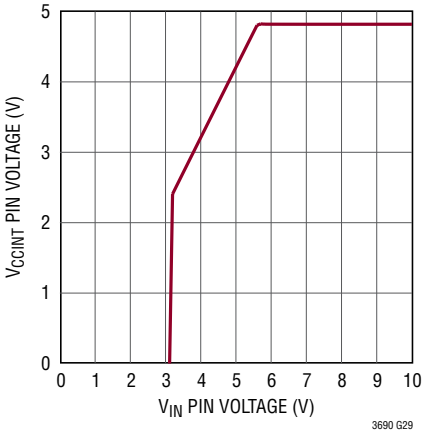
Minimum Switch On-Time vs Temperature



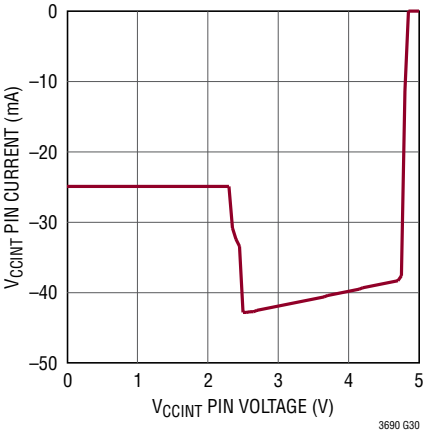
Soft-Start Pin Current vs Temperature



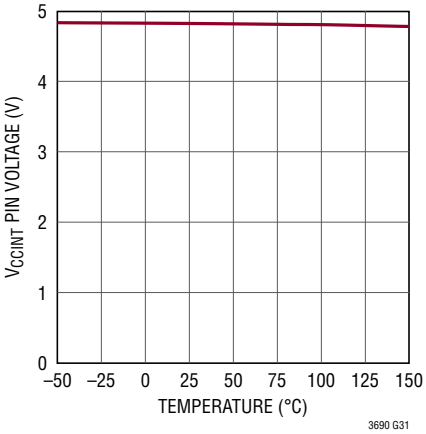
V_{CCINT} vs V_{IN}



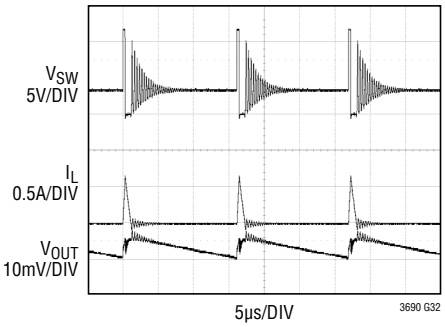
V_{VCCINT} Current Limit



V_{CCINT} Pin Voltage

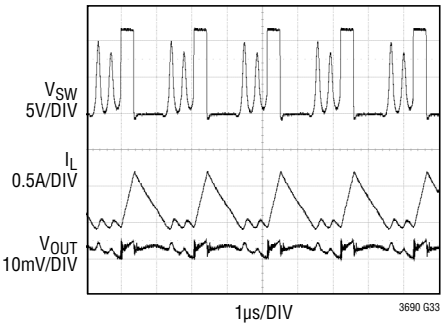


Switching Waveforms, Burst Mode Operation



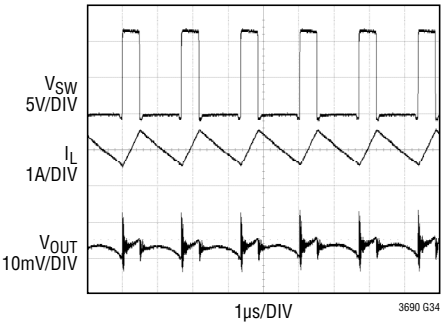
V_{IN} = 12V, I_{LOAD} = 20mA
FRONT PAGE APPLICATION

Switching Waveforms, Transition from Burst Mode Operation to Full Frequency



V_{IN} = 12V, I_{LOAD} = 200mA
FRONT PAGE APPLICATION

Switching Waveforms, Full Frequency Continuous Operation



V_{IN} = 12V, I_{LOAD} = 2A
FRONT PAGE APPLICATION

PIN FUNCTIONS

SW (Pins 1-4, 23-26, Exposed Pad Pin 27): The SW pin is the emitter output of the internal highside NPN power switch (HS) and the drain output of the internal lowside power N-channel switch (LS). Connect this pin to the inductor and boost capacitor. This pin is driven up to the V_{IN} voltage by the HS switch during the on-time of the PWM duty cycle. The inductor current drives the SW pin negative during the off-time. The on-resistance of the LS switch and the internal Schottky diode fixes the negative voltage.

The exposed pad is connected internally with SW pins 1-4, 23-26 and should be soldered to a large copper area to reduce thermal resistance.

SYNC (Pin 5): The SYNC pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 20% and 80% duty cycle. The synchronizing range is from 170kHz to 1.5MHz. See the Synchronization section in the Applications Information section for details. When not used for synchronization, the SYNC pin can be tied to ground to select low ripple Burst Mode operation or tied to the output voltage to select standard PWM mode.

RT (Pin 7): Oscillator Resistor Input. Connecting a resistor to ground (Pin 10) from this pin sets the switching frequency.

V_C (Pin 8): The V_C pin is the output of the internal error amplifier. The voltage on this pin controls the peak switch current. Tie an RC network from this pin to ground to compensate the control loop.

FB (Pin 9): The LT3690 regulates the FB pin to 0.8V. Connect the feedback resistor divider tap to this pin. The adjacent ground pin (Pin 10) is recommended for the resistor divider.

SS (Pin 11): The SS pin is used to provide a soft-start or tracking function. The internal 2µA pull-up current I_{SS} in combination with an external capacitor tied to this pin creates a voltage ramp. The output voltage tracks to this voltage. For tracking, tie a resistor divider to this pin from the tracked output. In undervoltage, overvoltage and thermal shutdown, the SS pin pulls low if the output voltage is below the power good threshold to restart the output voltage with soft-start behavior. If driving this pin from a digital output, use at least 10k in series. Leave this pin disconnected if unused.

UVLO (Pin 12): Tie a resistor divider between V_{IN}, UVLO, and GND to program an undervoltage lockout threshold. The UVLO pin has an accurate 1.25V threshold. Above the threshold, the part operates normally. Below the threshold, the part drops into a low quiescent current state. See the Undervoltage Lockout section in the Applications Information section for more details.

V_{IN} (Pins 13, 14, 15): The V_{IN} pin supplies current to the LT3690's internal regulator and to the internal power switch. This pin must be locally bypassed.

EN (Pin 17): The EN input is used to put the LT3690 in shutdown mode. Pull to GND to shut down the LT3690. Tie to 1.5V or more for normal operation.

PG (Pin 18): The PG pin is the open collector output of an internal comparator. PG remains low until the FB pin is within 10% of the final regulation voltage. The PG output is valid when V_{IN} is above 3.9V, the UVLO pin is high and EN is high.

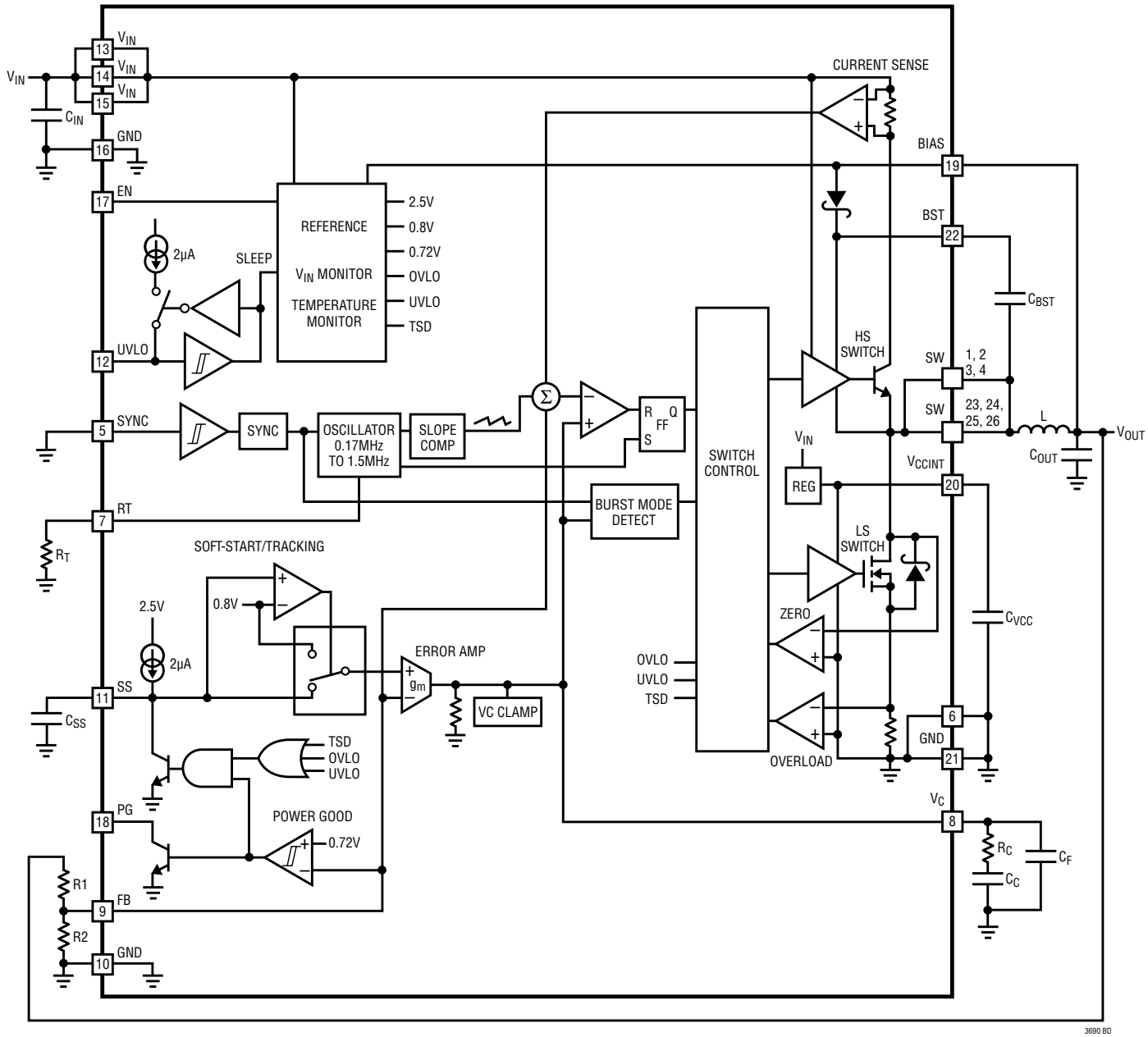
BIAS (Pin 19): This pin connects to the anode of the internal boost Schottky diode. BIAS also supplies the current to the LT3690's internal regulator. Tie this pin to the lowest available voltage source above 3V (typically V_{OUT}). This pin must be locally bypassed with 10nF.

V_{CCINT} (Pin 20): V_{CCINT} is an output of the internally generated supply voltage for the synchronous power DMOS transistor driver. An external capacitor C_{VCC} must be connected between this pin and ground (Pin 21) to buffer the internal supply voltage of the LS switch.

BST (Pin 22): This pin is used to provide, with the external boost capacitor, a drive voltage higher than the input voltage V_{IN} to the internal bipolar NPN power switch.

GND (Exposed Pad Pin 28, Pin 6, Pin 10, Pin 16, Pin 21): Ground. The exposed pad is connected internally to GND Pins 6, 10, 16 and 21, and should be soldered to a large copper area to reduce thermal resistance.

BLOCK DIAGRAM



OPERATION

The LT3690 is a constant frequency, current mode step-down regulator. An oscillator, with frequency set by R_T, enables an RS flip-flop, turning on the internal high side (HS) power switch. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the RS flip-flop and HS switch off when this current reaches a level determined by the voltage at V_C.

While the high side switch is off, the inductor current conducts through the catch diode and the turned on low side (LS) switch until either the next clock pulse of the oscillator starts the next cycle, or the inductor current becomes too low, as indicated by the zero crossing comparator. This prevents the inductor from running reverse current.

An error amplifier measures the output voltage through an external resistor divider tied to the FB pin and servos the V_C pin. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp on the V_C pin provides current limit.

The SS node acts as an auxiliary input to the error amplifier. The voltage at FB will servo to the SS voltage until SS goes above 0.8V. Soft-start is implemented by generating a voltage ramp at the SS pin using an external capacitor C_{SS} which is charged by an internal constant current. Alternatively, connecting the SS pin to a resistive divider between the voltage to be tracked and ground provides a tracking function.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 3V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency.

The EN pin is used to place the LT3690 in shutdown, disconnecting the output and reducing the input current to less than 1µA. A comparator monitors the voltage at the UVLO input. A external resistive divider connected to V_{IN} programs the wake up threshold and hysteresis. If unused, connect the input to V_{IN} or above 1.5V.

The HS switch driver operates from either the input or from the BOOST pin. An external capacitor is used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation.

The synchronously driven N-channel transistor (LS switch) in parallel with the catch diode reduces the overall solution size and improves efficiency. Internal overload comparator circuitry monitors the current through the LS switch and delays the generation of new switch pulses if this current is too high (above 5A nominal). This mechanism also protects the part during short-circuit and overload conditions by keeping the current through the inductor under control. A short-circuit protected regulator at V_{CCINT} supplies the LS driver. The LS switch only operates at V_{CCINT} voltages greater than 3.8V.

To further optimize efficiency, the LT3690 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 70µA in a typical application. Pulling the SYNC pin above 0.8V prevents Burst Mode operation. The positive edge of an external clock signal at the SYNC pin synchronizes the internal oscillator and therefore switching.

The oscillator reduces the LT3690's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during start-up and overload conditions.

The LT3690 contains a power good comparator which trips when the FB pin is at 90% of its regulated value. The PG output is an open-collector transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. Power good is valid when the LT3690 is enabled, the UVLO pin is high and V_{IN} is above 3.9V.

The LT3690 has an overvoltage protection feature which disables switching action when V_{IN} goes above 38V (typical) during transients. When switching is disabled, the LT3690 can safely sustain transient input voltages up to 60V.

APPLICATIONS INFORMATION

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.8V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

Setting the Switching Frequency

The LT3690 uses a constant frequency PWM architecture that can be programmed to switch from 150kHz to 1.5MHz by using a resistor tied from the RT pin to ground. Table 1 shows the necessary R_T value for a desired switching frequency.

Table 1. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.15	164
0.2	117
0.3	72.9
0.4	52.2
0.5	40.2
0.6	32.4
0.7	26.8
0.8	22.7
0.9	19.6
1.0	17.0
1.1	15.0
1.2	13.3
1.3	11.8
1.4	10.6
1.5	10.0

Operating Frequency Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, minimum dropout voltage, and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, lower maximum input voltage, and higher dropout voltage. The highest acceptable switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{LS}}{t_{ON(MIN)} \bullet (V_{IN} - V_{SW} + V_{LS})}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, V_{LS} is the LS switch drop (0.12V at maximum load) and V_{SW} is the internal switch drop (0.37V at maximum load). This equation shows that slower switching frequency is necessary to accommodate high V_{IN}/V_{OUT} ratio. Also, as shown in the Input Voltage Range section, lower frequency allows a lower dropout voltage. Input voltage range depends on the switching frequency because the LT3690 switch has finite minimum on and off times. An internal timer forces the switch to be off for at least $t_{OFF(MIN)}$ per cycle; this timer has a maximum value of 210ns over temperature. On the other hand, delays associated with turning off the power switch dictate the minimum on-time $t_{ON(MIN)}$ before the switch can be turned off; $t_{ON(MIN)}$ has a maximum value of 210ns (250ns for $T_J > 125°C$) over temperature. The minimum and maximum duty cycles that can be achieved taking minimum on and off times into account are:

$$DC_{MIN} = f_{SW} \bullet t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_{SW} \bullet t_{OFF(MIN)}$$

where f_{SW} is the switching frequency, the $t_{ON(MIN)}$ is the minimum switch on-time (210ns; 250ns for $T_J > 125°C$), and the $t_{OFF(MIN)}$ is the minimum switch off-time (210ns). These equations show that duty cycle range increases when switching frequency is decreased.

A good choice of switching frequency should allow adequate input voltage range (see Input Voltage Range section) and keep the inductor and capacitor values small.

APPLICATIONS INFORMATION

Input Voltage Range

The minimum input voltage is determined by either the LT3690's minimum operating voltage of 3.9V (V_{BIAS} > 3V) or by its maximum duty cycle (see equation in the Operating Frequency Trade-Offs section). The minimum input voltage due to duty cycle limitation is:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{LS}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{LS} + V_{SW}$$

where $V_{IN(MIN)}$ is the minimum input voltage, and $t_{OFF(MIN)}$ is the minimum switch off-time (210ns). Note that higher switching frequency will increase the minimum input voltage. If a lower dropout voltage is desired, a lower switching frequency should be used.

The maximum input voltage for LT3690 applications depends on switching frequency, the absolute maximum ratings of the V_{IN} and BST pins, and the operating mode. The LT3690 can operate from continuous input voltages up to 36V. If the operating junction temperature is below 125°C, the LT3690 will tolerate input voltage transients of up to 60V. However, note that while $V_{IN} > V_{OVLO}$ (typically 38V), the LT3690 will stop switching, allowing the output to fall out of regulation.

For a given application where the switching frequency and the output voltage are already fixed, the maximum input voltage that guarantees optimum output voltage ripple for that application can be found by applying the following expression:

$$V_{IN(MAX)} = \frac{V_{OUT} + V_{LS}}{f_{SW} \bullet t_{ON(MIN)}} - V_{LS} + V_{SW}$$

where $V_{IN(MAX)}$ is the maximum operating input voltage, V_{OUT} is the output voltage, V_{LS} is the LS switch drop (0.12V at maximum load), V_{SW} is the internal switch drop (0.37V at maximum load), f_{SW} is the switching frequency (set by RT), and $t_{ON(MIN)}$ is the minimum switch on-time (210ns; 250ns for T_J > 125°C). Note that a higher switching frequency will reduce the maximum operating input voltage. Conversely, a lower switching frequency will be necessary to achieve optimum operation at high input voltages. The maximum operating voltage is 36V (minimum overvoltage lockout threshold).

Special attention must be paid when the output is in start-up, short-circuit, or other overload conditions. In these cases, the LT3690 tries to bring the output in regulation by driving current into the output load. During these events, the inductor peak current might easily reach and even exceed the maximum current limit of the LT3690, especially in those cases where the switch already operates at minimum on-time. The circuitry monitoring the current through the LS switch prevents the HS switch from turning on again if the inductor valley current is above I_{PSDLIM} (5A nominal). In these cases, the inductor peak current is therefore the maximum current limit of the LT3690 plus the additional current overshoot during the turn-off delay due to minimum on-time:

$$I_{L(PEAK)} = 8A + \frac{V_{IN(MAX)} - V_{OUTOL}}{L} \bullet t_{ON(MIN)}$$

where $I_{L(PEAK)}$ is the peak inductor current, $V_{IN(MAX)}$ is the maximum expected input voltage, L is the inductor value, $t_{ON(MIN)}$ is the minimum on-time and V_{OUTOL} is the output voltage under the overload condition. The part is robust enough to survive prolonged operation under these conditions as long as the peak inductor current does not exceed 9A. Inductor current saturation and excessive junction temperature may further limit performance.

If the output is in regulation and no short-circuit, start-up, or overload events are expected, then input voltage transients of up to V_{OVLO} are acceptable regardless of the switching frequency. In this case, the LT3690 may enter pulse-skipping operation where some switching pulses are skipped to maintain output regulation. In this mode, the output voltage ripple and inductor current ripple will be higher than in normal operation.

APPLICATIONS INFORMATION

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = \left(V_{OUT} + V_{LS}\right) \bullet \frac{0.67MHz}{f_{SW}}$$

where V_{LS} is the voltage drop of the low side switch (0.12V), f_{SW} is in MHz, and L is in µH. The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be at least 30% higher. For highest efficiency, the series resistance (DCR) should be less than 0.03Ω. Table 2 lists several vendors and types that are suitable.

Table 2. Inductor Vendors

VENDOR	URL	PART SERIES
Murata	www.murata.com	LQH6P
TDK	www.tdk.com	CLF10040T SLF10165T
Toko	www.toko.com	DEM8045C FDVE1040
Coilcraft	www.coilcraft.com	MSS1048
Sumida	www.sumida.com	CDRH8D43 CDRH105R
Vishay	www.vishay.com	IHLP-2525EZ

The optimum inductor for a given application may differ from the one indicated by this simple design guide. A larger value inductor provides a higher maximum load current, and reduces the output voltage ripple. If your load is lower than the maximum load current, then you can relax the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR, resulting in higher efficiency. Be aware that if the inductance differs from the simple rule above, then the maximum load current will depend on input voltage. In addition, low inductance may result in discontinuous mode operation, which further reduces maximum load current. For details of maximum output current and discontinuous mode operation, see Application Note 44.

Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillations:

$$L_{MIN} = \left(V_{OUT} + V_{LS}\right) \bullet \frac{0.42MHz}{f_{SW}}$$

where V_{LS} is the voltage drop of the low side switch (0.12V at maximum load), f_{SW} is in MHz, and L_{MIN} is in µH.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT3690 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT3690 will deliver depends on the switch current limit, the inductor value, and the input and output voltages.

When the switch is off, the potential across the inductor is the output voltage plus the low side switch drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1-DC)\left(V_{OUT} + V_{LS}\right)}{\left(L \bullet f_{SW}\right)}$$

where f_{SW} is the switching frequency of the LT3690 and L is the value of the inductor. The peak inductor and switch current is:

$$I_{SW(PK)} = I_{L(PK)} = I_{OUT} + \frac{\Delta I_L}{2}$$

To maintain output regulation, this peak current must be less than the LT3690's switch current limit I_{LIM}. See the Typical Performance graphs for the change in current limit vs duty cycle.

Choosing an inductor value so that the ripple current is small will allow a maximum output current near the switch current limit.

APPLICATIONS INFORMATION

One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors, and choose one to meet cost or space goals. Then use these equations to check that the LT3690 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT} is less than $\Delta I_L/2$.

Input Capacitor

Bypass the input of the LT3690 circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 10µF ceramic capacitor is adequate to bypass the LT3690, and easily handles the ripple current. Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a lower performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3690 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 10µF capacitor is capable of this task, but only if it is placed close to the LT3690 (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3690. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3690 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3690's maximum voltage rating. See Application Note 88 for more details.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3690 to produce the DC output. In this role it determines the output ripple, and low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3690's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{150}{V_{OUT} \bullet f_{SW}}$$

where f_{SW} is in MHz, and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types, which will provide low output ripple and good transient response. Using a high value capacitor on the output can improve transient performance, but a phase lead capacitor across the feedback resistor R1 may be required to get the full benefit (see the Frequency Compensation section).

High performance electrolytic capacitors can be used for the output capacitor. If using an electrolytic capacitor, choose one intended for use in switching regulators, and with a specified ESR of 0.03Ω or less. Such a capacitor will be larger than a ceramic capacitor and will have a larger capacitance because the capacitor must be large to achieve low ESR. Table 3 lists several capacitor vendors.

Table 3. Capacitor Vendors

VENDOR	PART SERIES	COMMENTS
Panasonic	Ceramic, Polymer, Tantalum	EEF Series
Kemet	Ceramic, Tantalum	T494, T495
Sanyo	Ceramic, Polymer, Tantalum	POSCAP
Murata	Ceramic	
AVX	Ceramic, Tantalum	TPS Series
Taiyo Yuden	Ceramic	

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can sometimes cause problems when used with the LT3690 due to their piezoelectric nature. When in Burst Mode operation, the LT3690's switching frequency depends on the load current, and at very light loads the LT3690 can excite the ceramic capacitor at audio frequencies, generating audible

APPLICATIONS INFORMATION

noise. Since the LT3690 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

Frequency Compensation

The LT3690 uses current mode control to regulate the output. This simplifies loop compensation. In particular, the LT3690 does not require the ESR of the output capacitor for stability, so you are free to use ceramic capacitors to achieve low output ripple and small circuit size.

Frequency compensation is provided by the components tied to the V_C pin, as shown in Figure 1. Generally a capacitor (C_C) and a resistor (R_C) in series to ground are used. In addition, there may be a lower value capacitor in parallel. This capacitor (C_F) is not part of the loop compensation but is used to filter noise at the switching frequency, and is required only if a phase-lead capacitor is used or if the output capacitor has high ESR.

Loop compensation determines the stability and transient performance. The best values for the compensation network depend on the application and, in particular, the type of output capacitor. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

Figure 1 shows an equivalent circuit for the LT3690 control loop. The error amplifier is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current, and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. In most cases, a zero is required and comes either from the output capacitor ESR or from a resistor R_C in series with C_C. This simple model works well as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (CPL) across the feedback divider may improve the transient response.

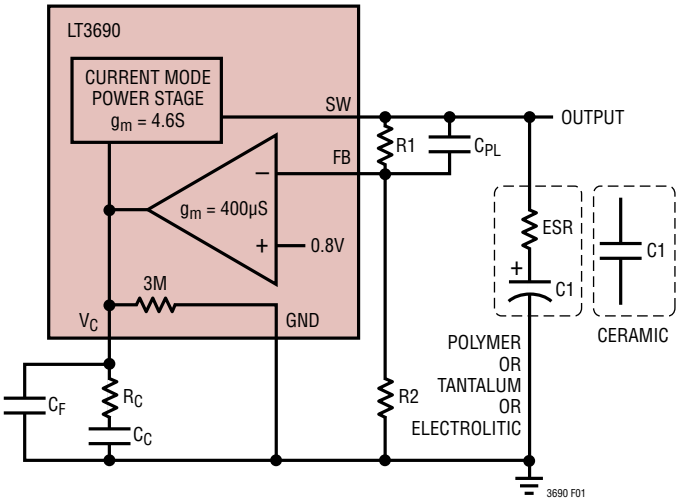
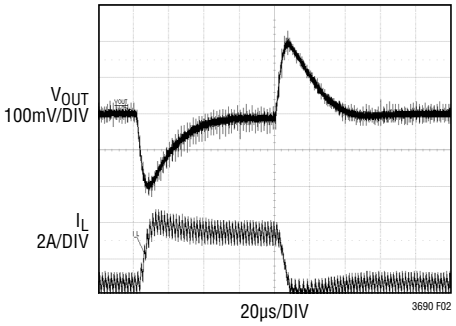


Figure 1. Model for Loop Response



V_{IN} = 12V, I_{LOAD} STEPPED BETWEEN 0.6A AND 3.5A
FRONT PAGE APPLICATION

Figure 2. Transient Load Response

APPLICATIONS INFORMATION

Low-Ripple Burst Mode and Pulse-Skipping Mode

The LT3690 is capable of operating in either low ripple Burst Mode operation or pulse-skipping mode, which is selected using the SYNC pin. See the Synchronization and Mode section for details.

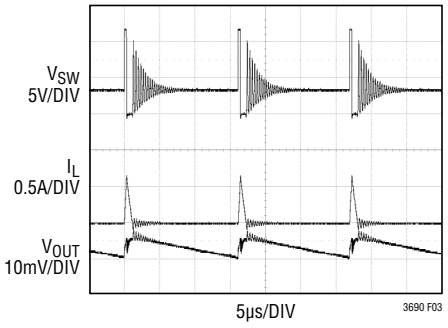
To enhance efficiency at light loads, the LT3690 can be operated in low ripple Burst Mode operation that keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LT3690 delivers single cycle bursts of current to the output capacitor followed by sleep periods where the output capacitor is delivers output power to the load. Because the LT3690 delivers power to the output with single, low current pulses, the output ripple stays below 15mV for a typical application. In addition, V_{IN} and BIAS quiescent currents are reduced to 35µA and 70µA (typical), respectively, during the sleep time. As the load current decreases towards a no-load condition, the percentage of time that the LT3690 operates in sleep mode increases and the average input current is greatly reduced, resulting in high efficiency even at very low loads (see Figure 3). At higher output loads (above about 385mA at V_{IN} = 12V for the front page application) the LT3690 will run at the frequency programmed by the R_T resistor, and operate in standard PWM mode. The transition between PWM and low ripple Burst Mode operation is seamless, and does not disturb the output voltage.

If low quiescent current is not required, the LT3690 can operate in pulse-skipping mode. The benefit of this mode is that the LT3690 will enter full frequency standard PWM operation at a lower output load current than when in Burst Mode operation. The front page application circuit will switch at full frequency at output loads higher than about 64mA at V_{IN} = 12V.

Low Side Switch Considerations

The operation of the internal low side switch is optimized for reliable, high efficiency operation. The low side switch is connected in parallel with a catch diode. When the top side switch turns off, the inductor current pulls the SW pin low, and forward biases the internal catch diode. In order to prevent shoot through currents, the internal low side switch only turns on after detecting the SW pin going low. Once the low side switch turns on, the voltage drop between SW and GND is very small, minimizing power loss and improving efficiency. At the end of the switching cycle, the low side switch turns off, and after a delay, the top side switch can turn on again. The switching sequence is shown in Figure 4.

The overload comparator monitors the current flowing through the low side switch and helps protect the circuit. This comparator delays switching if the low side switch current goes higher than 5A (typical) during a fault condition such as a shorted output with high input voltage.



V_{IN} = 12V: I_{LOAD} = 20mA
FRONT PAGE APPLICATION

Figure 3. Burst Mode Operation

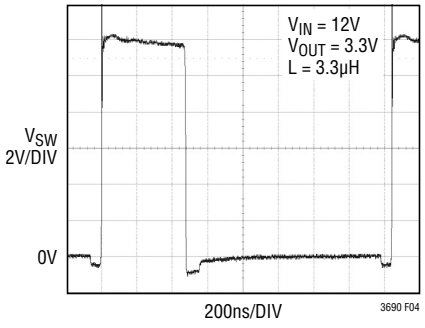


Figure 4. Switching Sequence of High Side, Catch Diode and Low Side Switch

APPLICATIONS INFORMATION

The switching will only resume once the low side switch current has fallen below the 5A limit. This way, the comparator regulates the valley current of the inductor to 5A during short-circuit. With properly chosen external components, this will ensure that the part will survive a short-circuit event.

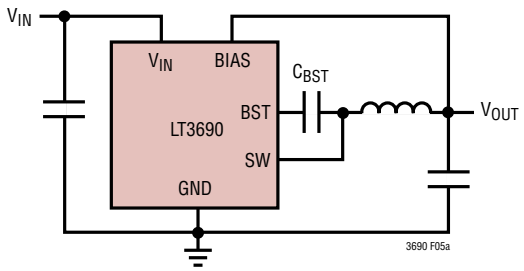
V_{CCINT} Considerations

The linear voltage regulator requires a capacitor of 0.47µF to deliver the peak current for the gate driver of the low side N-channel transistor. The output voltage is monitored by a comparator. To ensure proper operation, the low side driver only turns on if V_{CCINT} is above 3.8V (typ).

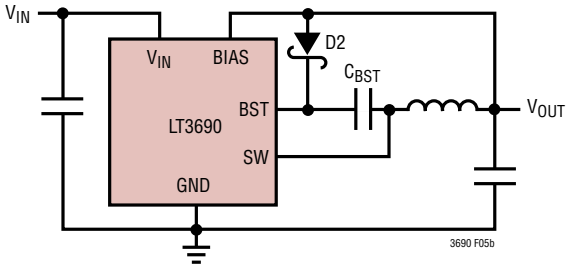
BST and BIAS Pin Considerations

Capacitor C_{BST} and the internal boost Schottky diode (see the Block Diagram) are used to generate boost voltages that are higher than the input voltage. In most cases a 0.68µF capacitor will work well. Figure 5 shows three ways to arrange the boost circuit. The BST pin must be more than 2.3V above the SW pin for best efficiency. For outputs of 3V and above, the standard circuit (Figure 5a) is best. For outputs between 2.8V and 3V, use a 1µF boost capacitor. A 2.5V output presents a special case because it is marginally adequate to support the boosted drive stage while using the internal boost diode. For reliable BST pin operation with 2.5V outputs, use a good external Schottky diode (such as the ON Semi MBR0540), and a 1µF boost capacitor (see Figure 5b). For lower output voltages, the boost diode can be tied to the input (Figure 5c), or to another supply greater than 2.8V. The circuit in Figure 5a is more efficient because the BST pin current and BIAS pin quiescent current comes from a lower voltage source. However, the full benefit of the BIAS pin is not realized unless it is at least 3V. Ensure that the maximum voltage ratings of the BST and BIAS pins are not exceeded.

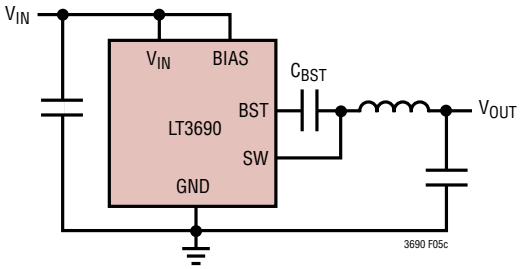
The minimum operating voltage of an LT3690 application is limited by the minimum input voltage (3.9V) and by the maximum duty cycle as outlined in the Input Voltage Range section. For proper start-up, the minimum input



(5a) $V_{OUT} > 2.8$



(5b) $2.5V < V_{OUT} < 2.8V$



(5c) $V_{OUT} < 2.5V$, $V_{IN(MAX)} = 27V$

Figure 5. Three Circuits for Generating the Boost Voltage

APPLICATIONS INFORMATION

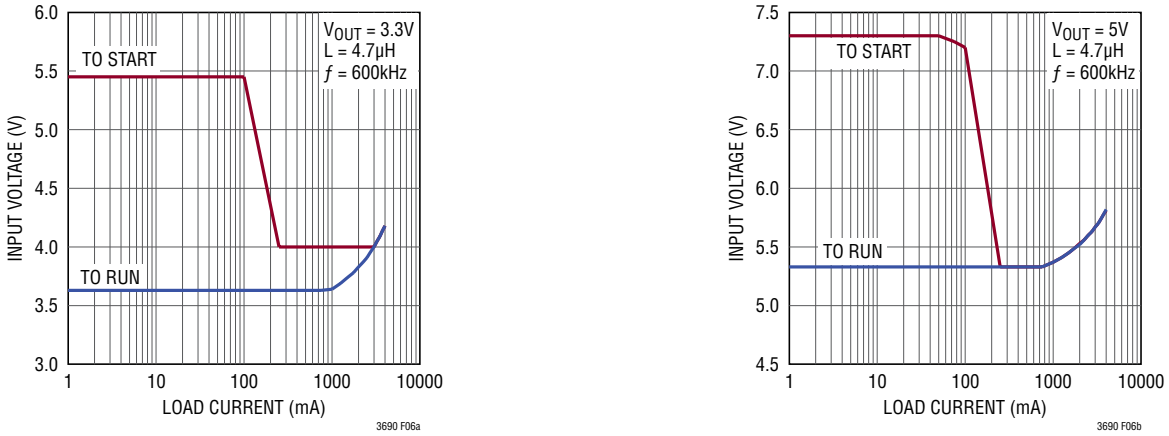


Figure 6. The Minimum Input Voltage Depends on Output Voltage, Load Current and Boost Circuit

voltage is also limited by the boost circuit. If the input voltage is ramped slowly, or the LT3690 is turned on with its EN pin when the output is already in regulation, then the boost capacitor may not be fully charged. Because the boost capacitor charges with the energy stored in the inductor, the circuit relies on some minimum load current to get the boost circuit running properly. This minimum load depends on the input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. Figure 6 shows a plot of minimum load to start and to run as a function of input voltage. In many cases the discharged output capacitor will present a load to the switcher, which will allow it to start. The plots show the worst-case situation, where V_{IN} is ramping very slowly. For lower start-up voltage, the boost diode can be tied to V_{IN} ; however, this restricts the input range to one-half of the absolute maximum rating of the BST pin. At light loads, the inductor current becomes discontinuous and the effective duty cycle can be very high. This reduces the minimum input voltage to approximately 300mV above V_{OUT}. At higher load currents, the inductor current is continuous and the duty cycle is limited by the maximum duty cycle of the LT3690, requiring a higher input voltage to maintain regulation.

Soft-Start

The SS (soft-start) pin provides a soft-start function. If a capacitor C_{SS} is tied from the SS pin to ground, then the internal pull-up current will generate a voltage ramp on this pin. A good value for the soft-start capacitor is $C_{OUT}/10000$, where C_{OUT} is the value of the output capacitor.

The soft-start function limits peak input current to the circuit during start-up. The output of the LT3690 regulates to the lowest voltage present at either the SS pin or an internal 0.8V reference. A capacitor from the SS pin to ground is charged by an internal 2µA current source resulting in a linear output ramp from 0V to the regulated output voltage. The ramp duration is given by:

$$t_{RAMP} = \frac{C_{SS} \bullet 0.8V}{2\mu A}$$

At power-up, an internal open-collector output discharges the SS pin. The SS pin can be left floating if the soft-start feature is not used. The internal current sources will charge this pin to ~2V as shown in Figure 7.

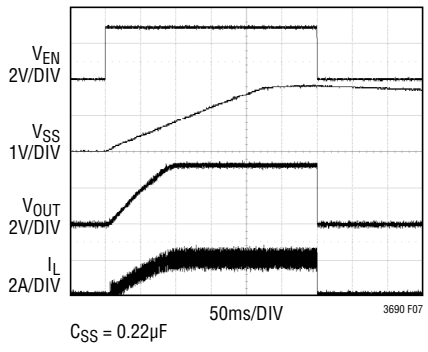
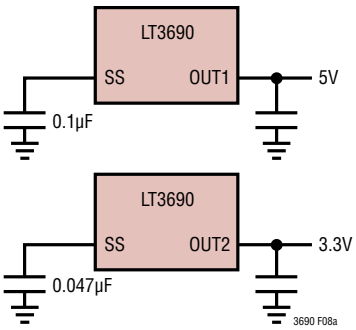
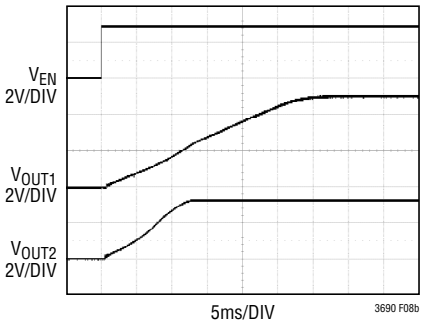


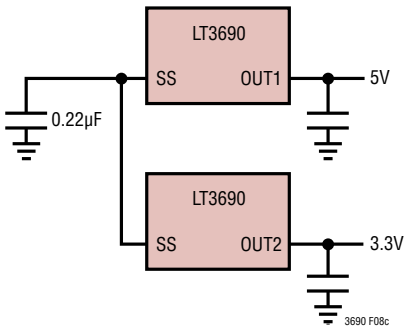
Figure 7. Soft-Start Ramp

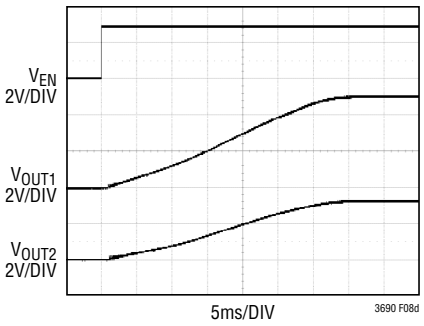
APPLICATIONS INFORMATION





(8a) Independent Start-Up

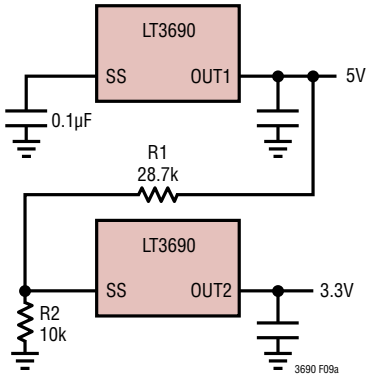


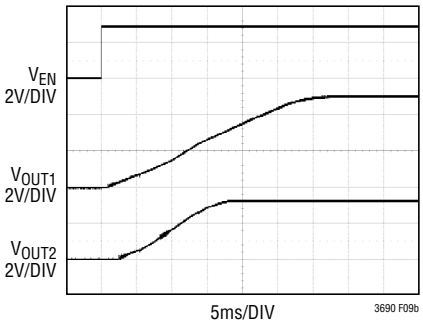


(8b) Ratiometric Start-Up

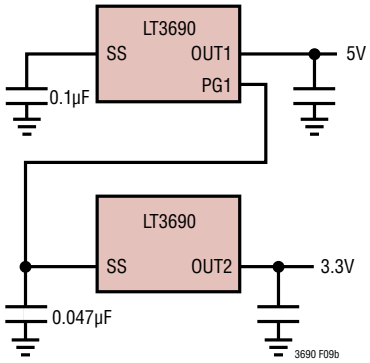
Figure 8. Output Tracking and Sequencing

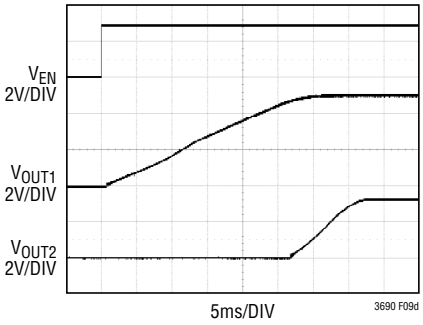
APPLICATIONS INFORMATION





(9a) Coincident Start-Up





(9b) Output Sequencing

Figure 9. Output Tracking and Sequencing

APPLICATIONS INFORMATION

Output Tracking and Sequencing

Output tracking and sequencing between voltage regulators can be implemented using the LT3690's SS and PG pins. Figure 8 and Figure 9 show several configurations for output tracking and sequencing of the LT3690 and an additional regulator. Independent soft-start for each channel is shown in Figure 8a. The output ramp time for each output is set by the soft-start capacitor as described in the Soft-Start section.

Ratiometric tracking is achieved in Figure 8b by connecting SS pins of two regulators together. In this configuration, the SS pin current is set by the sum of the SS pin currents of the two regulators, which must be taken into account when calculating the output rise time.

By connecting a feedback network from OUT1 to the SS pin with the same ratio that set the OUT2 voltage, absolute tracking shown in Figure 9a is implemented. A small OUT2 voltage offset will be present due to the SS pin's 2µA source current. This offset can be corrected by slightly reducing the value of R2.

Figure 9b illustrates output sequencing. When V_{OUT1} is within 10% of its regulated voltage, PG releases the SS soft-start pin, allowing V_{OUT2} to soft-start.

Synchronization

To select low-ripple Burst Mode operation, tie the SYNC pin below 0.4V (this can be ground or a logic output). Synchronize the LT3690 oscillator to an external frequency by connecting a square wave (with positive and negative pulse width > 100ns) to the SYNC pin. The square wave amplitude should have valleys that are below 0.4V and peaks that are above 1V (up to 6V).

The LT3690 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will skip pulses to maintain regulation.

The LT3690 may be synchronized over a 170kHz to 1.5MHz range. The R_T resistor should be chosen to set the LT3690 switching frequency 20% below the lowest synchronization input. For example, if the synchronization signal will be 350kHz and higher, choose R_T for 280kHz.

To assure reliable and safe operation, the LT3690 will synchronize when the output voltage is above 90% of its regulated voltage. It is therefore necessary to choose a large enough inductor value to supply the required output current at the frequency set by the R_T resistor (see the Inductor Selection and Maximum Output Current section). It is also important to note that slope compensation is set by the R_T value. When the synchronization frequency is much higher than the one set by R_T, the slope compensation is significantly reduced, which may require a larger inductor value to prevent sub-harmonic oscillation.

For duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillations:

$$L_{MIN} = (V_{OUT} + V_{LS}) \bullet \frac{0.42MHz}{f_{SW}}$$

where V_{LS} is the voltage drop of the low side switch (0.12V at maximum load), f_{SW} is in MHz, and L_{MIN} is in µH. For f_{SW} in the above calculation, use the frequency programmed by R_T, not the synchronization frequency.

Undervoltage Lockout

Figure 10 shows how to add undervoltage lockout (UVLO) to the LT3690. Typically, UVLO is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current

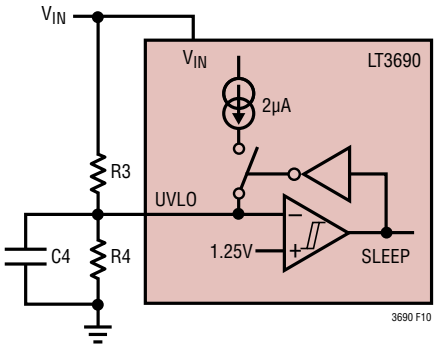


Figure 10. Undervoltage Lockout

APPLICATIONS INFORMATION

limit or latch low under low source voltage conditions. The UVLO circuitry prevents the regulator from operating at source voltages where the problems might occur. An internal comparator will force the part into shutdown below the fixed V_{IN} UVLO threshold of 3.0V. This feature can be used to prevent excessive discharge of battery-operated systems. If an adjustable UVLO threshold is required, the UVLO pin can be used. The threshold voltage of the UVLO pin comparator is 1.25V. Current hysteresis is added above the UVLO threshold. This can be used to set voltage hysteresis of the UVLO using the following equations:

$$R3 = \frac{V_H - V_L}{2\mu A}$$

$$R4 = R3 \bullet \frac{1}{\frac{V_H}{1.25V} - 1}$$

Example: switching should not start until the input is above 4.4V, and is to stop if the input falls below 4V.

$$R3 = \frac{4.4V - 4.0V}{2\mu A} = 200k\Omega$$

$$R4 = 200k\Omega \bullet \frac{1}{\frac{4.4V}{1.25V} - 1} = 79.4k\Omega$$

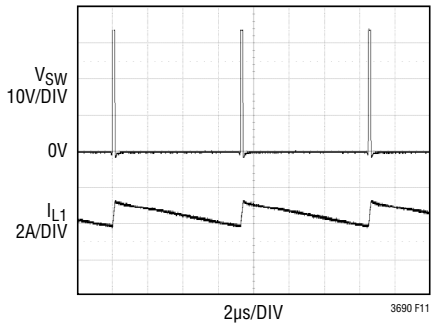


Figure 11. The LT3690 Reduces its Frequency to Below 250kHz to Protect Against Shorted Output with 36V Input

Keep the connection from the resistor to the UVLO pin short and minimize the interplane or surface capacitance to switching nodes. If high resistor values are used, the UVLO pin should be bypassed with a 1nF capacitor to prevent coupling problems from the switch node.

Shorted and Reversed Input Protection

If the inductor is chosen to prevent excessive saturation, the LT3690 will tolerate a shorted output. When operating in short-circuit condition, the LT3690 will reduce its frequency until the valley current is at a typical value of 5A (see Figure 11). There is another situation to consider in systems where the output is held high when the input to the LT3690 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LT3690's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT3690's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate a few mA in this state. If the EN pin is grounded, the SW pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, then parasitic diodes inside the LT3690 can pull large currents from the output through the SW pin and the V_{IN} pin. Figure 12 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

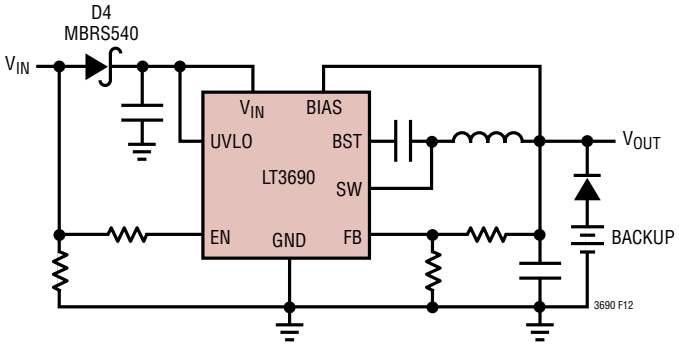


Figure 12. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output; It Also Protects the Circuit from a Reversed Input. The LT3690 Runs Only When the Input Is Present

APPLICATIONS INFORMATION

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 13 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3690's V_{IN}, SW and GND pins and the input capacitor (C_{IN}). The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The SW and BST nodes should be small as possible. If synchronizing the part externally using the SYNC pin, avoid routing this signal near sensitive nodes, especially V_C and FB. Finally, keep the FB and V_C nodes small so that the ground traces will shield them from the SW and BST nodes. The exposed GND pad on the bottom of the package must be soldered to ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT3690 to additional ground planes within the circuit board and on the bottom side. In addition, the exposed SW pad on the bottom of the package must be soldered to the PCB to act as a heat sink for the low side switch. Add thermal vias under the SW pad and to the bottom side.

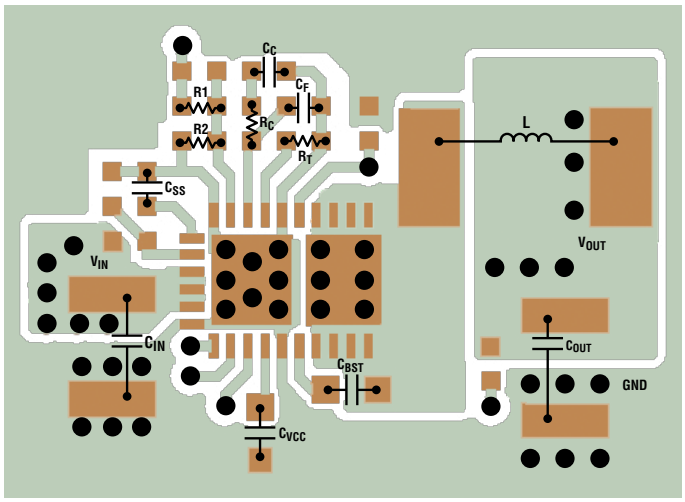


Figure 13. Top Layer PCB Layout and Component Placement in the LT3690 Demonstration Board

High Temperature Considerations

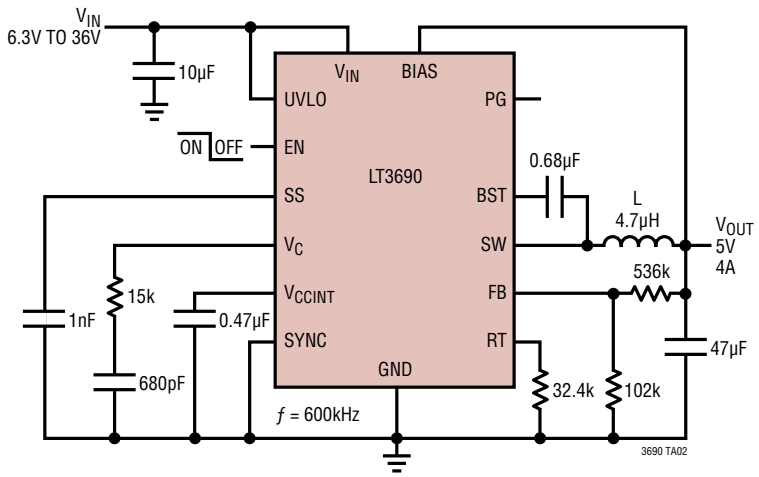
The PCB must provide heat sinking to keep the LT3690 cool. The GND exposed pad on the bottom of the package must be soldered to a ground plane and the SW exposed pad must be soldered to a SW plane. Tie the ground plane and SW plane to large copper layers below with thermal vias; these layers will spread the heat dissipated by the LT3690. Placing additional vias can reduce thermal resistance further. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to θ_{JA} = 40°C/W or less. With 100 LFPM airflow, this resistance can fall by another 25%. Further increases in airflow will lead to lower thermal resistance. Because of the large output current capability of the LT3690, it is possible to dissipate enough heat to raise the junction temperature beyond the absolute maximum of 125°C (150°C for H-grade or MP-grade). When operating at high ambient temperatures, the maximum load current should be derated as the ambient temperature approaches the maximum junction temperature. Power dissipation within the LT3690 can be estimated by calculating the total power loss from an efficiency measurement. The die temperature is calculated by multiplying the LT3690 power dissipation by the thermal resistance from junction-to-ambient. Thermal resistance depends on the layout of the circuit board, but values from 20°C/W to 60°C/W are typical. Die temperature rise was measured on a 4-layer, 6cm • 6cm circuit board in still air at a load current of 4A (f_{SW} = 600kHz). For a 12V input to 3.3V output the die temperature elevation above ambient was 43°C; for $24V_{IN}$ to $3.3V_{OUT}$ the rise was 52°C; for $12V_{IN}$ to $5V_{OUT}$ the rise was 55°C and for $24V_{IN}$ to $5V_{OUT}$ the rise was 62°C.

Other Analog Devices Publications

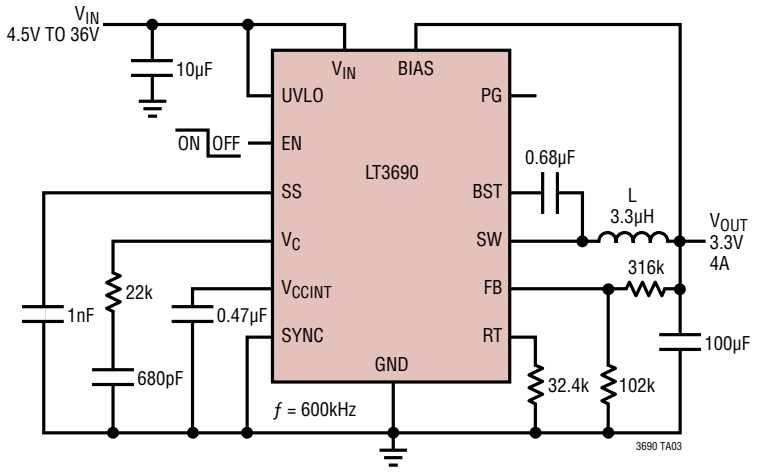
Application Notes 19, 35 and 44 contain detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 318 shows how to generate a bipolar output supply using a buck regulator.

TYPICAL APPLICATIONS

5V Step-Down Converter



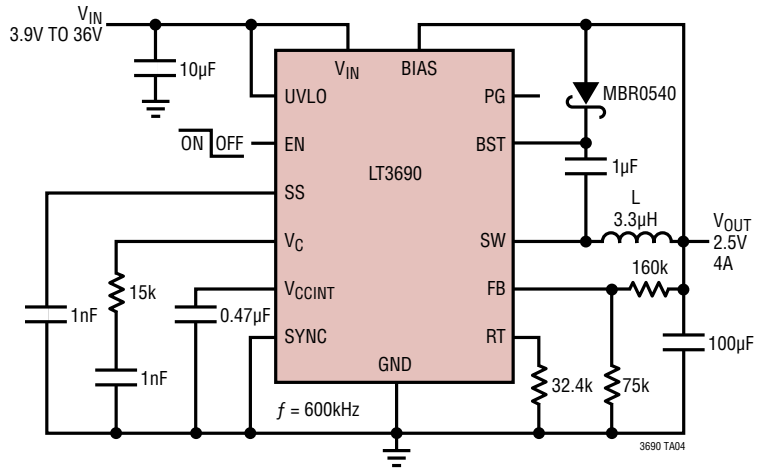
3.3V Step-Down Converter



(FIXED FREQUENCY AT V_{IN} < 26V)

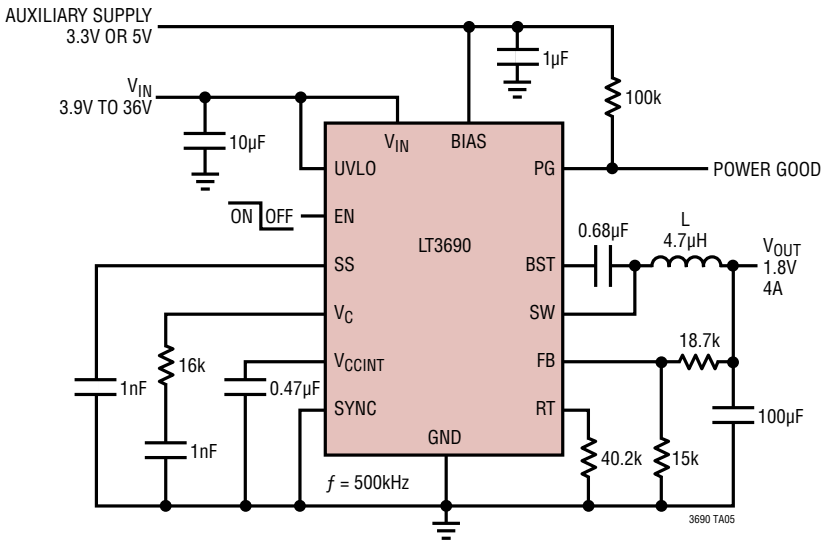
TYPICAL APPLICATIONS

2.5V Step-Down Converter



(FIXED FREQUENCY AT V_{IN} < 21V)

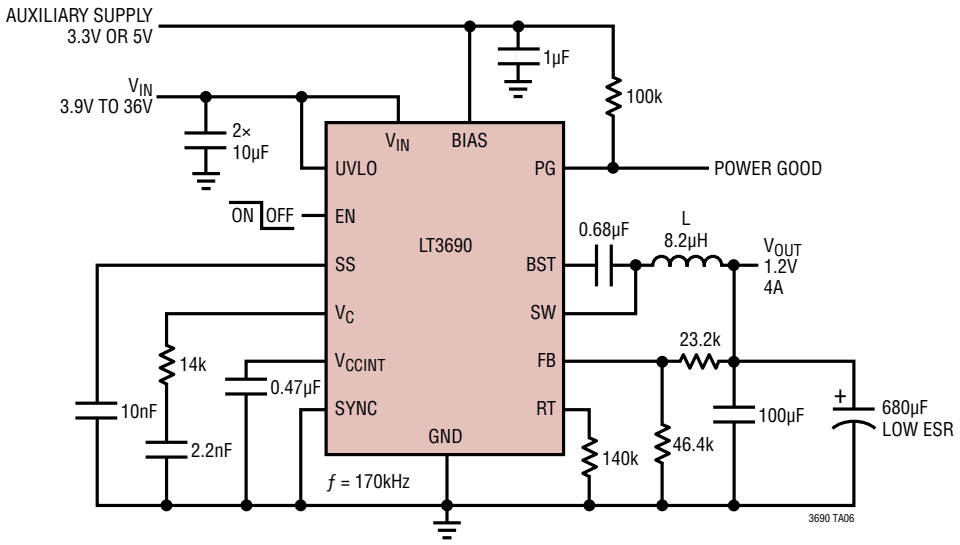
1.8V Step-Down Converter



(FIXED FREQUENCY AT V_{IN} < 18.5V)
(POWER GOOD IS ONLY VALID WHEN EN IS HIGH AND V_{IN} > 3.9V)

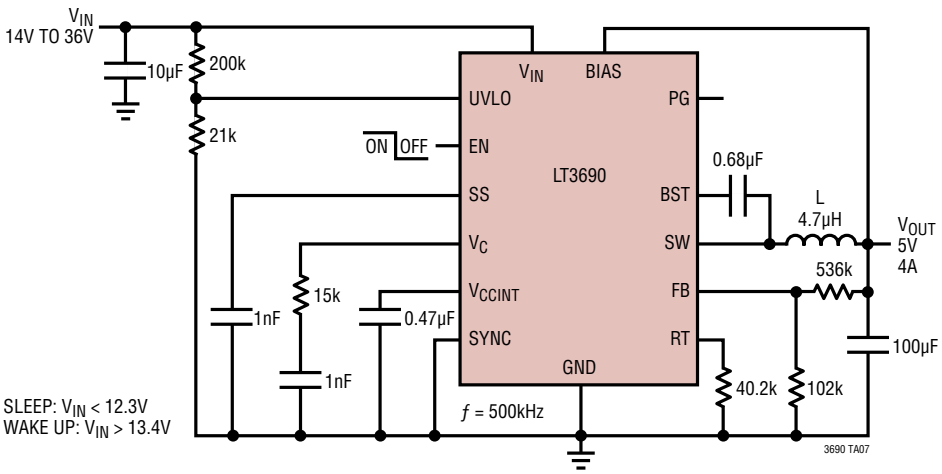
TYPICAL APPLICATIONS

1.2V Step-Down Converter



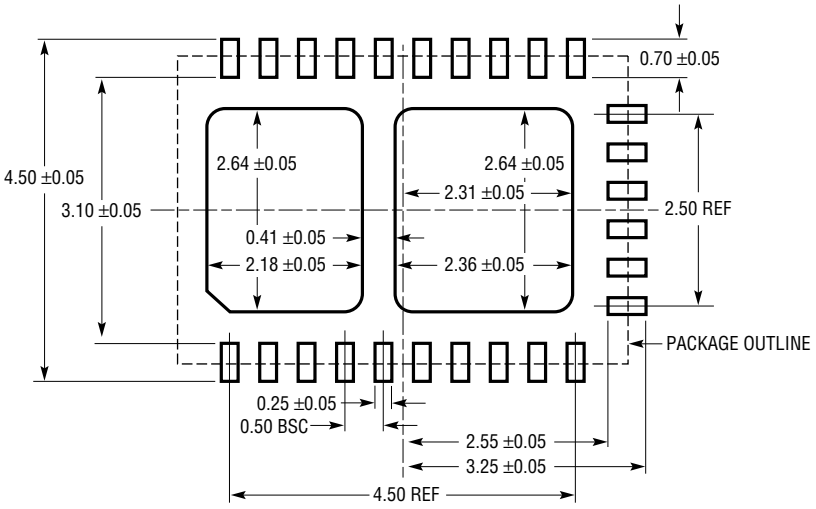
(POWER GOOD IS ONLY VALID WHEN EN IS HIGH AND V_{IN} > 3.9V)

5V Step-Down Converter with Undervoltage Lockout

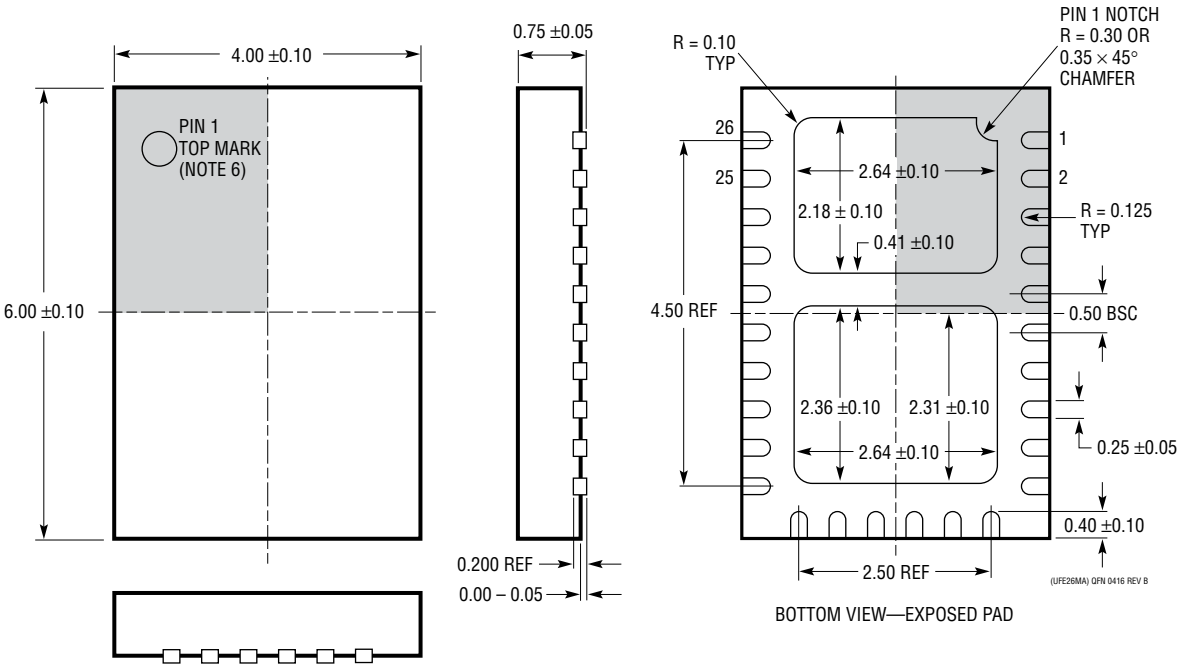


PACKAGE DESCRIPTION

UFE Package
Variation: UFE26MA
26-Lead Plastic QFN (4mm × 6mm)
(Reference LTC DWG # 05-08-1770 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

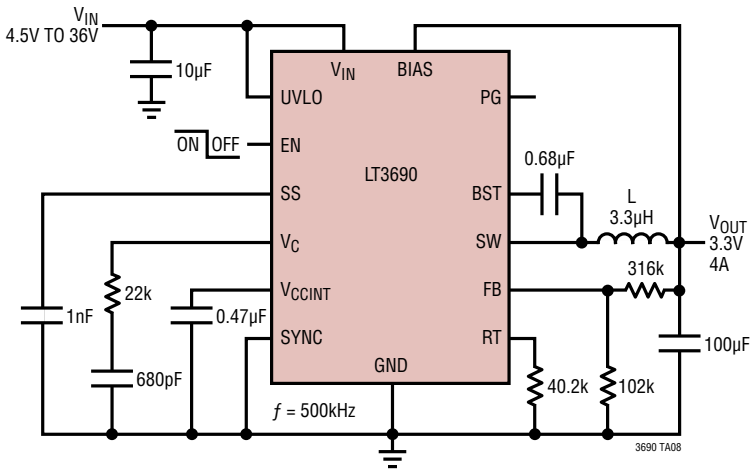
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	9/11	Added H- and MP-grades.	2 to 8, 13, 25
		Revised BIAS pin description in Pin Functions section.	9
B	11/15	Clarified ULVO Pin Current Hysteresis Conditions	3
		Clarified SS (Pin 11) and PG (Pin 18) Descriptions	9
		Clarified Power Good Description Paragraph	11
		Clarified 1.8V and 1.2V Step-Down Converter Schematics	26, 27
C	1/20	Updated data sheet to reflect ADI format	1, 2, 28
		Updated switching frequency vs R_T value from 9.59kΩ to 10.0kΩ	12

TYPICAL APPLICATION

3.3V Step-Down Converter



(FIXED FREQUENCY AT V_{IN} < 31V)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3680	36V, 3.5A, 2.4MHz High Efficiency MicroPower Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3972	Transients to 60V, 3.5A, 2.4MHz High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 33V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3971	38V, 1.2A (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.8µA of Quiescent Current	$V_{IN(MIN)}$ = 4.3V, $V_{IN(MAX)}$ = 38V, $V_{OUT(MIN)}$ = 1.19V, I_Q = 2.8µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3991	55V, 1.2A (I_{OUT}), 2MHz, High Efficiency Step-Down DC/DC Converter with Only 2.8µA of Quiescent Current	$V_{IN(MIN)}$ = 4.3V, $V_{IN(MAX)}$ = 38V, $V_{OUT(MIN)}$ = 1.19V, I_Q = 2.8µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3685	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} <1µA, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3500	36V, 40V_{MAX}, 2A, 2.5MHz High Efficiency Step-Down DC/DC Converter and LDO Controller	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} <10µA, 3mm × 3mm DFN-10 Package
LT3507	36V 2.5MHz, Triple (2.4A + 1.5A + 1.5A (I_{OUT})) with LDO Controller High Efficiency Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 4.0V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 7mA, I_{SD} = 1µA, 5mm × 7mm QFN-38 Package
LT3682	36V, 60V_{MAX}, 1A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter	$V_{IN(MIN)}$ = 3.6V, $V_{IN(MAX)}$ = 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} <1µA, 3mm × 3mm DFN-12 Package