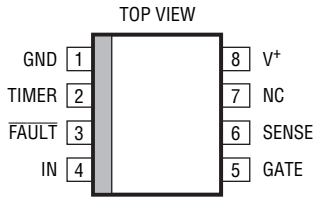
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Pin 8) ..... –15V to 60V
Input Voltage (Pin 4)..... (GND – 0.3V) to 15V
GATE Voltage (Pin 5)..... 75V
SENSE Voltage (Pin 6) ..... V^+ ±5V
$\overline{FAULT}$ Voltage (Pin 3) 36V
Current (Pins 1, 2, 4, 5, 6, 8) 40mA
Operating Temperature Range (Note 2)
LT1910E.....–40°C to 85°C
LT1910I.....–40°C to 125°C
Junction Temperature Range ..... –40°C to 125°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .....300°C

PIN CONFIGURATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1910ES8#PBF	LT1910ES8#TRPBF	1910	8-Lead Plastic SO	–40°C to 85°C
LT1910IS8#PBF	LT1910IS8#TRPBF	1910	8-Lead Plastic SO	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT1910ES8	LT1910ES8#TR	1910	8-Lead Plastic SO	–40°C to 85°C
LT1910IS8	LT1910IS8#TR	1910	8-Lead Plastic SO	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 12V to 48V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Supply Current (Off State)	V^+ = 48V, V_{IN} = 0.8V		1.2	1.9	2.5	mA
$\Delta I_{S(ON)}$	Delta Supply Current (On State)	V_{IN} = 2V, Measure Increase in I_S			0.8	1.2	mA
V_{INH}	Input High Voltage	E-Grade I-Grade	● ●	2 3.5			V V
V_{INL}	Input Low Voltage	E-Grade I-Grade	● ●			0.8 0.7	V V
I_{IN}	Input Current	V_{IN} = 2V V_{IN} = 5V	● ●	15 55	30 110	50 185	µA µA
C_{IN}	Input Capacitance (Note 3)				5		pF
$V_{T(TH)}$	Timer Threshold Voltage	V_{IN} = 2V, Adjust V_T	●	2.6	2.9	3.2	V
$V_{T(CL)}$	Timer Clamp Voltage	V_{IN} = 0.8V		3.2	3.5	3.8	V
I_T	Timer Charge Current	V_{IN} = V_T = 2V		9	14	20	µA
V_{SENSE}	Drain-Sense Threshold Voltage Temperature Coefficient (Note 3)			50	65 0.33	80	mV %/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 12V to 48V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SENSE}	Drain Sense Input Current	V^+ = 48V, V_{SENSE} = 65mV			0.5	1.5	µA
$V_{GATE} – V^+$	Gate Voltage Above Supply	V^+ = 8V		4	4.5	6	V
		V^+ = 12V	●	7	8.5	10	V
		V^+ = 24V					
		E-Grade	●	10	12	14	V
		I-Grade	●	10	12	15	V
		V^+ = 48V					
		E-Grade	●	10	12	14	V
		I-Grade	●	10	12	15	V
$V_{F(TH)}$	$\overline{FAULT}$ Output High Threshold Voltage	V_{IN} = 2V, I_F = 1mA, Adjust V_T		3.1	3.4	3.7	V
	$\overline{FAULT}$ Output Low Threshold Voltage			3.0	3.3	3.6	V
V_{FOL}	$\overline{FAULT}$ Output Low Voltage	I_F = 1mA	●		0.07	0.4	V
t_{ON}	Turn-On Time	V^+ = 24V, V_{GATE} = 32V, C_{GATE} = 1nF		100	220	400	µs
t_{OFF}	Turn-Off Time	V^+ = 24V, V_{GATE} = 2V, C_{GATE} = 1nF			25	100	µs
$t_{OFF(CL)}$	Current Limit Turn-Off Time	V^+ = 24V, ($V^+ – V_{SENSE}$)→0.1V, C_{GATE} = 1nF			20	50	µs

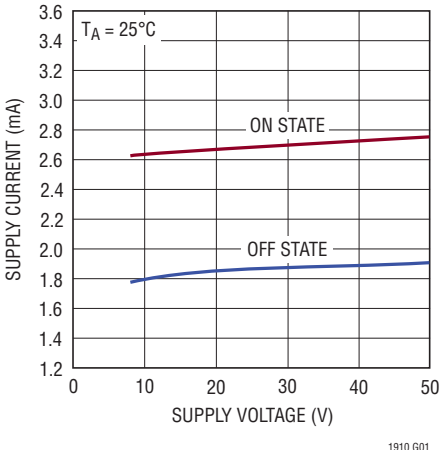
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT1910E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT1910I is guaranteed to meet performance specifications over the full –40°C to 125°C operating temperature range.

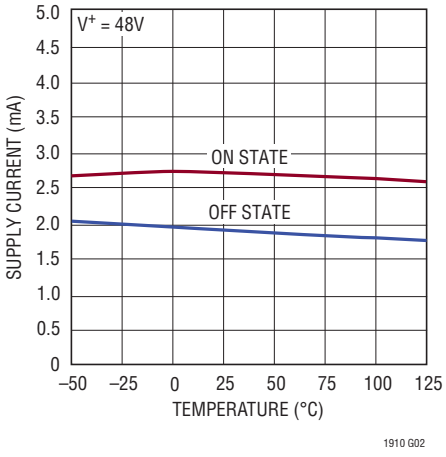
Note 3: Guaranteed but not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

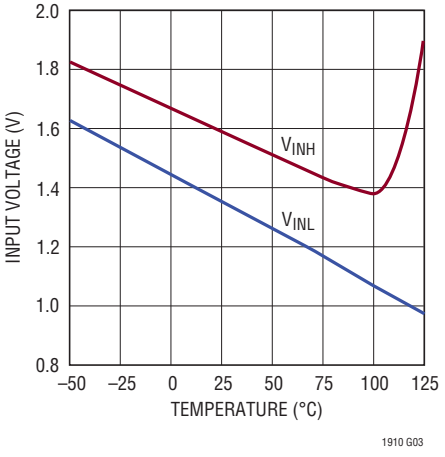
Supply Current vs Supply Voltage



Supply Current vs Temperature

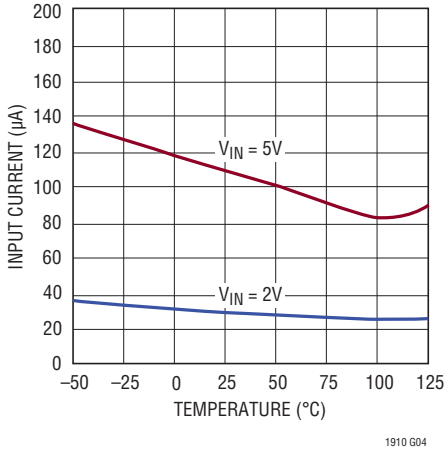


Input Voltage vs Temperature

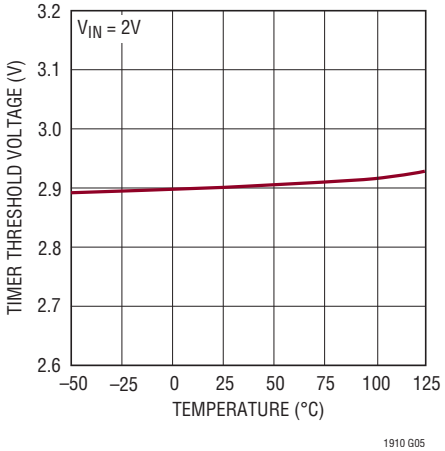


TYPICAL PERFORMANCE CHARACTERISTICS

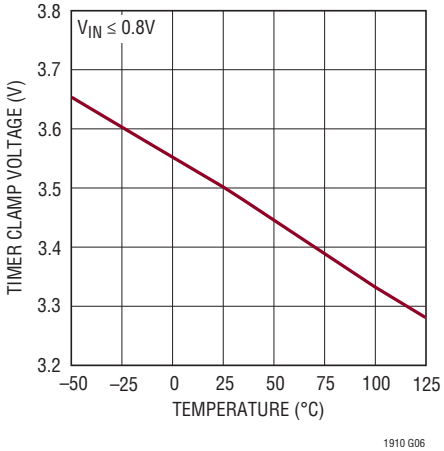
Input Current vs Temperature



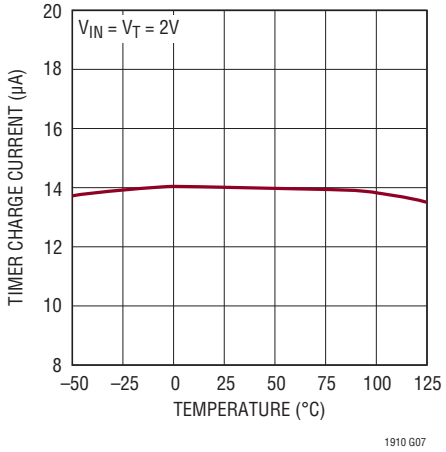
Timer Threshold Voltage vs Temperature



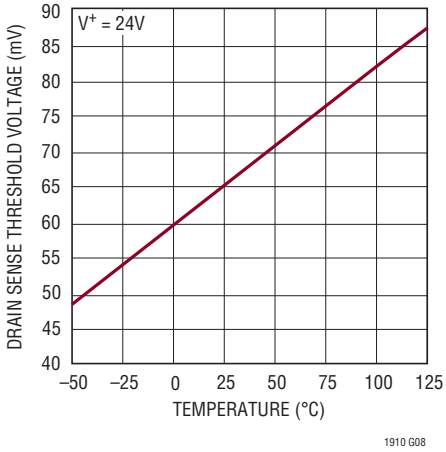
Timer Clamp Voltage vs Temperature



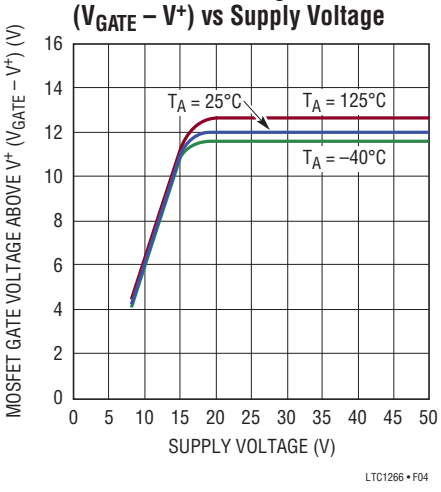
Timer Charge Current vs Temperature



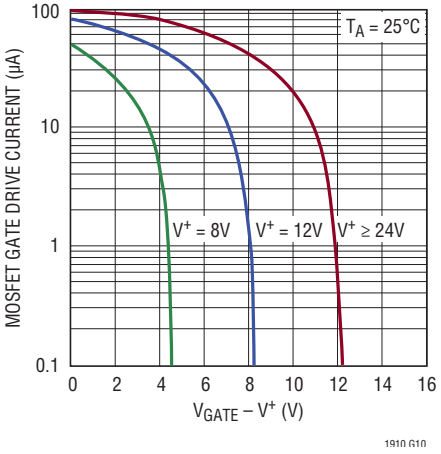
Drain Sense Threshold Voltage vs Temperature



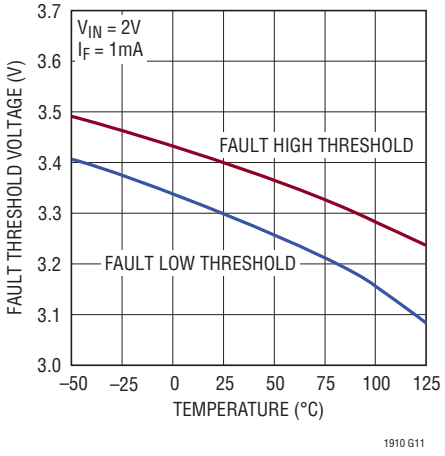
MOSFET Gate Voltage Above V+ (V_{GATE} – V+) vs Supply Voltage



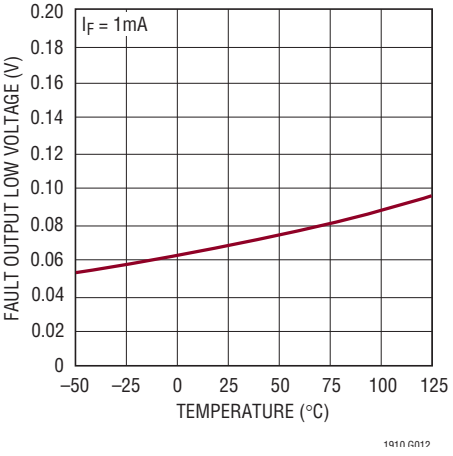
MOSFET Gate Drive Current vs V_{GATE} – V+



Fault Threshold Voltage vs Temperature

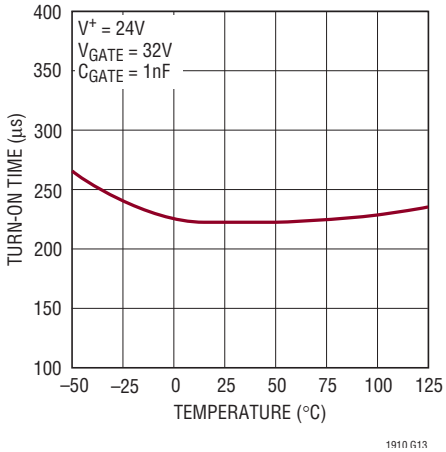


Fault Output Low Voltage vs Temperature

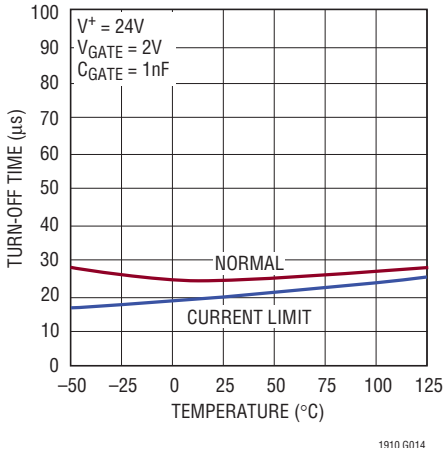


TYPICAL PERFORMANCE CHARACTERISTICS

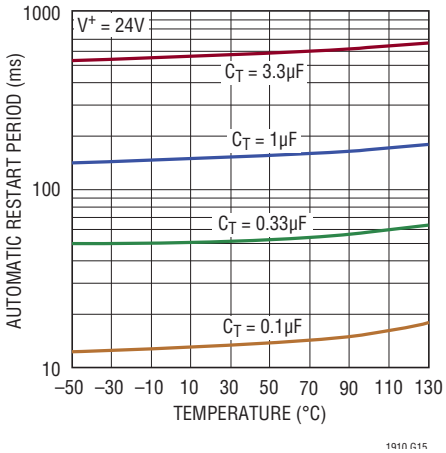
Turn-On Time vs Temperature



Turn-Off Time vs Temperature



Automatic Restart Period vs Temperature



PIN FUNCTIONS

GND (Pin 1): Common Ground.

TIMER (Pin 2): A timing capacitor, C_T, from the TIMER pin to ground sets the restart time following overcurrent detection. Upon detection of an overcurrent condition, C_T is rapidly discharged to less than 1V and then recharged by a 14µA nominal current source back to the 2.9V timer threshold, whereupon the restart is attempted. Whenever TIMER pulls below 2.9V, the GATE pin pulls low to turn off the external switch. This cycle repeats until the overcurrent condition goes away and the switch restarts successfully. During normal operation the pin clamps at 3.5V nominal.

$\overline{\text{FAULT}}$ (Pin 3): The $\overline{\text{FAULT}}$ pin monitors the TIMER pin voltage and indicates the overcurrent condition. Whenever the TIMER pin is pulled below 3.3V at the onset of a current limit condition, the $\overline{\text{FAULT}}$ pin pulls active LOW. The $\overline{\text{FAULT}}$ pin resets HIGH immediately when the TIMER pin ramps above 3.4V during autorestart. The $\overline{\text{FAULT}}$ pin is an open-collector output, thus requiring an external pull-up resistor and is intended for logic interface. The resistor should be selected with a maximum of 1mA pull-up at low status.

IN (Pin 4): The IN pin threshold is TTL/CMOS compatible and has approximately 200mV of hysteresis. When the IN pin is pulled active HIGH above 2V, an internal charge pump is activated to pull up the GATE pin. The IN pin can be pulled as high as 15V regardless of whether the supply is on or off. If the IN pin is left open, an internal 75k pull-down resistor pulls the pin below 0.8V to ensure that the GATE pin is inactive LOW.

GATE (Pin 5): The GATE pin drives the power MOSFET gate. When the IN pin is greater than 2V, the GATE pin is pumped approximately 12V above the supply. It has relatively high impedance (the equivalence of a few hundred kΩ) when pumped above the rail. Care should be taken to minimize any loading by parasitic resistance to ground or supply. The GATE pin pulls LOW when the TIMER pin falls below 2.9V.

SENSE (Pin 6): The SENSE pin connects to the input of a supply-referenced comparator with a 65mV nominal offset. When the SENSE pin is taken more than 65mV below supply, the MOSFET gate is driven LOW and the timing capacitor is discharged. The SENSE pin threshold has a 0.33%/°C temperature coefficient (TC), which closely matches the TC of the drain-sense resistor formed from the copper trace of the PCB.

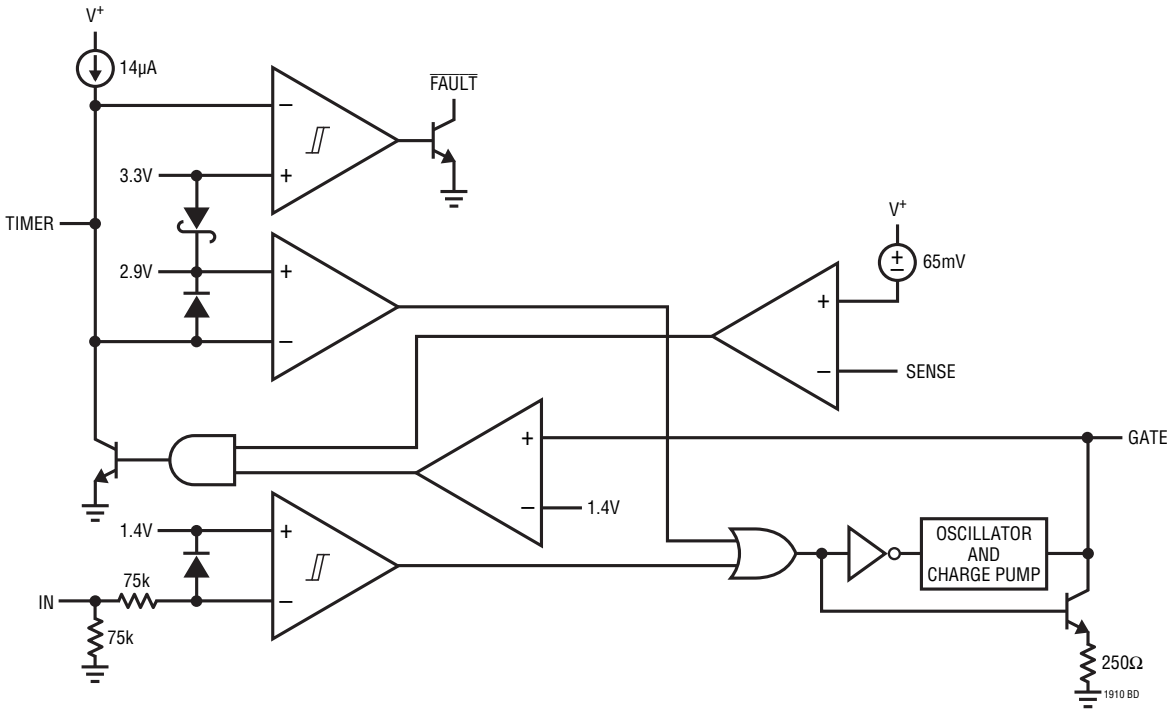
For loads requiring high inrush current, an RC timing delay can be added between the drain-sense resistor and the SENSE pin to ensure that the current-sense comparator

PIN FUNCTIONS

does not false trigger during start-up (see Applications Information). A maximum of 10kΩ can be inserted between a drain-sense resistor and the SENSE pin. If current sensing is not required, the SENSE pin is tied to supply.

V⁺ (Pin 8): In addition to providing the operating current for the LT1910, the V⁺ pin also serves as the Kelvin connection for the current-sense comparator. The V⁺ pin must be connected to the positive side of the drain-sense resistor for proper current-sensing operation.

BLOCK DIAGRAM



OPERATION (Refer to the Block Diagram)

The LT1910 GATE pin has two states, off and on. In the off state it is held LOW, while in the on state it is pumped to 12V above the supply by a self-contained 750kHz charge pump. The off state is activated when either the IN pin is below 0.8V or the TIMER pin is below 2.9V. Conversely, for the on state to be activated, the IN pin must be above 2V and the TIMER pin must be above 2.9V.

The IN pin has approximately 200mV of hysteresis. If it is left open, the IN pin is held LOW by a 75k resistor. Under normal conditions, the TIMER pin is held a diode drop above 2.9V by a 14µA pull-up current source. Thus the TIMER pin automatically reverts the GATE pin to the on state if the IN pin is above 2V.

The SENSE pin normally connects to the drain of the power MOSFET, which returns through a low value drain-sense resistor to supply. In order for the sense comparator to accurately sense the MOSFET drain current, the V⁺ pin must be connected directly to the positive side of the drain-sense resistor. When the GATE pin is on and the MOSFET drain current exceeds the level required to generate a 65mV drop across the drain-sense resistor, the sense comparator activates a pull-down NPN which rapidly pulls the TIMER pin below 2.9V. This in turn causes the timer comparator to override the IN pin and set the GATE pin to the off state, thus protecting the power MOSFET. When the TIMER pin is pulled below 3.3V, the fault comparator

OPERATION

also activates the open-collector NPN to pull the $\overline{\text{FAULT}}$ pin LOW, indicating an overcurrent condition.

When the MOSFET gate voltage is discharged to less than 1.4V, the TIMER pin is released. The 14µA current source then slowly charges the timing capacitor back to 2.9V where the charge pump again starts to drive the GATE pin HIGH. If a fault condition still exists, the sense comparator threshold will again be exceeded and the timer cycle will repeat until the fault is removed. The $\overline{\text{FAULT}}$ pin becomes inactive HIGH if the TIMER pin charges up successfully above 3.4V (see Figure 1).

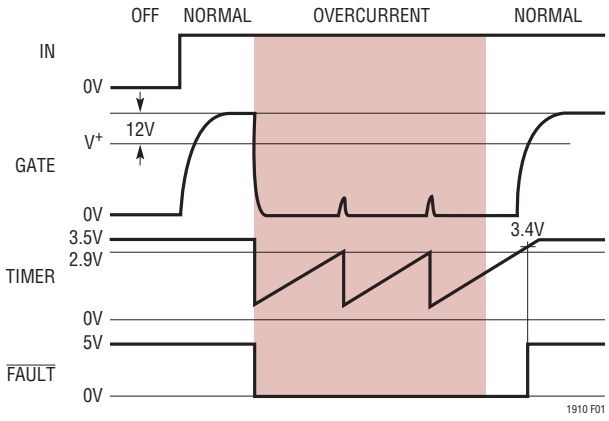


Figure 1. Timing Diagram

APPLICATIONS INFORMATION

Input/Supply Sequencing

There are no input/supply sequencing requirements for the LT1910. The IN pin may be taken up to 15V with the supply at 0V. When the supply is turned on with the IN pin set HIGH, the MOSFET turn-on will be inhibited until the timing capacitor charges up to 2.9V (i.e., for one restart cycle).

Isolating the Inputs

Operation in harsh environments may require isolation to prevent ground transients from damaging control logic. The LT1910 easily interfaces to low cost optoisolators. The network shown in Figure 2 ensures that the input will be pulled above 2V, but not exceed the absolute maximum rating for supply voltages of 12V to 48V over the entire temperature range. The optoisolator must have less than 20µA of dark current (leakage) at hot in order to maintain the off state (see Figure 2).

Drain-Sense Configuration

The LT1910 uses supply referenced current sensing. One input of the current-sense comparator is connected to a drain-sense pin, while the second input is offset 65mV below the supply inside the device. For this reason, Pin 8 of the LT1910 must be treated not only as a supply pin, but also as the reference input for the current-sense comparator.

Figure 3 shows the proper drain-sense configuration for the LT1910. Note that the SENSE pin goes to the drain end of the sense resistor, while the V+ pin is connected

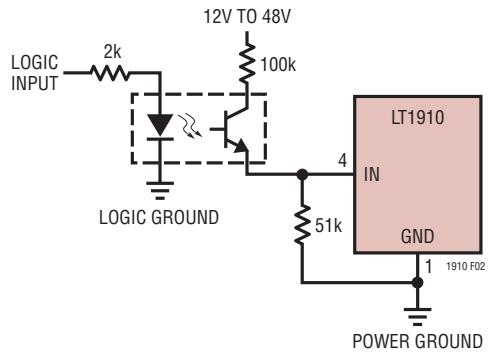


Figure 2. Isolating the Input

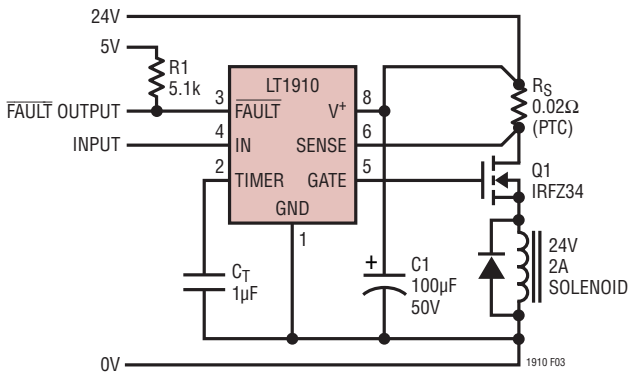


Figure 3. Drain-Sense Configuration

APPLICATIONS INFORMATION

to the supply at the same point as the positive end of the sense resistor.

The drain-sense threshold voltage has a positive temperature coefficient, allowing PTC sense resistors to be used (see Printed Circuit Board Shunts). The selection of R_S should be based on the minimum threshold voltage:

$$R_S = 50mV/I_{SET}$$

Thus the 0.02Ω drain-sense resistor in Figure 3 will yield a minimum trip current of 2.5A. This simple configuration is appropriate for resistive or inductive loads that do not generate large current transients at turn-on.

Automatic Restart Period

The timing capacitor, C_T, shown in Figure 3 determines the length of time the power MOSFET is held off following a current limit trip. Curves are given in the Typical Performance Characteristics to show the restart period for various values of C_T. For example, C_T = 0.33µF yields a 50ms restart period.

Defeating Automatic Restart

Some applications are required to remain off after a fault occurs. When the LT1910 is being driven from CMOS logic, this can be easily implemented by connecting resistor R2 between the IN and TIMER pins as shown in Figure 4. R2 supplies the sustaining current for an internal SCR which latches the TIMER pin LOW under a fault condition. The $\overline{FAULT}$ pin is set active LOW when the TIMER pin falls below 3.3V. This keeps the MOSFET gate from turning on and the $\overline{FAULT}$ pin from resetting HIGH until the IN pin has been recycled. C_T is used to prevent the $\overline{FAULT}$ pin from glitching whenever the IN pin recycles to turn on the MOSFET unsuccessfully under an existing fault condition.

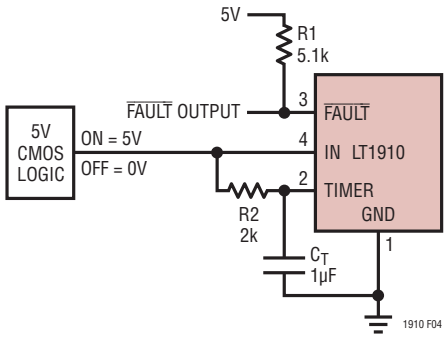


Figure 4. Latch-Off Configuration (Autorestart Defeated)

Inductive vs Capacitive Loads

Turning on an inductive load produces a relatively benign ramp in MOSFET current. However, when an inductive load is turned off, the current stored in the inductor needs somewhere to decay. A clamp diode connected directly across each inductive load normally serves this purpose. If a diode is not employed, the LT1910 clamps the MOSFET gate 0.7V below ground. This causes the MOSFET to resume conduction during the current decay with $(V^+ + V_{GS} + 0.7V)$ across it, resulting in high dissipation peaks.

Capacitive loads exhibit the opposite behavior. Any load that includes a decoupling capacitor will generate a current equal to $C_{LOAD} \bullet (\partial V/\partial t)$ during capacitor in-rush. With large electrolytic capacitors, the resulting current spike can play havoc with the power supply and false trip the current-sense comparator.

Turn-on ∂V/∂t is controlled by the addition of the simple network shown in Figure 5. This network takes advantage of the fact that the MOSFET acts as a source follower during turn-on. Thus the ∂V/∂t on the source can be controlled by controlling the ∂V/∂t on the gate.

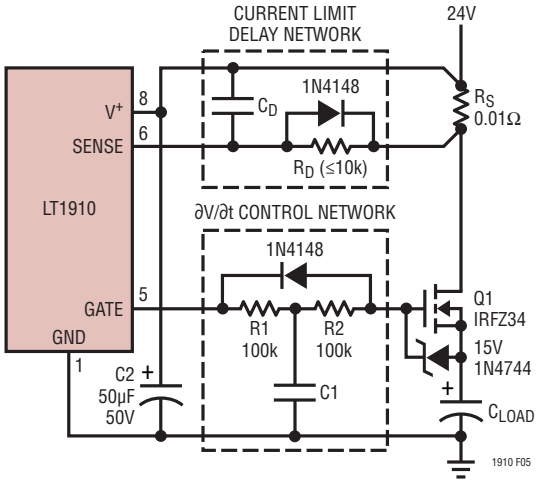


Figure 5. Control and Current Limit Delay

APPLICATIONS INFORMATION

The turn-on current spike into C_{LOAD} is estimated by:

$$I_{PEAK} = C_{LOAD} \bullet \frac{V_G - V_{TH}}{R1 \bullet C1}$$

where V_{TH} is the MOSFET gate threshold voltage. V_G is obtained by plotting the equation:

$$I_{GATE} = \frac{V_{GATE}}{R1}$$

on the graph of Gate Drive Current (I_{GATE}) vs Gate Voltage (V_{GATE}) as shown in Figure 6. The value of V_{GATE} at the intersection of the curves for a given supply is V_G. For example, if V^+ = 24V and R1 = 100k, then V_G = 18.3V. For V_{TH} = 2V, C1 = 0.1µF and C_{LOAD} = 1000µF, the estimated I_{PEAK} = 1.6A. The diode and the second resistor in the network ensure fast current limit turn-off.

When turning off a capacitive load, the source of the MOSFET can "hang up" if the load resistance does not discharge C_{LOAD} as fast as the gate is being pulled down. If this is the case, a 15V Zener may be added from gate to source to prevent $V_{GS(MAX)}$ from being exceeded.

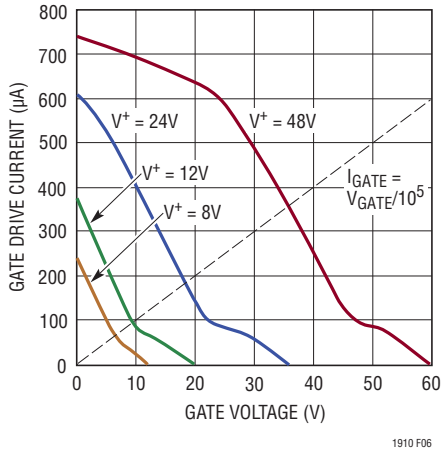


Figure 6. Gate Drive Current vs Gate Voltage

Adding Current Limit Delay

When capacitive loads are being switched or in very noisy environments, it is desirable to add delay in the drain current-sense path to prevent false tripping (inductive loads normally do not need delay). This is accomplished by the current limit delay network shown in Figure 5. R_D and C_D delay the overcurrent trip for drain currents up to approximately 10 • I_{SET}, above which the diode conducts and provides immediate turn-off (see Figure 7). To ensure proper operation of the timer, C_D must be ≤C_T.

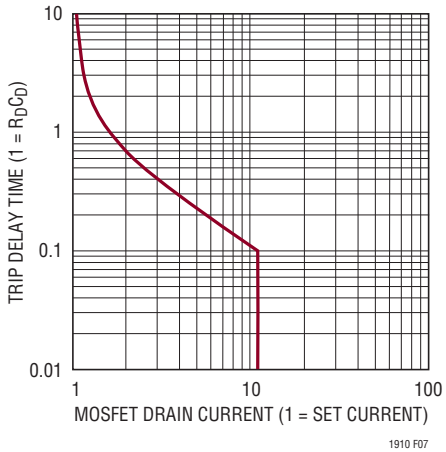


Figure 7. Current Limit Delay Time

Printed Circuit Board Shunts

The sheet resistance of 1oz copper clad is approximately 5 • $10^{-4}\Omega$/square with a temperature coefficient of 0.39%/°C. Since the LT1910 drain-sense threshold has a similar temperature coefficient (0.33%/°C), this offers the possibility of nearly zero TC current sensing using the "free" drain-sense resistor made out of PC trace material.

A conservative approach is to use 0.02" of width for each 1A of current for 1oz copper. Combining the LT1910 drain sense threshold with the 1oz copper resistance results in a simple expression for width and length:

Width (1oz Cu) = 0.02" • I_{SET}

Length (1oz Cu) = 2"

The width for 2oz copper would be halved while the length would remain the same.

Bends may be incorporated into the resistor to reduce space; each bend is equivalent to approximately 0.6 • the width of a straight length. Kelvin connection should be employed by running a separate trace from the ends of the resistor back to the LT1910's V^+ and SENSE pins. See Application Note 53 for further information on printed circuit board shunts.

APPLICATIONS INFORMATION

Low Voltage/Wide Supply Range Operation

When the supply is less than 12V, the LT1910's charge pump does not produce sufficient gate voltage to fully enhance the standard N-channel MOSFET. For these applications, a logic-level MOSFET can be used to extend the operating supply down to 8V. If the MOSFET has a maximum V_{GS} rating of 15V or greater, then the LT1910 can also operate up to a supply voltage of 60V (absolute maximum rating of the V^+ pin).

Protecting Against Supply Transients

The LT1910 is 100% tested and guaranteed to be safe from damage with 60V applied between the V^+ and GND pins. However, when this voltage is exceeded, even for a few microseconds, the result can be catastrophic. For this reason it is imperative that the LT1910 is not exposed to supply transients above 60V. A transient suppressor, such as Diodes Inc.'s SMAJ48A, should be added between the V^+ and GND pins for such applications.

For proper current sense operation, the V^+ pin is required to be connected to the positive side of the drain-sense resistor (see Drain-Sense Configuration). Therefore, the supply should be adequately decoupled at the node where the V^+ pin and drain sense resistor meet. Several hundred microfarads may be required when operating with a high current switch.

When the operating voltage approaches the 60V absolute maximum rating of the LT1910, local supply decoupling between the V^+ and GND pins is highly recommended. An RC snubber with a transient suppressor are an absolute necessity. Note however that resistance should not be added in series with the V^+ pin because it will cause an error in the current-sense threshold.

Low Side Driving

Although the LT1910 is primarily targeted at high side (grounded load) switch applications, it can also be used for low side (supply connected load) switch applications. Figures 8a and 8b illustrate the LT1910 driving low side power MOSFETs. Because the LT1910 charge pump tries to pump the gate of the N-channel MOSFET above the supply, a clamp Zener is required to prevent the V_{GS} (absolute maximum) of the MOSFET from being exceeded. The LT1910 gate drive is current limited for this purpose so that no resistance is needed between the GATE pin and Zener.

Current sensing for protecting low side drivers can be done in several ways. In the Figure 8a circuit, the supply voltage for the load is assumed to be within the supply operating range of the LT1910. This allows the load to be returned to supply through current-sense resistor, R_S, providing normal operation of the LT1910 protection circuitry.

If the load cannot be returned to supply through R_S, or the load supply voltage is higher than the LT1910 supply, the current sense must be moved to the source of the low side MOSFET.

Figure 8b shows an approach to source sensing. An operational amplifier (must common mode to ground) is used to level shift the voltage across R_S up to the drain-sense pin. This approach allows the use of a small sense resistor which could be made from PC trace material. The LT1910 restart timer functions the same as in the high side switch application.

APPLICATIONS INFORMATION

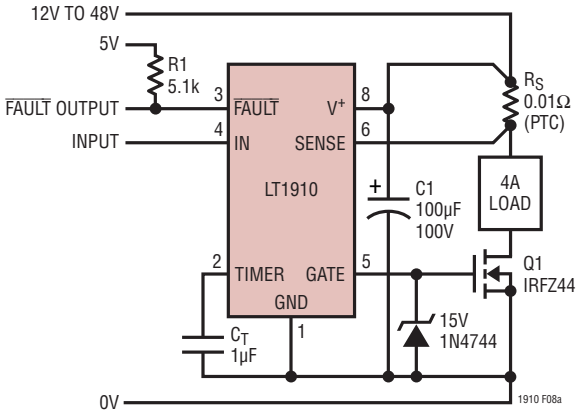


Figure 8a. Low Side Driver with Load Current Sensing

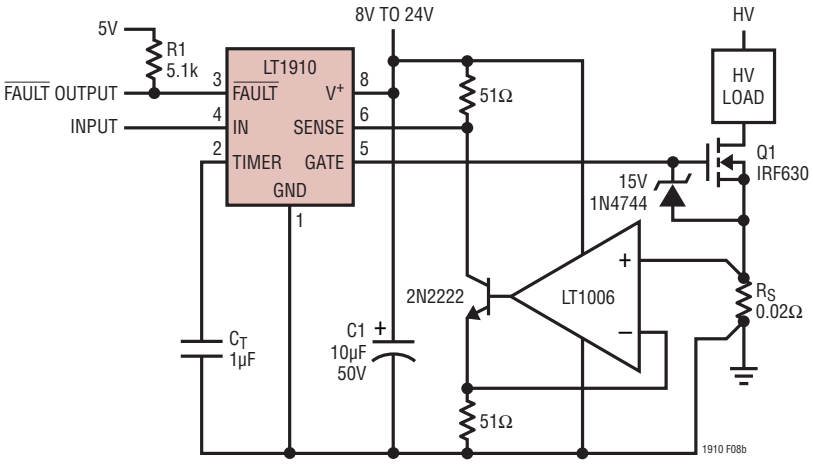
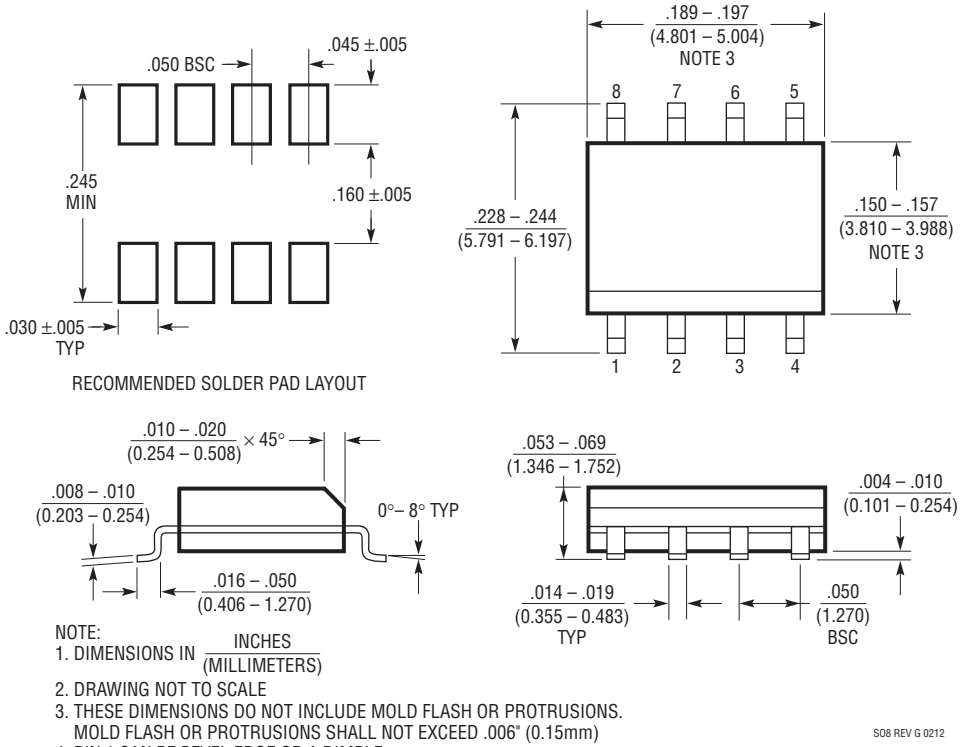


Figure 8b. Low Side Driver for Source Current Sensing

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

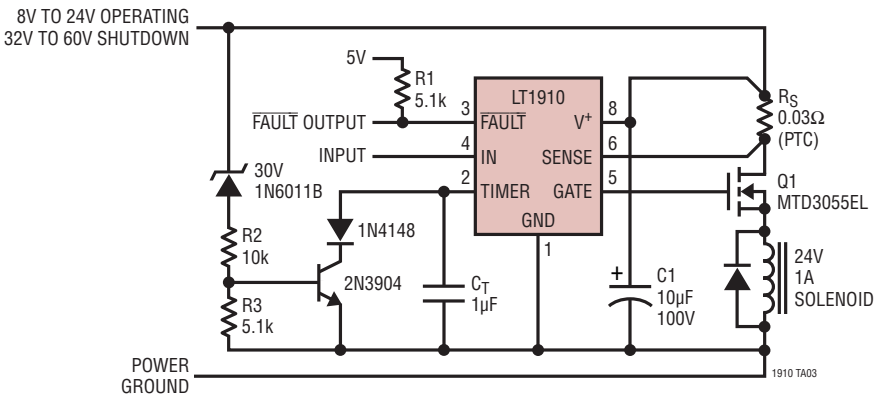
S08 REV G 0212

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	7/14	Updated $\overline{\text{FAULT}}$ pin description	5
C	6/15	Changed top mark	2

TYPICAL APPLICATION

Protected 1A Automotive Solenoid Driver with Overvoltage Shutdown



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1153	Autoreset Electronic Circuit Breaker	Programmable Trip Current, Fault Status Output
LTC1155	Dual High Side Micropower MOSFET Driver	Operates from 4.5V to 18V, 85µA On Current, Short-Circuit Protection
LT1161	Quad Protected High Side MOSFET Driver	8V to 48V Supply Range, Individual Short-Circuit Protection
LTC1163	Triple 1.8V to 6V High Side MOSFET Driver	0.01µA Standby Current, Triple Driver in SO-8 Package
LTC1255	Dual 24V High Side MOSFET Driver	Operates from 9V to 24V, Short-Circuit Protection
LTC1477	Protected Monolithic High Side Switch	Low $R_{DS(ON)}$ 0.07Ω Switch, 2A Short-Circuit Protected
LTC1623	SMBus Dual High Side Switch Controller	2-Wire SMBus Serial Interface, Built-In Gate Charge Pumps
LTC1693 Family	High Speed Single/Dual N-Channel/P-Channel MOSFET Drivers	1.5A Peak Output Current, 4.5V ≤ V_{CC} ≤ 13.2V, SO-8 Package
LTC1710	SMBus Dual Monolithic High Side Switch	Two Low $R_{DS(ON)}$ 0.4Ω/300mA Switches in 8-Lead MSOP Package
LTC4412	Low Loss PowerPath™ Controller	Implements “Ideal Diode” Function, ThinSOT™ Package

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