LP62S1664C Series

64K X 16 BIT LOW VOLTAGE CMOS SRAM

Features

- Operating voltage: 2.7V to 3.6V
- Access times: 45/55/70 ns (max.)
- Current:
  - LP62S1664C-45 series: Operating: 50mA (max.)
    Standby: 5μA (max.)
  - LP62S1664C-55 series: Operating: 50mA (max.)
    Standby: 5μA (max.)
  - LP62S1664C-70 series: Operating: 40mA (max.)
    Standby: 5μA (max.)
- Extended operating temperature range : -40°C to 85°C for -LLI series
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2V (min.)
- Available in 44-pin TSOP and 48-ball Mini BGA (6X8) packages.

General Description

The LP62S1664C is a low operating current 1,048,576-bit static random access memory organized as 65,536 words by 16 bits and operates on low power supply voltage from 2.7V to 3.6V. It is built using AMIC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

The chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.

Data retention is guaranteed at a power supply voltage as low as 2V.

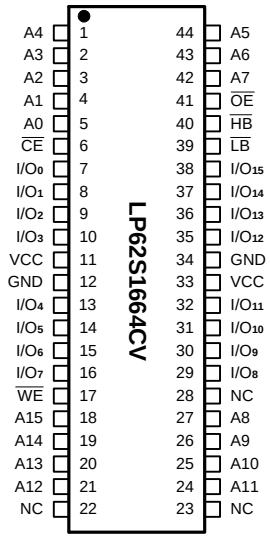
Product Family

Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I_{CCDR}, Typ.)	Standby (I_{SB1}, Typ.)	Operating (I_{CC2}, Typ.)	
LP62S1664C	-40°C ~ +85°C	2.7V~3.6V	45ns / 55ns / 70ns	0.2μA	0.3μA	3mA	44L TSOP 48B MBGA

1. Typical values are measured at VCC = 3.0V, T_A = 25°C and not 100% tested.
2. Data retention current VCC = 2.0V.

Pin Configuration

■ **TSOP (Type II)**



■ **Mini BGA (6X8) Top View**

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O_8	$\overline{HB}$	A3	A4	$\overline{CS}$	I/O_0
C	I/O_9	I/O_{10}	A5	A6	I/O_1	I/O_2
D	VSS	I/O_{11}	NC	A7	I/O_3	VCC
E	VCC	I/O_{12}	NC	NC	I/O_4	VSS
F	I/O_{14}	I/O_{13}	A14	A15	I/O_5	I/O_6
G	I/O_{15}	NC	A12	A13	$\overline{WE}$	I/O_7
H	NC	A8	A9	A10	A11	NC

LP62S1664CU

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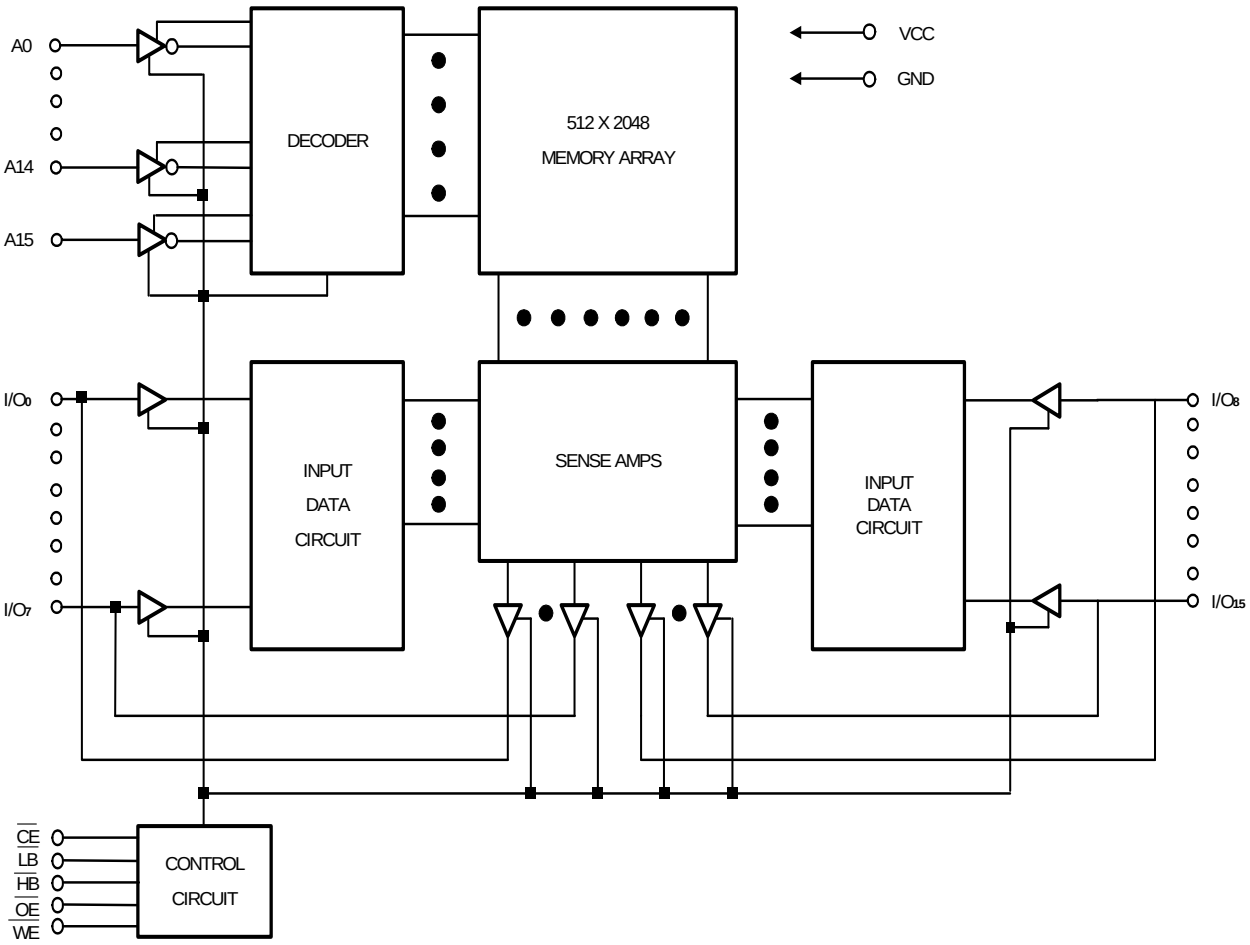
Block Diagram



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Pin Description - TSOP

Pin No.	Symbol	Description
1 - 5, 18 - 21, 24 - 27,42 - 44	A0 - A15	Address Inputs
6	$\overline{CE}$	Chip Enable Input
7 - 10, 13 - 16, 29 - 32, 35 - 38	I/O_0 - I/O_{15}	Data Input/Outputs
17	$\overline{WE}$	Write Enable Input
39	$\overline{LB}$	Byte Enable Input (I/O_0 to I/O_7)
40	$\overline{HB}$	Byte Enable Input (I/O_8 to I/O_{15})
41	$\overline{OE}$	Output Enable Input
11, 33	VCC	Power
12, 34	GND	Ground
22 , 23, 28	NC	No Connection

Recommended DC Operating Conditions

(T_A = -25°C to + 85°C for –LLT or -40°C to 85°C for -LLI)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3.0	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	+0.6	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

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Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +4.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . -40°C to +85°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = -25°C to + 85°C for -LLT or -40°C to + 85°C for -LLI, VCC = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	LP62S1664C-45LLT/LLI		LP62S1664C-55LLT/LLI		LP62S1664C-70LLT/LLI		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	-	1	-	1	-	1	µA	V_{IN} = GND to VCC
$\|I_{LO}\|$	Output Leakage Current	-	1	-	1	-	1	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{LB}$ = $\overline{HB}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	-	5	-	5	-	5	mA	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{CC1}	Dynamic Operating Current	-	50	-	50	-	40	mA	Min. Cycle, Duty = 100% $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{CC2}		-	5	-	5	-	5	mA	$\overline{CE}$ = V_{IL}, V_{IH} = VCC, V_{IL} = 0V, f = 1MHz, $I_{I/O}$ = 0 mA
I_{SB}	Standby Power Supply Current	-	0.3	-	0.3	-	0.3	mA	$\overline{CE}$ = V_{IH}
I_{SB1}		-	5	-	5	-	5	µA	$\overline{CE}$ ≥ VCC - 0.2V V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	-	0.4	-	0.4	-	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.2	-	2.2	-	2.2	-	V	I_{OH} = -1.0mA

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Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O_0 to I/O_7 Mode	I/O_8 to I/O_{15} Mode	VCC Current
H	X	X	X	X	Not selected	Not selected	I_{SB1}, I_{SB}
L	L	H	L	L	Read	Read	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Read	High - Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	High - Z	Read	I_{CC1}, I_{CC2}, I_{CC}
L	X	L	L	L	Write	Write	I_{CC1}, I_{CC2}, I_{CC}
			L	H	Write	Not Write/Hi - Z	I_{CC1}, I_{CC2}, I_{CC}
			H	L	Not Write/Hi - Z	Write	I_{CC1}, I_{CC2}, I_{CC}
L	H	H	L	X	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
			X	L	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
X	X	X	H	H	Not selected	Not selected	I_{SB1}, I_{SB}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance	-	6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance	-	8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

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AC Characteristics (T_A = -25°C to +85°C for -LLT or -40°C to +85°C for -LLI, VCC = 2.7V to 3.6V)

Symbol	Parameter	LP62S1664C-45LLT/LLI		LP62S1664C-55LLT/LLI		LP62S1664C-70LLT/LLI		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	45	-	55	-	70	-	ns
t_{AA}	Address Access Time	-	45	-	55	-	70	ns
t_{ACE}	Chip Enable Access Time	-	45	-	55	-	70	ns
t_{BE}	Byte Enable Access Time	-	45	-	55	-	70	ns
t_{OE}	Output Enable to Output Valid	-	20	-	30	-	35	ns
t_{CLZ}	Chip Enable to Output in Low Z	5	-	10	-	10	-	ns
t_{BLZ}	Byte Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
t_{CHZ}	Chip Disable to Output in High Z	-	15	-	20	-	25	ns
t_{BHZ}	Byte Disable to Output in High Z	-	15	-	20	-	25	ns
t_{OHZ}	Output Disable to Output in High Z	-	15	-	20	-	25	ns
t_{OH}	Output Hold from Address Change	5	-	5	-	10	-	ns
Write Cycle								
t_{WC}	Write Cycle Time	45	-	55	-	70	-	ns
t_{CW}	Chip Enable to End of Write	35	-	50	-	60	-	ns
t_{BW}	Byte Enable to End of Write	35	-	50	-	60	-	ns
t_{AS}	Address Setup Time	0	-	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	35	-	50	-	60	-	ns
t_{WP}	Write Pulse Width	35	-	40	-	50	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	-	20	-	25	-	30	ns
t_{DW}	Data to Write Time Overlap	20	-	25	-	30	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{OW}	Output Active from End of Write	5	-	5	-	5	-	ns

Note: t_{CHZ}, t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

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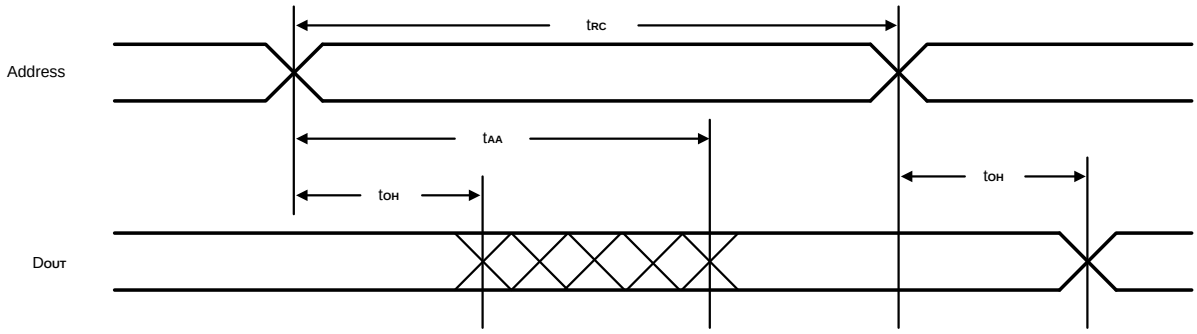
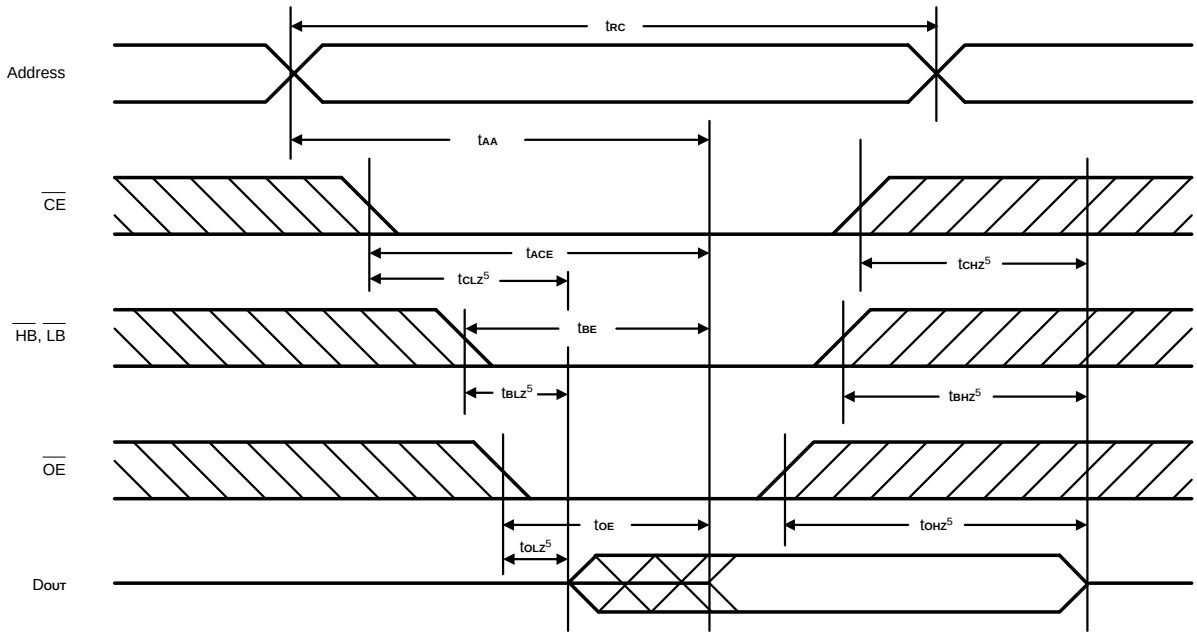
Timing Waveforms

Read Cycle 1[1, 2, 4]



Read Cycle 2[1, 2, 3]



Notes:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE}$ = V_{IL}, $\overline{HB}$ = V_{IL} and, or $\overline{LB}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

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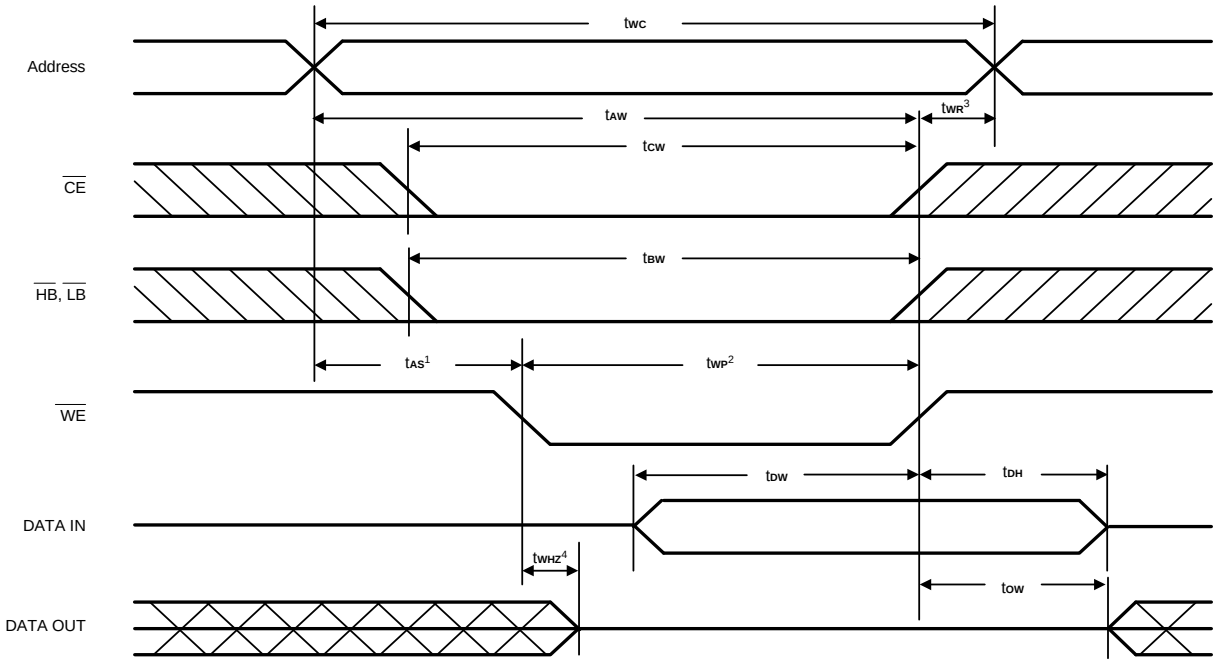
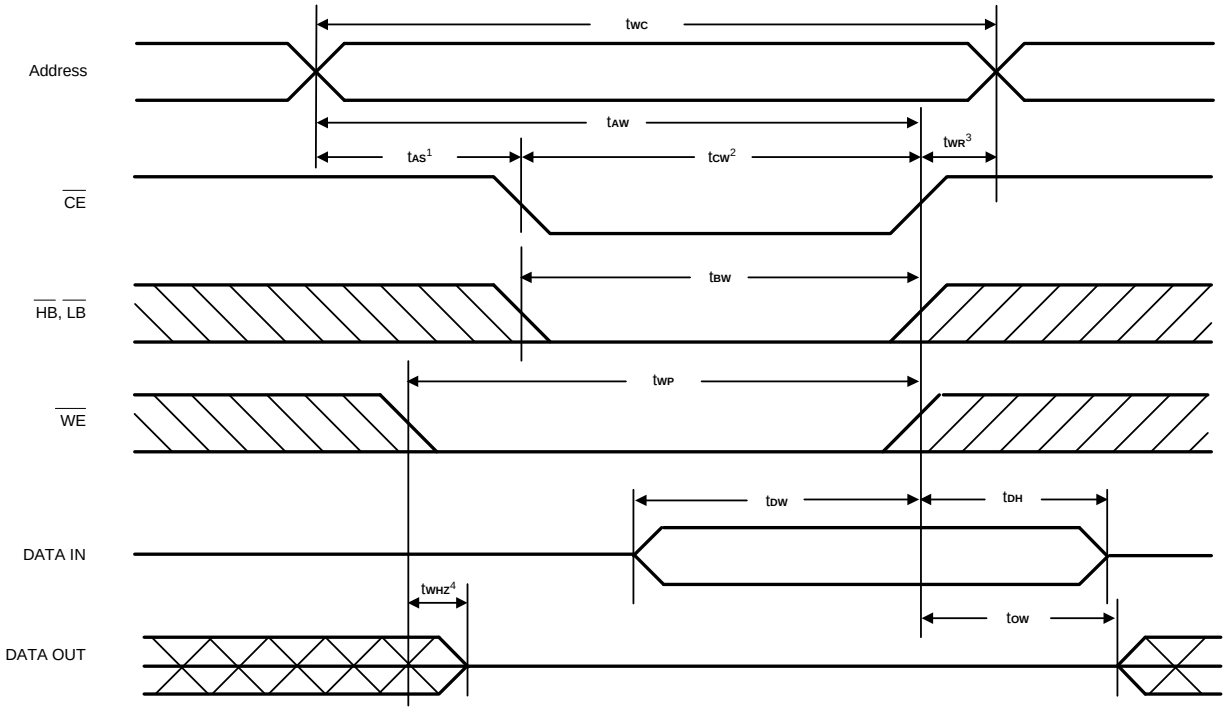
Timing Waveforms (continued)

Write Cycle 1
(Write Enable Controlled)



Write Cycle 2
(Chip Enable Controlled)



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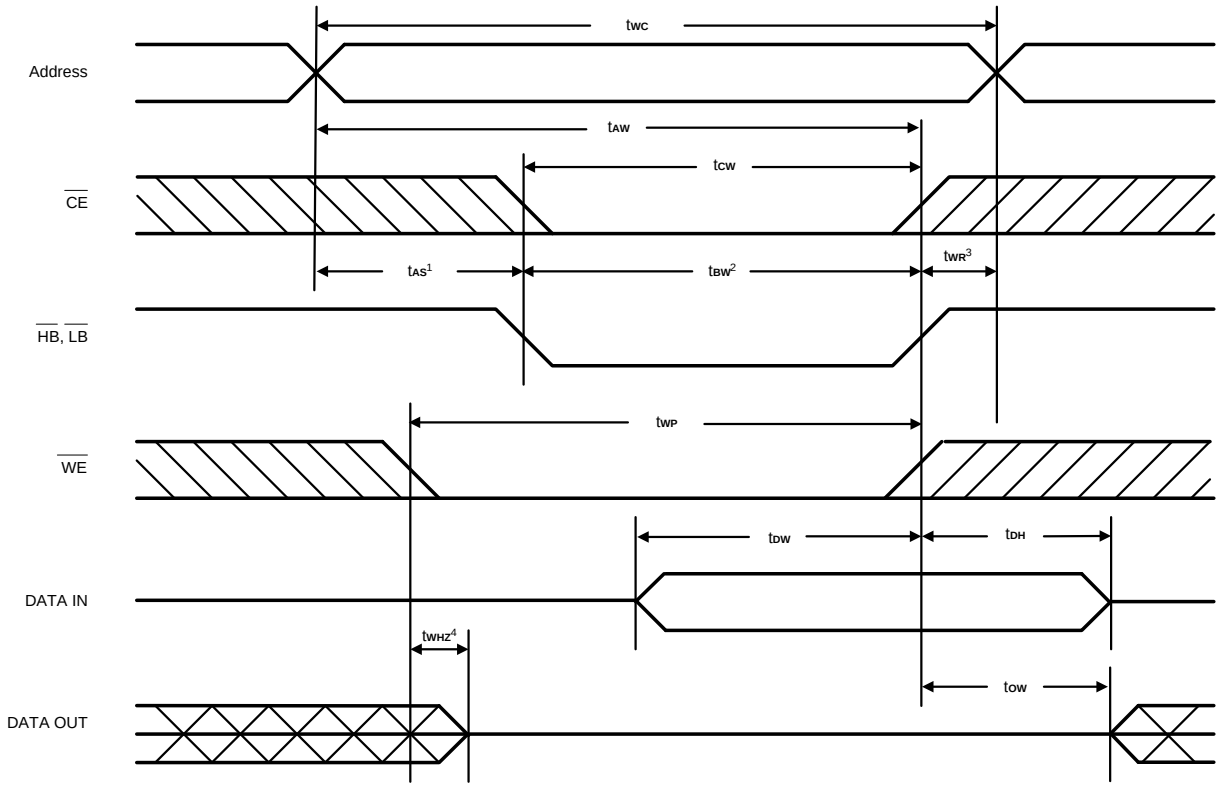
Timing Waveforms (continued)

Write Cycle 3
(Byte Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}, t_{BW}) of a low $\overline{CE}$, $\overline{WE}$ and ($\overline{HB}$ and, or $\overline{LB}$).
3. t_{WR} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ or ($\overline{HB}$ and, or $\overline{LB}$) going high to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

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AC Test Conditions

Input Pulse Levels	0V to 2.4V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

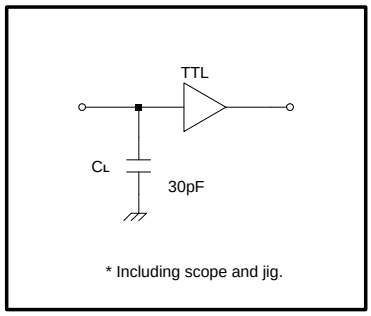

Figure 1. Output Load

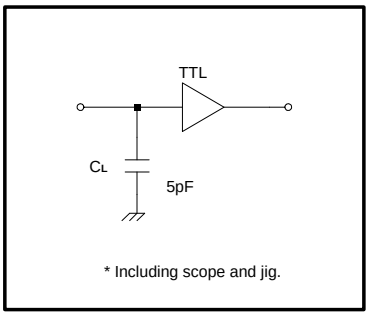

Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (TA = -25°C to 85°C for –LLT or -40°C to 85°C for -LLI)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	2.0	3.6	V	$\overline{CE} \geq$ VCC - 0.2V
I_{CCDR}	Data Retention Current	-	3*	µA	VCC = 2.0V, $\overline{CE} \geq$ VCC - 0.2V $V_{IN} \geq$ 0V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}	-	ns	
t_{VR}	VCC Rise Time from Data Retention Voltage to Operating Voltage	5	-	ms	

* LP62S1664C-45/55/70(LLT/LLI) I_{CCDR}: max. 1µA at T_A = 0°C to + 40°C

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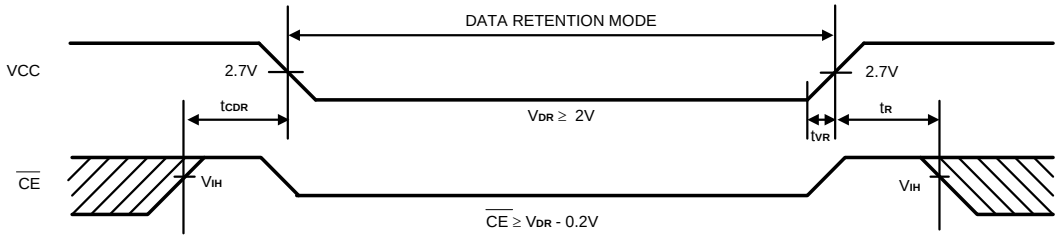
Low VCC Data Retention Waveform



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Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (μA)	Package
LP62S1664CV-45LLIF	45	50	5	44L Pb-Free TSOP
LP62S1664CU-45LLIF				48B Pb-Free Mini BGA
LP62S1664CV-55LLT	55	50	5	44L TSOP
LP62S1664CV-55LLTF				44L Pb-Free TSOP
LP62S1664CV-55LLI				44L TSOP
LP62S1664CV-55LLIF				44L Pb-Free TSOP
LP62S1664CU-55LLT				48B Mini BGA
LP62S1664CU-55LLTF				48B Pb-Free Mini BGA
LP62S1664CU-55LLI				48B Mini BGA
LP62S1664CU-55LLIF				48B Pb-Free Mini BGA
LP62S1664CV-70LLT	70	40	5	44L TSOP
LP62S1664CV-70LLTF				44L Pb-Free TSOP
LP62S1664CV-70LLI				44L TSOP
LP62S1664CV-70LLIF				44L Pb-Free TSOP
LP62S1664CU-70LLT				48B Mini BGA
LP62S1664CU-70LLTF				48B Pb-Free Mini BGA
LP62S1664CU-70LLI				48B Mini BGA
LP62S1664CU-70LLIF				48B Pb-Free Mini BGA

LLT : for -25°C ~ 85°C
LLI : for -40°C ~ 85°C

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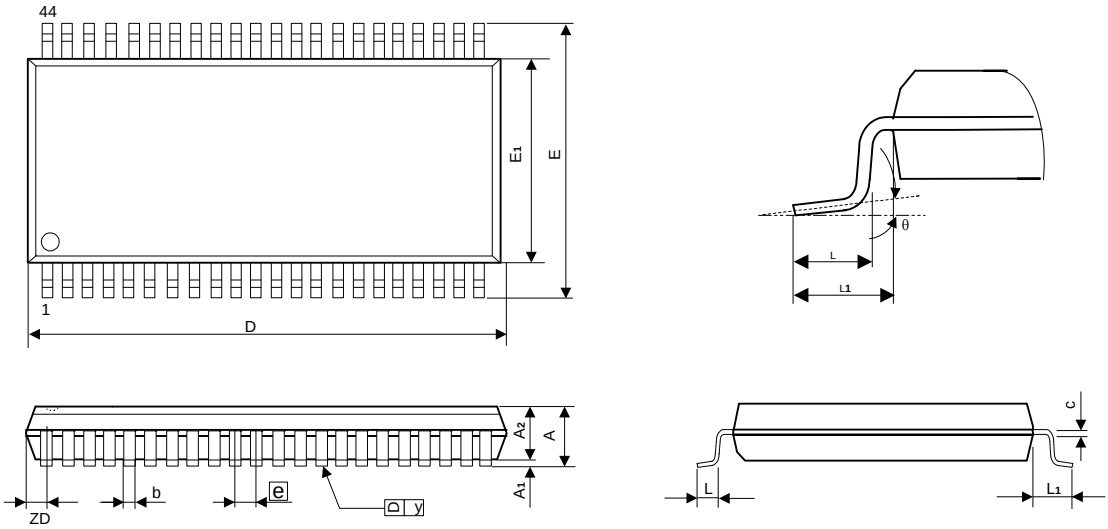
Package Information

TSOP 44L (Type II) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.012	-	0.018	0.30	-	0.45
c	0.005	-	0.008	0.12	-	0.21
D	0.720	0.725	0.730	18.28	18.41	18.54
ZD	0.032 REF			0.805 REF		
E	0.455	0.463	0.471	11.56	11.76	11.96
E_1	0.395	0.400	0.405	10.03	10.16	10.29
L	0.019	0.023	0.027	0.49	0.59	0.69
L_1	0.031 REF			0.80 REF		
e	0.031 BSC			0.80 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension ZD includes end flash.

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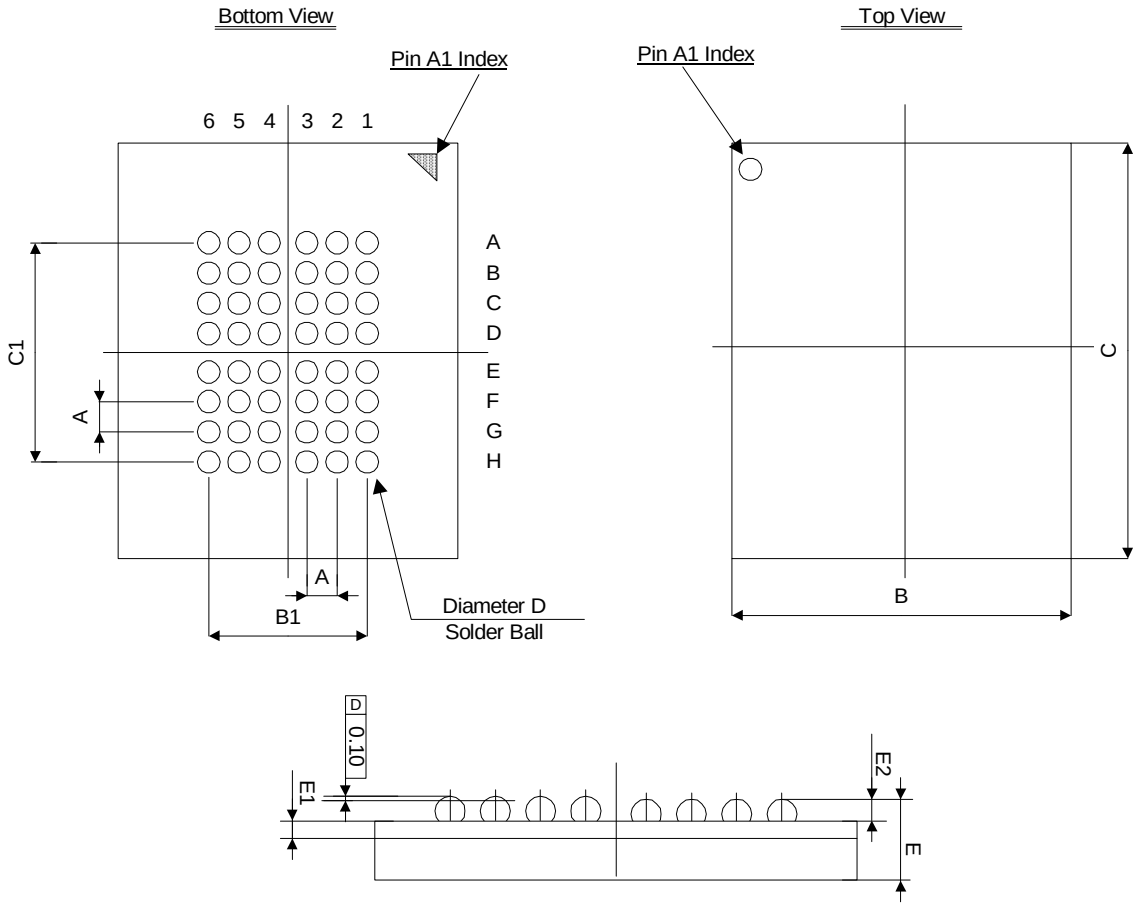
Package Information

Mini BGA 6X8 (48 BALLS) Outline Dimensions unit : millimeter(mm)



Symbol	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.10	1.20
E1	-	0.36	-
E2	-	0.25	-

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