2.2 Outputs various information to make system configuration easy

- Outputs DTS-CD/LD detection flag by DTS sync signal detection.
- Outputs burst preamble Pc from microcontroller interface.
- Calculates sampling frequency of input signal and outputs it from microcontroller interface.
- Outputs interrupt signal for microcontroller (interrupt source can be selected).
- Outputs signal of transitional period switching between VCO clock and oscillation amplifier clock.
- Outputs bit 1 of channel status (non-PCM data detection bit).
- Outputs emphasis information of channel status.
- Outputs renewed flag of the first 48 bits channel status.
- Channel status bit, validity flag and user data output are selectable.
- Outputs modulation/demodulation preamble B information.
- Possible to carry out and output various settings through microcontroller interface.

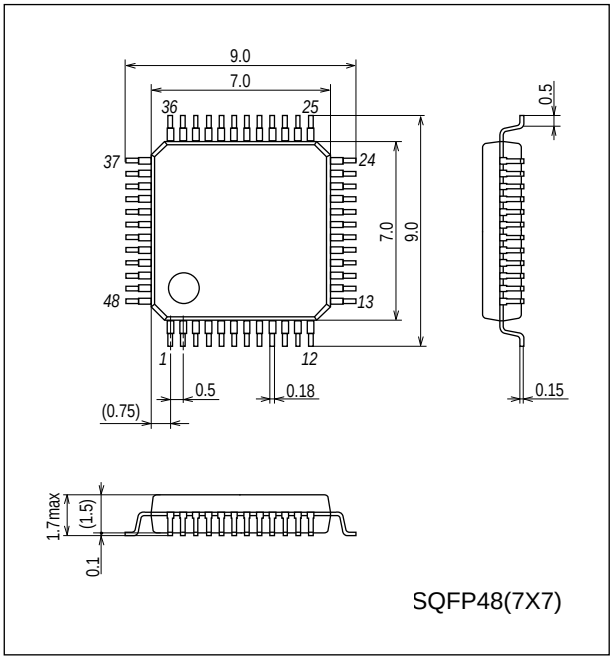
2.3 Plenty of built-in functions to reduce peripheral circuits

- Includes modulation function that can attach channel status, validity flag, and user data.
- Equipped with a total of 7 digital data input pins: 1 input pin with an amplifier and 6 input pins with 5V tolerable TTL level signal.
- Possible to monitor input pin status with microcontroller by mounting a bi-phase input data detection function.
- Possible to select input data among 8 system input data including modulation function output.
- Possible to select output of input-data through among 8 system input data aside from selecting demodulation data.
- Includes 2 system bit clock and LR clock outputs. Various frequency-dividing ratios can be set to one of these two systems.
- Equipped with a serial digital audio data input pin. Possible to switch with demodulation output.
- Possible to modulate the data that is input to the serial digital audio data input pin.
- Includes built-in oscillation amplifier and frequency divider for quartz resonator and also possible to use them as clock generator.
- Includes 4 bits general-purpose parallel I/O port. It can be used for interface with peripheral ICs.
- All the channel status can be decoded through peripheral circuit using preamble B information.
- A continuous switching operation between external clock synchronous mode and PLL clock synchronous mode is possible.
- Single 3.3V-power supply operation. TTL input port supports 5V interface.
- Adopts small SQFP48 package for efficient use of substrate mounting area.

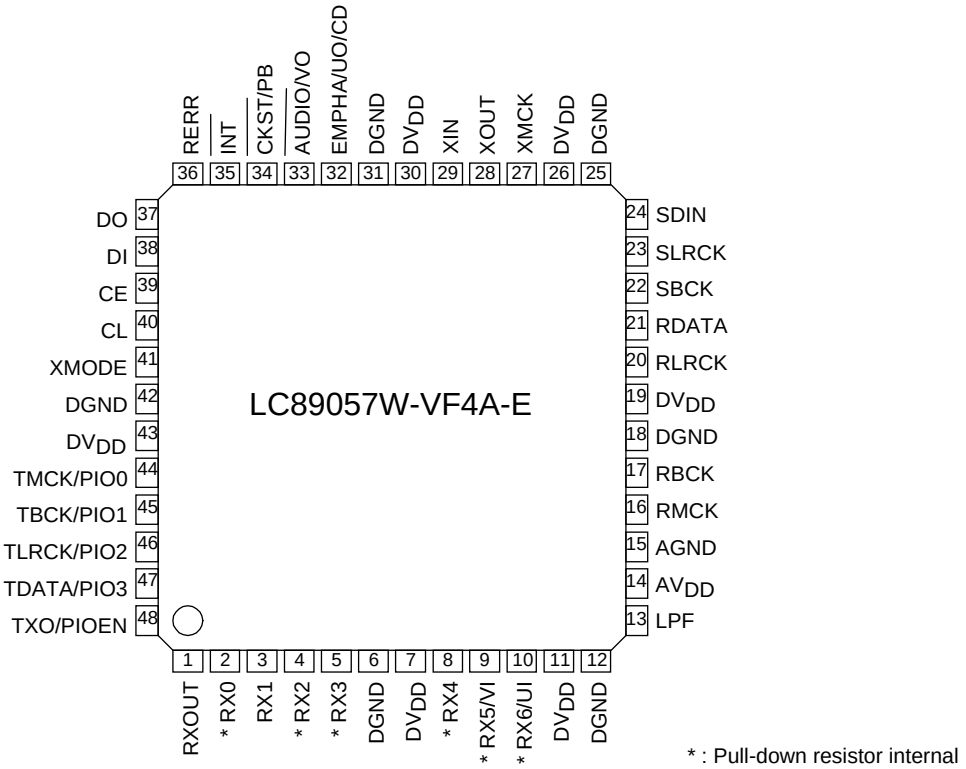
Package Dimensions

unit : mm (typ)

3163B



4. Pin Assignment



* : Pull-down resistor internal

Top view

5. Pin Functions

Table 5.1 Pin Functions

Pin No.	Name	I/O	Function
1	RXOUT	O	Output pin of Input bi-phase selection data
2	RX0	I_5	Input pin of TTL-compatible digital data
3	RX1	I	Digital data input pin with built-in amplifier that supports coaxial
4	RX2	I_5	Input pin of TTL-compatible digital data
5	RX3	I_5	Input pin of TTL-compatible digital data
6	DGND		Digital GND
7	DV_{DD}		Digital power supply
8	RX4	I_5	Input pin of TTL-compatible digital data
9	RX5/VI	I_5	TTL-compatible digital data || Validity flag input pin for modulation
10	RX6/UI	I_5	TTL-compatible digital data || User data input pin for modulation
11	DV_{DD}		Digital power supply for PLL
12	DGND		Digital GND for PLL
13	LPF	O	PLL loop filter connection pin
14	AV_{DD}		Analog power supply for PLL
15	AGND		Analog GND for PLL
16	RMCK	O	R system clock output pin (256fs, 512fs, XIN, VCO)
17	RBCK	O/I	R system bit clock input/output pin (64fs)
18	DGND		Digital GND
19	DV_{DD}		Digital power supply
20	RLRCK	O/I	R system LR clock input/output pin (fs)
21	RDATA	O	Output pin of serial audio data
22	SBCK	O	S system bit clock output pin (32fs, 64fs, 128fs)
23	SLRCK	O	S system LR clock output pin (fs/2, fs, 2fs)
24	SDIN	I_5	Input pin of serial audio data

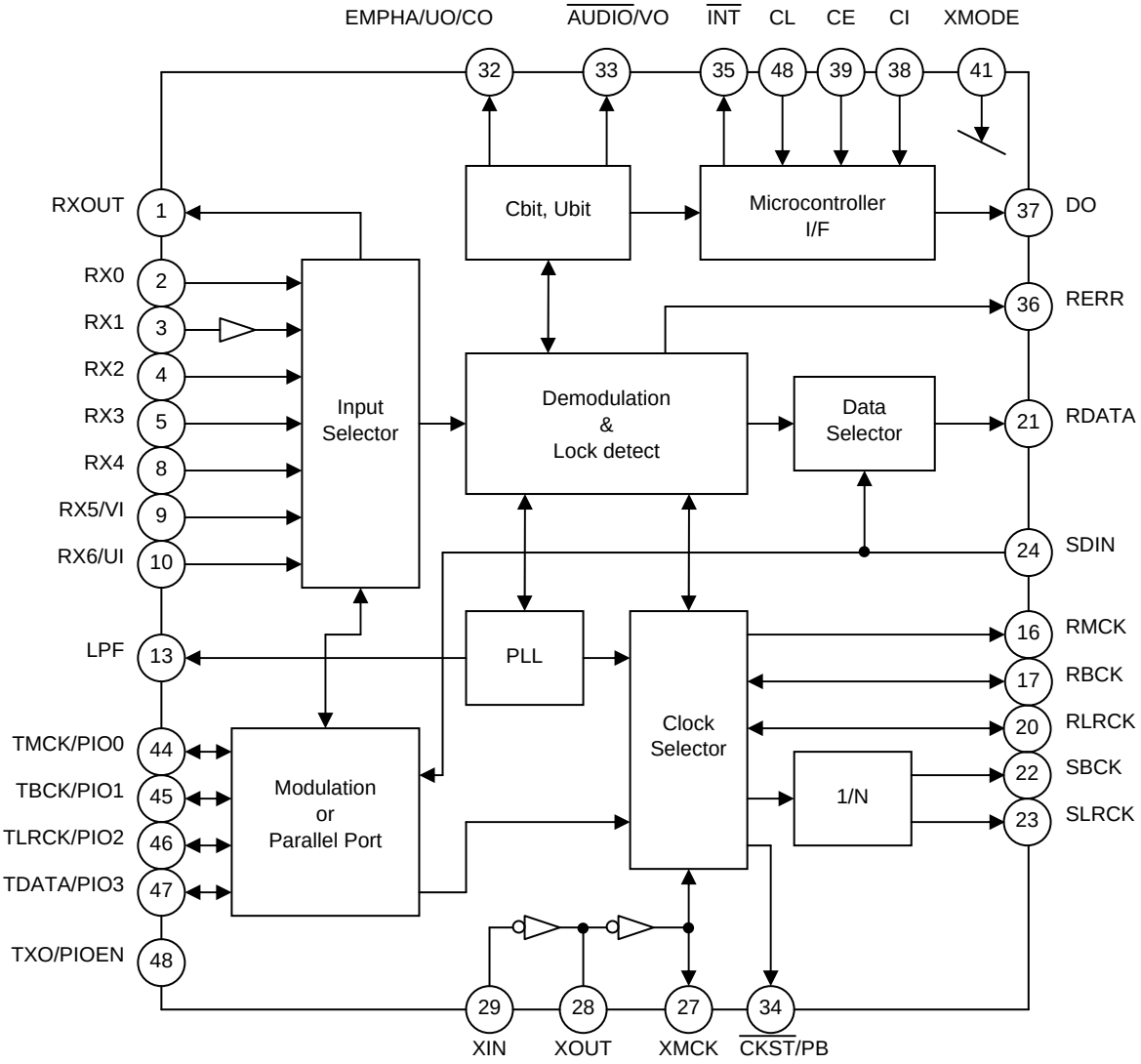
Continued on next page.

Continued from preceding page.

Pin No.	Name	I/O	Function
25	DGND		Digital GND
26	DV_{DD}		Digital power supply
27	XMCK	O	Oscillation amplifier output pin
28	XOUT	O	Quartz resonator connection output pin
29	XIN	I	Quartz resonator connection, input pin of external supply clock (24.576MHz or 12.288MHz)
30	DV_{DD}		Digital power supply
31	DGND		Digital GND
32	EMPHA/UO/CO	I/O	Emphasis information || U data output || C data output || Chip address setting pin
33	$\overline{\text{AUDIO}}$/VO	I/O	Non-PCM detection || V flag output || Chip address setting pin
34	$\overline{\text{CKST}}$/PB	I/O	Output of clock switch transitional period signal || Preamble B output || Demodulation master or slave function switch pin
35	$\overline{\text{INT}}$	I/O	Interrupt output for Microcontroller (Possible to select an interrupt factor.) || Modulation or general-purpose I/O switch pin
36	RERR	O	PLL clock error, data error flag output
37	DO	O	Microcontroller I/F, read data output pin (3-state)
38	DI	I_5	Microcontroller I/F, write data input pin
39	CE	I_5	Microcontroller I/F, chip enable input pin
40	CL	I_5	Microcontroller I/F, clock input pin
41	XMODE	I_5	System reset input pin
42	DGND		Digital GND
43	DV_{DD}		Digital power supply
44	TMCK/PIO0	I/O	256fs or 128fs system clock input for modulation || 256fs or 512fs system clock input for external clock sync function || General-purpose I/O pin
45	TBCK/PIO1	I/O	64fs bit clock input for modulation || General-purpose I/O pin
46	TLRCK/PIO2	I/O	fs clock input for modulation || General-purpose I/O pin
47	TDATA/PIO3	I/O	serial audio data input for modulation || General-purpose I/O pin
48	TXO/PIOEN	O/I	Modulation data output || General-purpose I/O enable input pin

1) Withstand voltage input/output: I or O = -0.3 to 3.6V, I_5 = -0.3 to 5.5V
2) Pins 32 and 33 are input pins for chip address setting, when pin 41 = "L".
3) Pin 34 is a demodulation function master or an input pin for slave setting, when pin 41 = "L".
4) Pin 35 is a modulation function or an input pin for general-purpose I/O function switch setting, when pin 41 = "L".
5) ON/OFF for all power supplies must be done at the same timing as a latch-up countermeasure.

6. Block Diagram



7. Comparison between LC89057W-VF4 and LC89057W-VF4A

Table 7.1 Difference between LC89057W-VF4 and LC89057W-VF4A

Item	LC89057W-VF4	LC89057W-VF4A
DIR function: External synchronization mode	256fs clock input	256fs or 512fs clock input
DIR function: Setting of RERR wait time after PLL is locked	After preamble B is counted 6. After preamble B is counted 12. After preamble B is counted 24. After preamble B is counted 48.	After preamble B is counted 3. After preamble B is counted 6. After preamble B is counted 12. After preamble B is counted 24.
DIR function: Setting of clock wait time after PLL is unlocked	50µs from when oscillation amplifier starts 100µs from when oscillation amplifier starts 200µs from when oscillation amplifier starts 400µs from when oscillation amplifier starts	0µs from when oscillation amplifier starts 50µs from when oscillation amplifier starts 100µs from when oscillation amplifier starts 200µs from when oscillation amplifier starts
DIR function: Channel status bit output	Microcontroller read out	Microcontroller read out or terminal output (full decode processing possible)
DIR function: Preamble B info output	×	○
DIT function: System clock	256fs clock input	256fs or 128fs clock input
DIT function: Preamble B info output	×	○

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 8.1: Absolute Maximum Ratings at AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	AV_{DD} max	8-1-1	-0.3 to +4.6	V
Maximum supply voltage	DV_{DD} max	8-1-2	-0.3 to +4.6	V
Input voltage 1	$V_{IN}1$	8-1-3	-0.3 to +3.9	V
Input voltage 2	$V_{IN}2$	8-1-4	-0.3 to +5.8	V
Output voltage	V_{OUT}	8-1-5	-0.3 to +3.9	V
Storage ambient temperature	Tstg		-55 to +125	°C
Operating ambient temperature	Topr		-30 to +70	°C
Maximum input/output current	I_{IN}, I_{OUT}	8-1-6	±20	mA

8-1-1: AV_{DD} pin
8-1-2: DV_{DD} pin
8-1-3: RX1, RBCK, RLRCK, XIN, TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2, TDATA/PIO3, TXO/PIOEN pins
8-1-4: RX0, RX2, RX3, RX4, RX5/VI, RX6/UI, SDIN, DI, CE, CL, XMODE pins
8-1-5: $\overline{\text{RXOUT}}$, RMCK, $\overline{\text{RBCK}}$, RL$\overline{\text{RCK}}$, SBCK, SLRCK, RDATA, XMCK, XOUT, EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO pins, $\overline{\text{CKST}}$/PB, $\overline{\text{INT}}$, RERR, DO, TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2, TDATA/PIO3, TXO/PIOEN pins
8-1-6: Per input/output pin

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

8.2 Allowable Operating Ranges

Table 8.2: Allowable Operating Ranges at Ta = -30 to 70°C, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	AV_{DD}, DV_{DD}		3.0	3.3	3.6	V
Input voltage range 1	$V_{IN}1$	8-2-1	0	3.3	3.6	V
Input voltage range 2	$V_{IN}2$	8-2-2	0	3.3	5.5	V
Operating temperature	Topr		-30		70	°C

8-2-1: RX1, RBCK, RLRCK, XIN, TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2, TDATA/PIO3, TXO/PIOEN pins
8-2-2: RX0, RX2, RX3, RX4, RX5/VI, RX6/UI, SDIN, DI, CE, CL, XMODE pins

8.3 DC Characteristics

Table 8.3: DC Characteristics at Ta = -30 to 70°C, AV_{DD} = DV_{DD} = 3.0 to 3.6V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input, High	V_{IH}	8-3-1	$0.7V_{DD}$			V
Input, Low	V_{IL}				$0.2V_{DD}$	V
Input, High	V_{IH}	8-3-2	2.0		5.8	V
Input, Low	V_{IL}		-0.3		0.8	V
Output, High	V_{OH}	8-3-3	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-4	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-5	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Output, High	V_{OH}	8-3-6	V_{DD}-0.8			V
Output, Low	V_{OL}				0.4	V
Input amplitude	V_{PP}	8-3-7	200			mV
Consumption current	$I_{DD}1$	8-3-8		1.7	3.4	mA
Consumption current	$I_{DD}2$	8-3-9		17	34	mA
Consumption current	$I_{DD}3$	8-3-10		19	38	mA

8-3-1: CMOS compatible: RBCK, RLRCK, XIN input pins
8-3-2: TTL compatible: Input pins other than those listed above
8-3-3: I_{OH} = –12mA, I_{OL} = 8mA: RMCK output pin
8-3-4: I_{OH} = –8mA, I_{OL} = 8mA: XMCK, XOUT output pins
8-3-5: I_{OH} = –4mA, I_{OL} = 4mA: RXOUT, RBCK, RLRCK, RDATA, SBCK, SLRCK, TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2 output pins, TDATA/PIO3, TXO/PIOEN output pins
8-3-6: I_{OH} = –2mA, I_{OL} = 2mA: Output pins other than those listed above
8-3-7: Before capacitance of RX1 input pin
8-3-8: Demodulation function and oscillation amplifier stopped, modulation only, output sampling frequency = 96kHz
8-3-9: XIN input continuous 24.576MHz oscillation, demodulation only, input sampling frequency = 96kHz
8-3-10: XIN input continuous 24.576MHz oscillation, modulation, input/output sampling frequency = 96kHz

8.4 AC Characteristics

Table 8.4: AC Characteristics at Ta=-30 to 70°C, AV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=DGND=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
RX0 to RX6 sampling frequency	f_{RFS}		28		195	kHz
XIN clock frequency	$f_{XF}1$	8-4-1	8	12.288	19	MHz
XIN clock frequency	$f_{XF}2$	8-4-2	20	24.576	30	MHz
RMCK clock frequency	f_{RCK}		4		100	MHz
RMCK clock jitter	tj			200		ps
RMCK, RBCK delay	t_{MBO}				10	ns
RBCK, RDATA delay	t_{BDO}				10	ns
RMCK, SBCK delay	t_{MBO}	8-4-3			10	ns
SBCK, RDATA delay	t_{BDO}	8-4-4			10	ns
TMCK input pulse width	t_{WMI}		10			ns
RX*, TMCK delay	t_{RDI}				1/4TMCK	ns
TBCK input pulse width	t_{WBI}		40			ns
TLRCK sampling frequency	t_{TFS}		28		195	kHz
TBCK, TDATA setup	t_{DSI}			20		ns
TBCK, TDATA hold	t_{DHI}			20		ns
TMCK, TBCK delay	t_{MBI}	8-4-5			10	ns
TBCK, TDATA delay	t_{BDI}				10	ns

8-4-1: XINSEL = 0 setting, 12.288MHz must be set when calculating input sampling frequency
8-4-2: XINSEL =1 setting, 24.576MHz must be set when calculating input sampling frequency
8-4-3: When RMCK and SBCK source clocks are identical
8-4-4: When SBCK is the PLL source clock
8-4-5: TCKSEL = 0 setting (256fs), the falling edge of TBCK is in synchronization with the rising edge of TMCK.
TCKSEL = 1 setting (128fs), the falling edge of TBCK is in synchronization with the falling edge of TMCK.

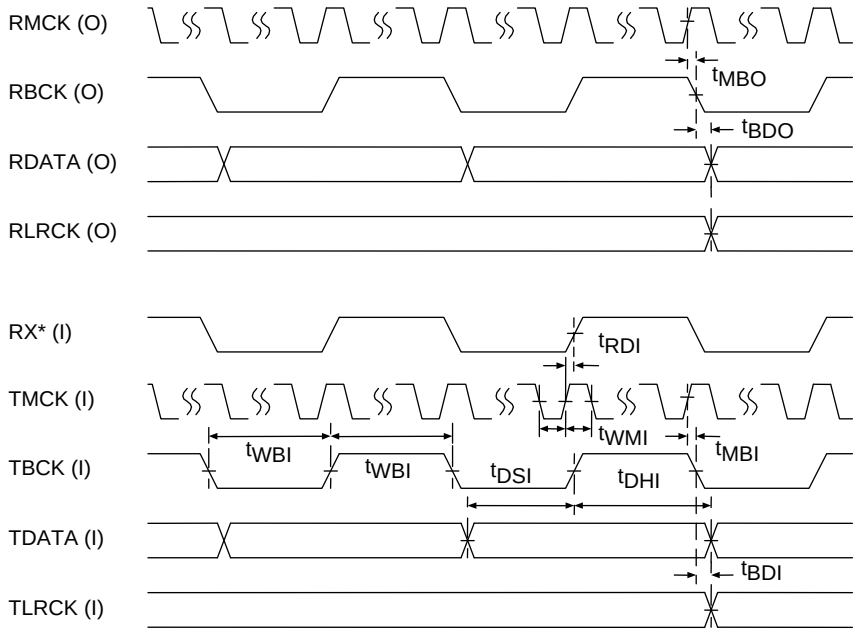


Figure 8.1 AC Characteristics

8.5 Microcontroller Interface AC Characteristics

Table 8.5: I/F AC Characteristics at Ta=-30 to 70°C, AV_{DD}=DV_{DD}=3.0 to 3.6V, AGND=DGND=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
XMODE pulse width, Low	$t_{RST\ dw}$		200			µs
$\overline{INT}$ pulse width, Low	$t_{INT\ wd}$	8-5-1	5	1/fs	36	µs
CL pulse width, Low	$t_{CL\ dw}$		100			ns
CL pulse width, High	$t_{CL\ uw}$		100			ns
CL, CE setup time	$t_{CE\ setup}$		50			ns
CL, CE hold time	$t_{CE\ hold}$		50			ns
CL, DI setup time	$t_{DI\ setup}$		50			ns
CL, DI hold time	$t_{DI\ hold}$		50			ns
CL, CE hold time	$t_{CL\ hold}$		50			ns
CL, DO delay time	$t_{CL\ to\ DO}$				20	ns
CE, DO delay time	$t_{CE\ to\ DO}$				20	ns

8-5-1: When INTOPF is set to "1", fs = input sampling frequency

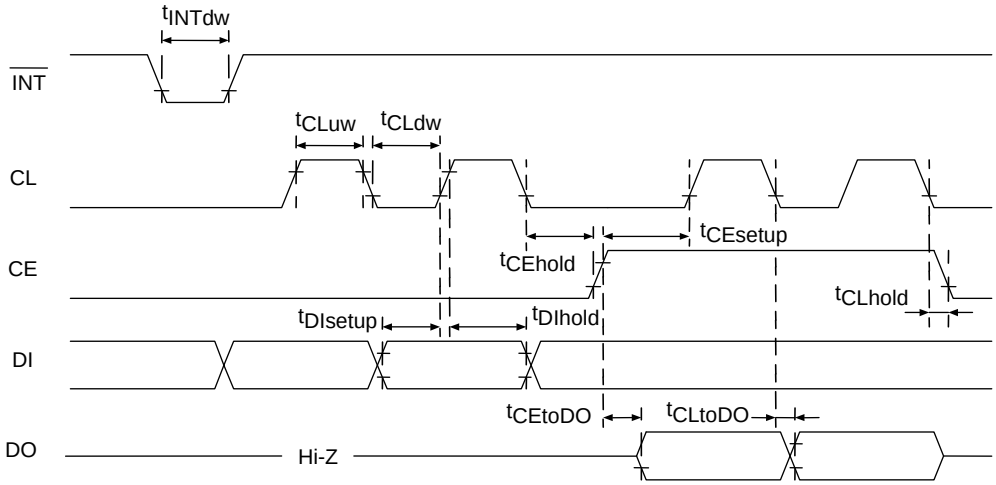


Figure 8.2 Microcontroller Interface AC Characteristics

9. Initial System Settings

9.1 System Reset (XMODE)

- The system operates correctly when XMODE is set to "H" after 3.0V or higher supply voltage is applied. When XMODE is set to "L" after power is turned on, the system is reset.
- When setting chip address, demodulation function master or slave, and modulation function or general-purpose I/O function, connect a 10kΩ pull-down or pull-up resistor to EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO, $\overline{\text{CKST}}$/PB, and $\overline{\text{INT}}$ pins.
- If EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO, $\overline{\text{CKST}}$/PB, and $\overline{\text{INT}}$ are not pulled up or down, their pin state is unstable at the time of input. Consequently proper setting cannot be realized. For these pins, pull-up or pull-down resistor must be connected.

Table 9.1: Pin Names and Settings

Setting	Pins
Chip address	EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO
Demodulation function master or slave	$\overline{\text{CKST}}$/PB
Modulation function or general-purpose I/O function	$\overline{\text{INT}}$

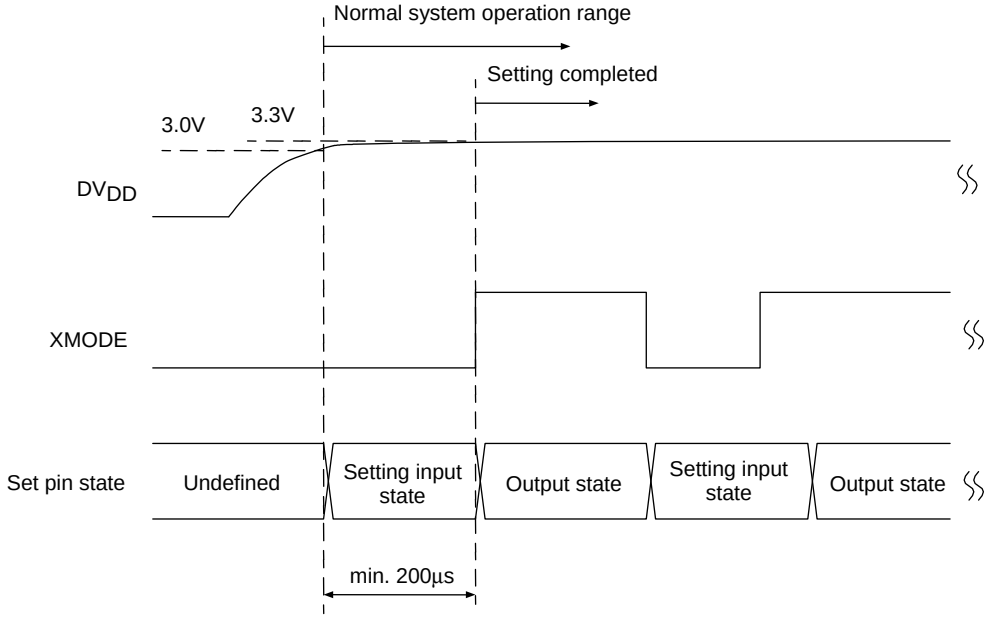


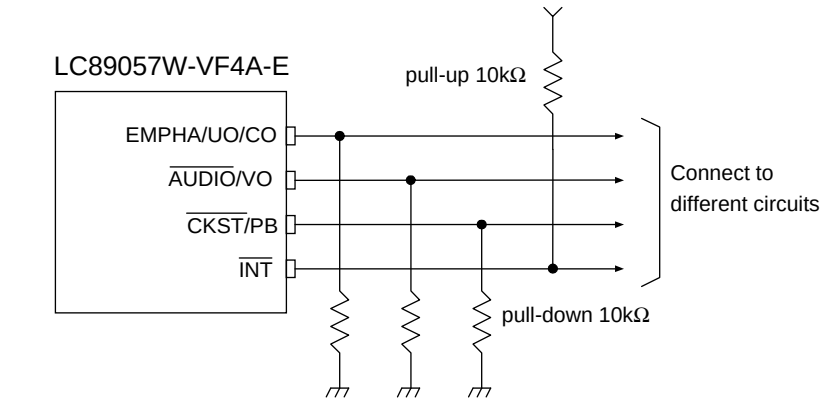
Figure 9.1 Setting Timing Chart of Function Setting Input Pins

9.2 Chip Address Settings (EMPHA/UO/CO, $\overline{\text{AUDIO}}$/VO)

- The LC89057W-VF4A-E comes with a function to set a unique chip address to allow the use of several LC89057W-VF4A-E on the same microcontroller interface bus.
- In chip address setting, connect a 10kΩ pull-down or pull-up resistor to EMPHA/UO/CO and $\overline{\text{AUDIO}}$/VO. By this setting, 4 kinds of chip addresses can be set at a maximum.
- Chip addresses in the microcontroller interface are set with CAL and CAU provided as the first two bits on the LSB side. CAL corresponds to the lower chip address and CAU to the higher chip address.
- Command writing is enabled by making the chip address settings with EMPHA/UO/CO and $\overline{\text{AUDIO}}$/VO identical to the chip addresses sent from the microcontroller.
- The chip address setting is required even when only one LC89057W-VF4A-E is used in the system. If the chip address is not set, the chip address is undefined and the microcontroller cannot control the system. When the microcontroller is not used, a chip address-setting pin is input open while XMODE is "L". Be sure to connect either a pull-down resistor or a pull-up resistor to EMPHA/UO/CO and $\overline{\text{AUDIO}}$/VO.

Table 9.2 Chip Address Settings (Register Connection)

$\overline{\text{AUDIO}}$/VO	EMPHA/UO/CO	CAU	CAL
Pull-down	Pull-down	0	0
Pull-down	Pull-up	0	1
Pull-up	Pull-down	1	0
Pull-up	Pull-up	1	1



Setting Contents of Above Figure

Chip address setting	→ CAIL=CAU=0
Demodulation function master or slave setting	→ Master
Modulation function or General-purpose I/O port switch	→ General-purpose I/O function

Figure 9.2 Setting Example of Function Setting Input Pin

9.3 Demodulation Function Master/Slave Settings ($\overline{\text{CKST}}$/PB)

- A master/slave function that allows multi-channel synchronized transfer using multiple LC89057W-VF4A-E ICs is included. For this setting, connects either a 10kΩ pull-down or a pull-up resistor to $\overline{\text{CKST}}$/PB.
- Set to the master mode normally, when single LC89057W-VF4A-E IC is used. When multiple LC89057W-VF4A-E ICs are used, set one of them to the master mode and the others to the slave mode.
- In the multi-channel synchronous transfer mode using multiple LC89057W-VF4A-E ICs, connect RBCK and RLRCK (output) on the master side to RBCK and RLRCK (input) on the slave side. Also connect XMCK on the master side to XIN on the slave side. At this time, the polarity of RBCK and RLRCK, and the frequency of XIN and XMCK must be identical.
- If the input data sampling frequency or the phase are different between the master mode and slave mode or if the clock sources differ while the sampling frequencies are not different, some of the output data may get dropped or read twice on the slave side. You can see if these are happening by $\overline{\text{INT}}$ and the microcontroller interface.

Table 9.3 Master/Slave Switching (Register Connection)

$\overline{\text{CKST}}$/PB	Mode
Pull-down	Master
Pull-up	Slave

Table 9.4 Clock Pin State

Pin	Master mode	Slave mode
RMCK	Output	Output
RBCK	Output	Input
RLRCK	Output	Input

9.4 Switching between Modulation Function and General-Purpose I/O Port ($\overline{\text{INT}}$)

- The modulation function and the general-purpose I/O function share same pins. Therefore, these two functions cannot be used simultaneously.
- To switch functions, connect either a 10kΩ pull-down or pull-up resistor to $\overline{\text{INT}}$ pin.

Table 9.5 Switching between Modulation Function and General-Purpose I/O Port (Register Connection)

$\overline{\text{INT}}$ State	Function
Pull-down	Modulation function
Pull-up	General-purpose I/O

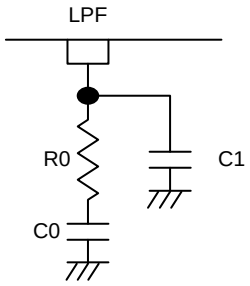
10 Description of Demodulation Function

• The demodulation function is set with RXOPR. An initial value is set to an operating status.

10.1 Clocks

10.1.1 PLL (LPF)

• The LC89057W-VF4A-E incorporates a VCO (Voltage Controlled Oscillator) that can be stopped with PLLOPR and it synchronizes with sampling frequencies from 32kHz to 192kHz and with the data with transfer rate from 4MHz to 25MHz.
• The PLL lock frequency is selected with PLLSEL. For systems whose input data sampling frequency is 105kHz or lower, the initial setting of 512fs is recommended. Since the initial output value of the system clock RMCK is set to 1/2 of PLLSEL, the RMCK output is 256fs when a PLL clock frequency is 512fs.
• For reception systems whose sampling frequency is higher than 105kHz, switch the PLL clock frequency to 256fs. If the same initial output setting is applied, RMCK is 128fs. Then set with PRSEL[1:0] when necessary.
• When the PLL lock frequency is selected with PLLSEL after PLL is locked, unlock is generated. Accordingly, PLLSEL must be set prior to bi-phase data input.
• LPF is a pin for PLL loop filter. Connect the following resistance and capacitances regardless of PLLSEL settings.



Clock	R0	C0	C1
512fs	220Ω	0.1μF	0.022μF
256fs			

Figure 10.1 Loop Filter Configuration

10.1.2 Demodulation function without using PLL (TMCK)

• The LC89057W-VF4A-E has a function that processes input bi-phase data using an external clock (external clock synchronization function). In normal demodulation processing, the built-in PLL generates a clock that is synchronized with data and carries out data processing with the clock. In the LC89057W-VF4A-E, data processing can be also done by providing a clock synchronized with data instead of the PLL-generated clock via an independent transmission path.
• To use the external clock synchronization function, set the PLL unused demodulation function with EXSYNC, set the 256fs or 512fs clock with PLLSEL, and set 1/1 of PLLSEL set frequency with PRSEL[1:0]. After that input the clock synchronized with input data to TMCK. By this settings, the same operation as PLL demodulation processing is performed. For example, 512fs clock should be supplied with TMCK because the setting of PLLSEL is at 512fs in case EXSYNC is set on initial condition. In the event of switching the setting of TMCK clock frequency to 256fs, the setting of PLLSEL should be at 256fs.
• Jitter of input data and clock should be as small as possible. Excessive jitter might invite errors in operation of PLL. Pay attention to the noise of clock transmission path.
• In the external synchronization mode, supply clock with TMCK all the time. Without input of clock, system will shut down and be in malfunction.
• In case of using external clock synchronization mode only, it is not necessary to connect anything to LPF pin. However, configuring PLL loop filter enables to use both PLL clock synchronization mode and external clock synchronization mode by switching EXSYNC.
• Applying the external clock synchronization function can also configure a high-precision clock system using an external PLL.

10.1.3 Oscillation amplifiers (XIN, XOUT, XMCK)

- The LC89057W-VF4A-E features a built-in oscillation amplifier. Connecting a quartz resonator, feedback resistor, and load capacitance to XIN and XOUT can configure an oscillation circuit. When connecting a quartz resonator, use one with a fundamental wave. Be aware that the load capacitance depends on the quartz resonator characteristics.
- If the built-in oscillation amplifier is not used and oscillation module is used as the clock source instead, connect the output of an external clock supply source to XIN. At this time, it is not necessary to connect a feedback resistor between XIN and XOUT.
- Supply XIN with the 12.288MHz or 24.576MHz-clock set with XINSEL. If inputting other frequencies to XIN, it is necessary to set that the result of change in sampling frequency fs of input data is not reflected to an error flag. By this setting, the operation functions properly. However, since time definition gap occurs in relation to the operation with recommended frequency, the encoding result cannot be used for input fs calculations. In this case, the input fs can be calculated by dividing decimally the calculation count value with 1/2000th of the XIN input frequency. For details, see Chapter 12. Microcontroller Interface.
- Since the XIN clock serves as the reference for internal processing, complete the XINSEL setting prior to bi-phase data input.
- Supply XIN with clocks all the time to be used in the following applications.
    (1) Detection whether or not bi-phase data is input
    (2) Clock source while PLL is unlocked
    (3) Calculation of input data sampling frequency
    (4) Time definition when switching input data
    (5) External source of supply clock (clock for an AD converter, etc.) in XIN source mode.

- The oscillation amplifier automatically stops while PLL is locked. However, it can be also set for continuous operation with AMPOPR[1:0]. In the continuous operation mode, data detection and calculation of input sampling frequency become possible while the PLL is locked. In that case, both the oscillator amplifier clock and the PLL clock signals coexist, and then users must pay attention and make sure sound quality is not adversely affected.
- If the oscillation amplifier is set to continuous operation with AMPOPR[1:0] while PLL is locked, RERR temporarily outputs an error ("H"). When oscillation amplifier is switched to an operation state, fs calculation value maintained during a stop state is reset at the same time. This process is regarded as an error, since fs seems to change. This error has no influence on clock output, but RDATA is muted during this error period. Therefore, setting of the AMPOPR[1:0] must be completed either prior to bi-phase data input or while PLL is unlocked.
- The oscillation amplifier can be stopped if it is unnecessary. However, when the normal operation is resumed, it must wait for 10ms or longer until the resonator oscillation gets stable.
- XMCK outputs the XIN clock. The XMCK output is set with XMSEL[1:0]. The XIN clock can be set to 1/1, 1/2, or muted output.
- When only the modulation function is used, no clock needs to be supplied to XIN. In this case, the built-in oscillation amplifier and frequency divider can be also used for MCK, BCK, and LRCK clock generation. If you use only the oscillation amplifier, input the quartz resonator to XIN and XOUT or an external clock to XIN, and fix the electric potential of digital data input pins of RX0 to RX6. At this time, do not set to stop the DIR function with RXOPR and PLLOPR. The output clock may be muted.

10.1.4 Switching between Master clock and clock source

- The RMCK, RBCK, and RLRCK (hereunder, R system), and the SBCK and SLRCK (hereunder, S system) clock sources can be selected among the following three master clocks.
  (1) PLL source (256fs or 512fs)
  (2) XIN source (12.288MHz or 24.576MHz)
  (3) TMCK source (256fs or 512fs)

- There are two ways available for clock source switching; one is to set with the R system and the S system interlocked, and the other is to set only the R system while XIN source is fixed in the S system. This setting is carried out with SELMTD, OCKSEL, and RCKSEL.
- The clock source is automatically switched between PLL clock and XIN clock by locking/unlocking the PLL. During this period, continuity of the clock is maintained. However, if the clock source is switched with SELMTD, continuity of the S system is not maintained.
- The clock source can be switched to XIN with OCKSEL and RCKSEL, regardless of the PLL status. The clock source switch command and each clock output of the R and S systems are shown below.

Table 10.1 Correspondence between Clock Source Switch Commands and Clock Output Pins

SELMTD	R System Output Clock	S System Output Clock
0	According to OCKSEL	According to OCKSEL
1	According to RCKSEL	Fixed to XIN source

Table 10.2 Relationship between Clock Source Switch Commands and Clock Sources when PLL Locked/Unlocked

SELMTD	OCKSEL	RCKSEL	R System Clock Source		S System Clock Source	
			Locked	Unlocked	Locked	Unlocked
0	0	X	PLL	XIN	PLL	XIN
	1	X	XIN	XIN	XIN	XIN
1	X	0	PLL	XIN	XIN	XIN
	X	1	XIN	XIN	XIN	XIN

- TMCK source should be selected with EXYSNC and the input clock frequency (256fs or 512fs) should be set with PLLSEL. The same action as the one of PLL source should be taken except inputting clock from TMCK on this setting.
- When data synchronized with the TMCK source is input, various clocks are output with the TMCK source as the master clock, in a manner similar to the PLL clock status. In this case as well, the source is switched to XIN with OCKSEL and RCKSEL. When the TMCK source is not supplied or the input data is not synchronized, the source is switched to the XIN source, in a manner similar to the PLL source unlocked status.
- The PLL status can be always monitored with RERR even after switching to the XIN source. Moreover, the processed information can be read with the microcontroller interface regardless of the PLL status.
- When the PLL changes from the locked status to the unlocked, the timing for switching the clock from the PLL source to the XIN source can be changed with XTWT [1:0]. Use these commands if noise occurs during clock switching.

10.1.5 Points to notice about switching clock source while PLL is locked

- In the state where the PLL is locked, if the clock is switched to XIN source with SELMTD, OCKSEL, and RCKSEL while the oscillator amplifier is stopped (initial setting), clock continuity is maintained but RERR temporarily outputs an error (high level) indication. When switched to XIN source, the oscillator amplifier is switched to the operating state at the same time. Consequently the input fs calculation restarts. At this time, the previous fs calculation value is reset and compared with the newly calculated fs value. Then those two values are found not identical, that's why the error is temporarily issued.
- The following settings are required to switch the clock source with SELMTD, OCKSEL, and RCKSEL without changing the RERR status while PLL is locked.
  (1) Set the oscillation amplifier to the continuous operation mode with AMPOPR[1:0].
  (2) Set with FSERR to the mode where fs change is not reflected to the error flag.

- By one of the above settings, changing of the RERR status can be constrained when the clock source is switched with SELMTD, OCKSEL, and RCKSEL.
- When switching the clock source to XIN from the state where the oscillation amplifier is stopped while the PLL is locked, the output clock using XIN as the source starts being output after the oscillation amplifier starts operating. When the PLL is locked, switching of the clock source from XIN to PLL is performed instantaneously. In either case, clock continuity is maintained.

10.1.6 Master clock block diagram (TMCK, XIN, XOUT, RMCK, XMCK)

- The relationships between the three master clocks, switching, and the frequency division function, are described below.
- The contents in the square brackets [***] by the switch and function blocks correspond to the write command names.
- Lock/Unlock is automatically switched by PLL locking/unlocking.

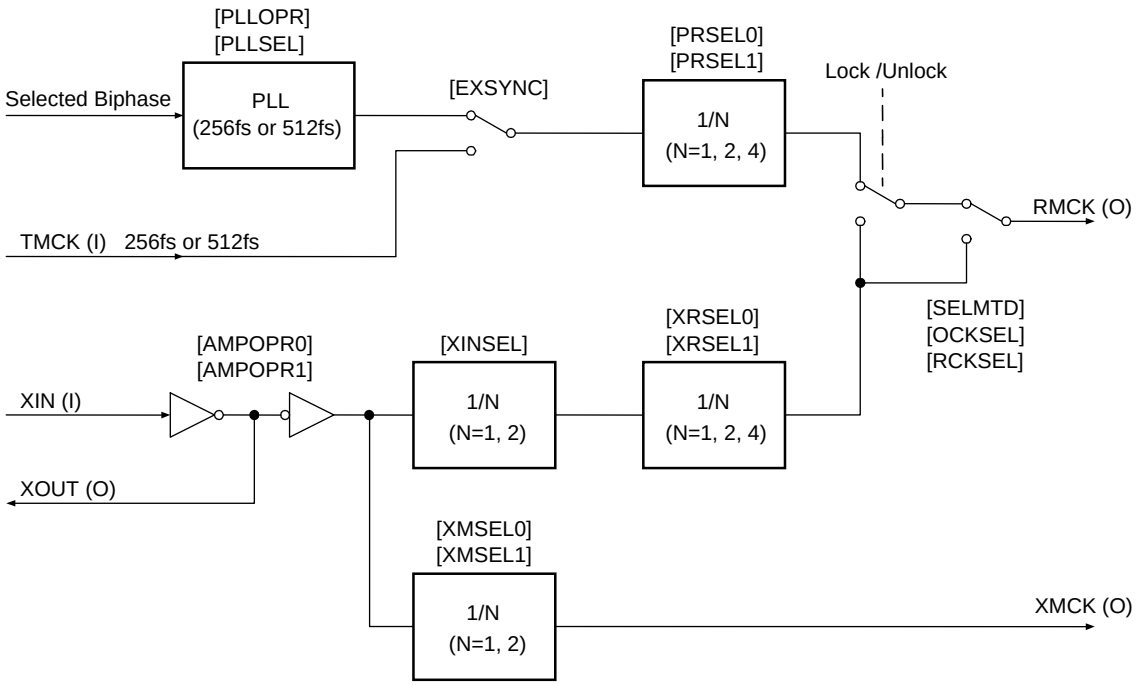


Figure 10.2 Master Clock Block Diagram

10.1.7 Output clocks (RMCK, RBCK, RLRCK, SBCK, SLRCK)

- The LC89057W-VF4A-E features two clock systems (R and S systems) in order to supply the various needed clocks to peripheral devices such as A/D converter and DSP.
- The clock output settings for the R and S systems are done with PRSEL[1:0], XRSEL[1:0], XRBCK[1:0], XRLRCK[1:0], PSBCK[1:0], PSLRCK[1:0], XSBCK[1:0], and XSLRCK[1:0].
- Setting range for each clock output pin when the PLL is used as source
  - (1) RMCK: Selection from 1/1, 1/2, and 1/4 of 512fs or 256fs
  - (2) RBCK: 64fs output
  - (3) RLRCK: fs output
  - (4) SBCK: Selection from 128fs, 64fs, and 32fs
  - (5)SLRCK: Selection from 2fs, fs, and fs/2
- Setting range for each clock output pins when the XIN is used as source
  - (1) RMCK: Selection from 1/1, 1/2, and 1/4 of 12.288MHz or 24.576MHz
  - (2) RBCK: Selection from 12.288MHz, 6.144MHz, and 3.072MHz
  - (3) SBCK: Selection from 12.288MHz, 6.144MHz, and 3.072MHz
  - (4) RLRCK: Selection from 192kHz, 96kHz, and 48kHz
  - (5) SLRCK: Selection from 192kHz, 96kHz, and 48kHz
- Setting range for each clock output pins when the TMCK is used as source
  - (1) RMCK: selection from 1/1, 1/2,1/4 of 512fs or 256fs.
  - (2) RBCK: 64fs output
  - (3) RLRCK: fs output
  - (4) SBCK: selection from 128fs, 64fs, 32fs
  - (5) SLRCK: selection from 2fs, fs, fs/2
- The polarity of RBCK, RLRCK, SBCK, and SLRCK can be reversed with RBCKP, RLRCKP, SBCKP, and SLRCKP.
- Clock switching is processed from the rising edge of RLRCK output after the falling edge of microcontroller interface CE.

Table 10.3 List of Output Clock Frequencies (Bold Items = Initial Settings)

Output Pin Name	PLL Source (Internal VCO CK)		TMCK Source (TMCK input CK)		XIN Source (XIN input CK)	
	512fs	256fs	512fs	256fs	12.288MHz	24.576MHz
RMCK	512fs **256fs** 128fs	256fs **128fs** 64fs	512fs **256fs** 128fs	256fs **128fs** 64fs	**12.288MHz** 6.144MHz 3.072MHz	**24.576MHz** 12.288MHz 6.144MHz
RBCK	**64fs**				12.288MHz 6.144MHz **3.072MHz**	
RLRCK	**fs**				192kHz 96kHz **48kHz**	
SBCK	128fs **64fs** 32fs				12.288MHz 6.144MHz **3.072MHz**	
SLRCK	2fs **fs** fs/2				192kHz 96kHz **48kHz**	

10.1.8 Output clocks block diagram (RMCK, RBCK, RLRCK, SBCK, SLRCK, XMCK)

- The relationships between the output clock and switch function are shown below.
- PLL in the figure indicates the PLL source (or TMCK source), and XIN the XIN source.
- The contents in the square brackets [***] by the switch function blocks correspond to the write command names.
- The broken lines connecting the switches indicate coordinated switching.
- Lock/Unlock is switched automatically by PLL locking/unlocking.
- Master/Slave is switched by master/slave function switching of demodulation function.

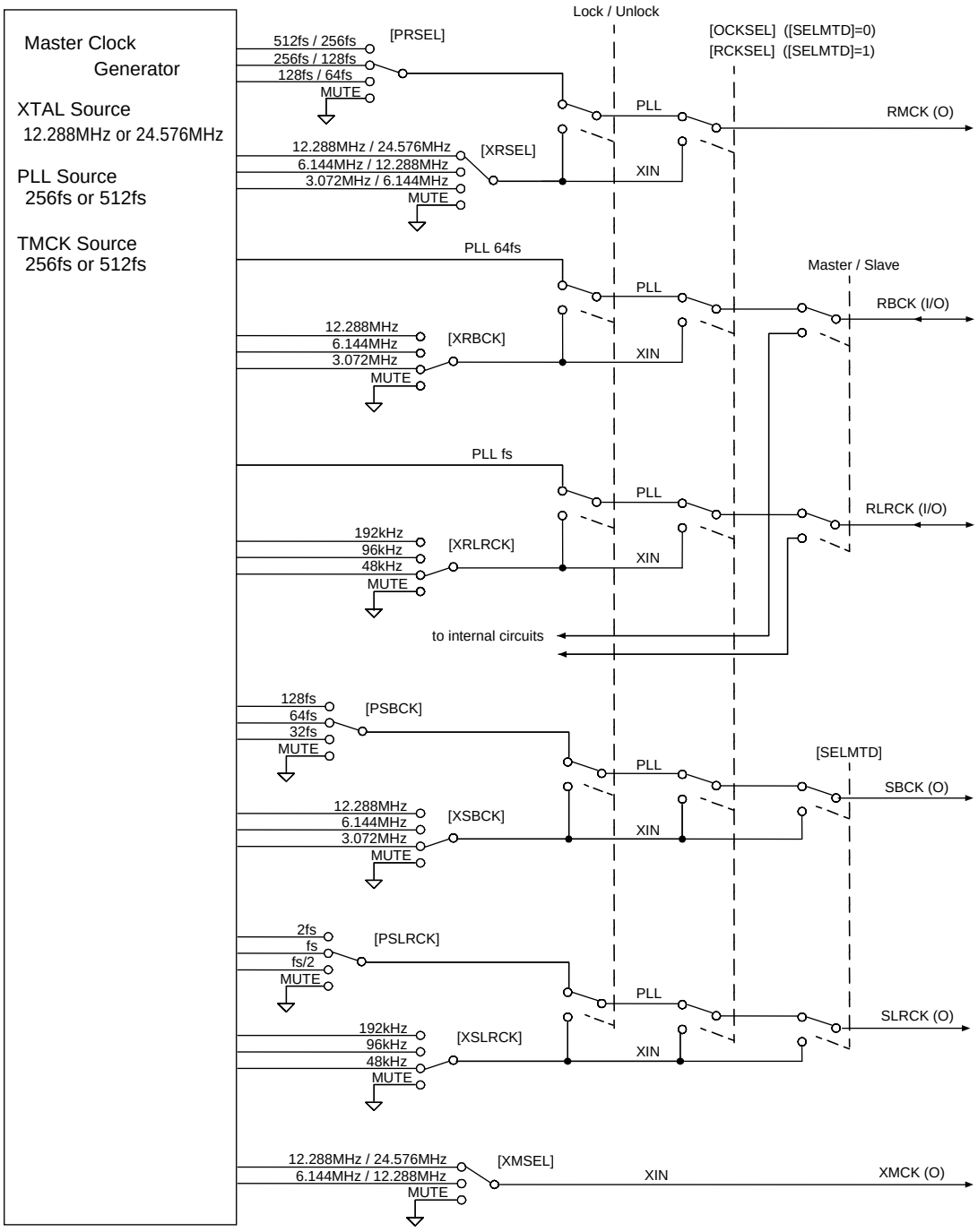
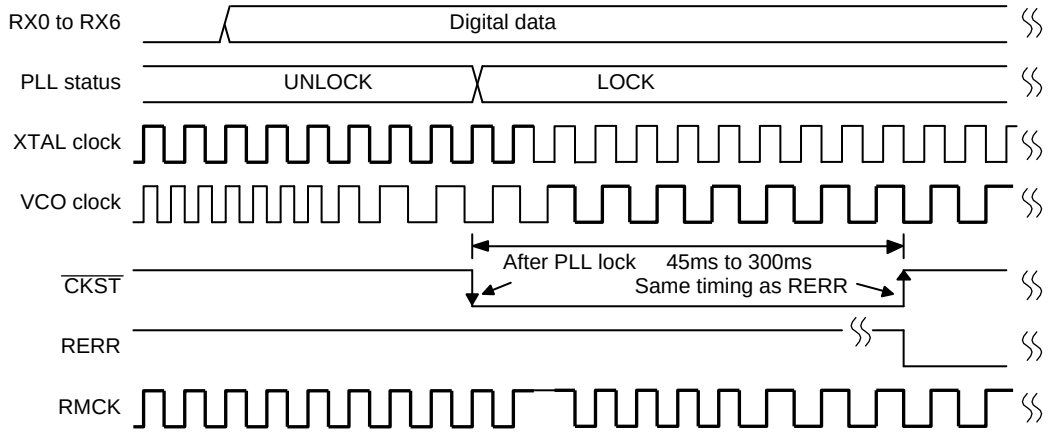


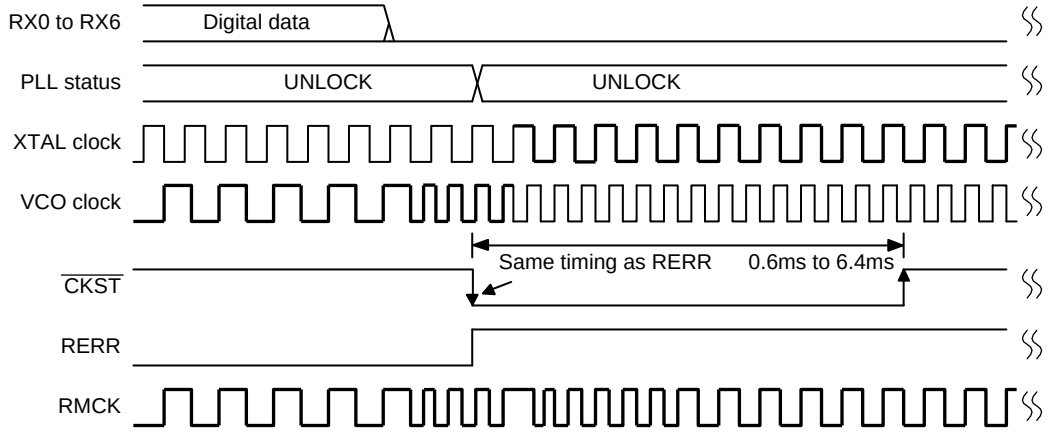
Figure 10.3 Clock Output Block Diagram

10.1.9 Output of Clock switch transition signal ($\overline{\text{CKST}}$)

- $\overline{\text{CKST}}$ outputs "L" pulse when the output clock changes by PLL lock/unlock.
- In the lock-in stage, the $\overline{\text{CKST}}$ "L" pulse falls at the word clock generated from the XIN clock after PLL is locked following detection of input data, and rises at the same timing as RERR after a designated period.
- In the unlock stage, the $\overline{\text{CKST}}$ "L" pulse falls at the same timing as RERR, PLL lock detection signal, and rises after word clocks generated from the XIN clock are counted for a designated period.
- Change of the PLL lock status and timing of the clock change can be seen by detecting the rising and falling edges of the $\overline{\text{CKST}}$ "L" pulse.



(a): Lock-in stage



(b): Unlock stage

Figure 10.4 Clock Switch Timing

10.2 Bi-phase Signal I/O

10.2.1 Reception range of bi-phase signal input

• Reception range of the input data depends on the PLL lock frequency setting done with PLLSEL. The relationship between this setting and the guaranteed reception range is shown below.

Table 10.4 Relationship between PLL Output Clock Setting and Reception Range (FSLIM [1:0] = 00)

PLL Output Clock Setting	Input Data Reception Range
512fs (PLLSEL = 0)	28kHz to 105kHz
256fs (PLLSEL = 1)	28kHz to 195kHz

• The fs reception range for input data can be limited within the set range of PLL output clocks stated above. This setting is carried out with FSLIM [1:0]. When this function is adopted, input data exceeding the set range is considered as an error, the clock source is automatically switched to the XIN source, and RDATA output data is subject to the RDTSEL setting.

10.2.2 Bi-phase signal I/O pins (RX0 to RX6, RXOUT)

• There are 7 kinds of digital data input pins. Moreover, data modulated with the modulation function is also available and thus there are 8 options in total. However, the pins to be selected are restricted, depending on the setting conditions.
  (1) The six pins of RX0 and RX2 to RX6 are TTL level input pins with 5V-tolerance voltage.
  (2) RX1 is an input pin with built-in amplifier, which is coaxial-compatible and it, can receive up to min, 200mVp-p data.
• The demodulation input and RXOUT output signals could each be selected independently.
  (1) The demodulation data is selected with RISEL [2:0].
  (2) The RXOUT output data is selected with ROSEL [2:0].
• RXOUT can be muted with RXOFF. Muting is recommended to reduce clock jitter when RXOUT is not used.
• The data input status can be monitored with the RXMON setting. The status of each data input pin is stored in CCB address 0xEA and output registers DO0 to DO7. Since this function uses the XIN clock, the oscillation amplifier must be set to the continuous operation mode when RXMON is set.
• Demodulation input pin can be switched via PLL unlock with the ULSEL setting. Thus data switching can be accurately conveyed to peripheral devices.
  The interval from pin switching through RISEL [2:0] until the data is received is about 250µs to 350µs. In this function, the oscillation amplifier also needs to be set to the continuous operation mode.

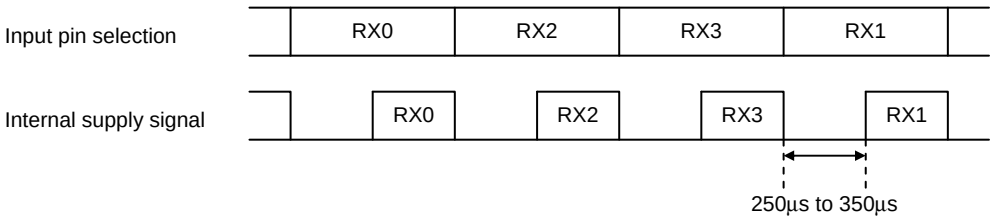


Figure 10.5 Input Pin Selecting Process via PLL Unlock

10.2.3 Bi-phase signal input circuits (RX0, RX1, RX2)

- If RX1 with a built-in amplifier is used as a coaxial input pin, malfunction may occur due to the influence from the adjacent RX0 and RX2 input pins. To avoid the influences from those pins, fix RX0 and RX2 to "L".
- When RX1 is selected and the input signal to RX1 is temporarily open because of AC coupling, the RX0 and RX2 potential must be fixed. In this case, there are 5 bi-phase signal input pins available, which are RX1 and RX3 to RX 6.
- When RX1 is selected and the input signal to RX1 is always fixed to either "H" or "L", RX0 and RX2 processes are not required. In this case, all 7 input pins can be used validly.

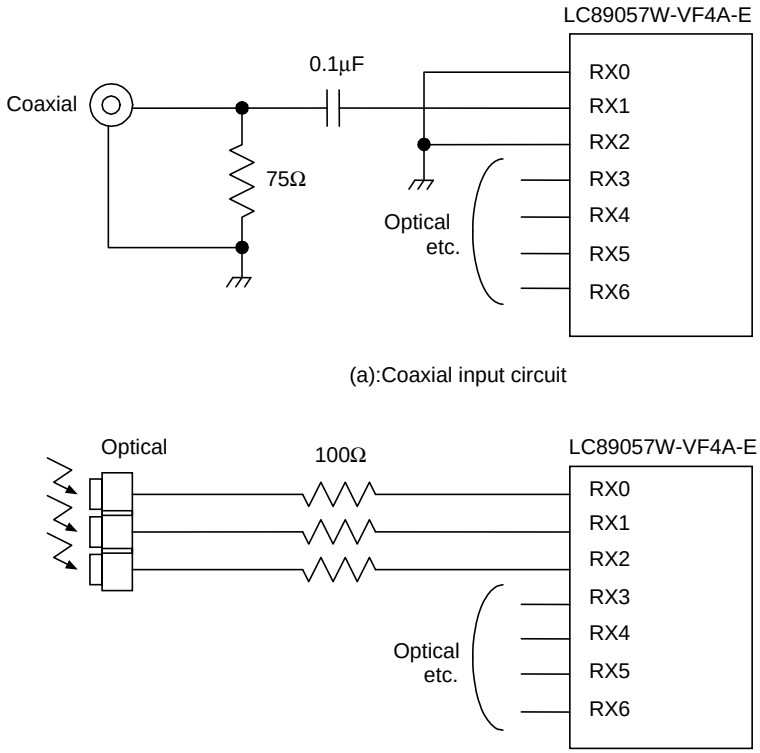
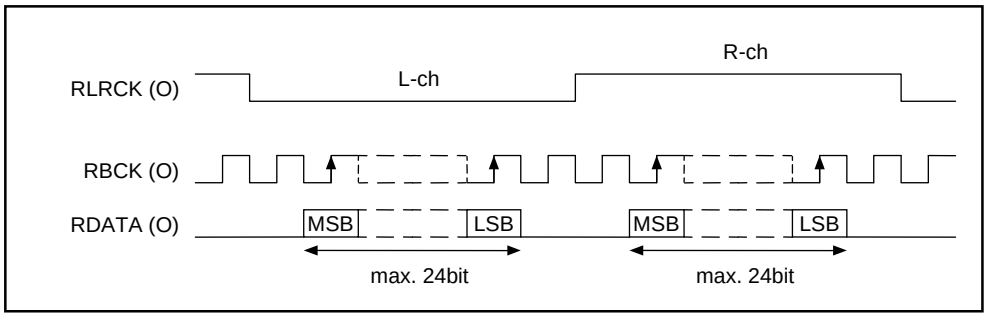


Figure 10.6 Bi-Phase Signal Input Circuits

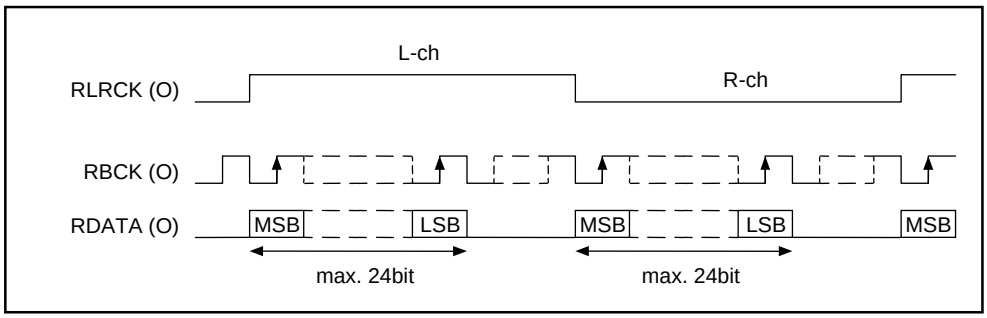
10.3 Serial Audio Data I/O

10.3.1 Output data format (RDATA)

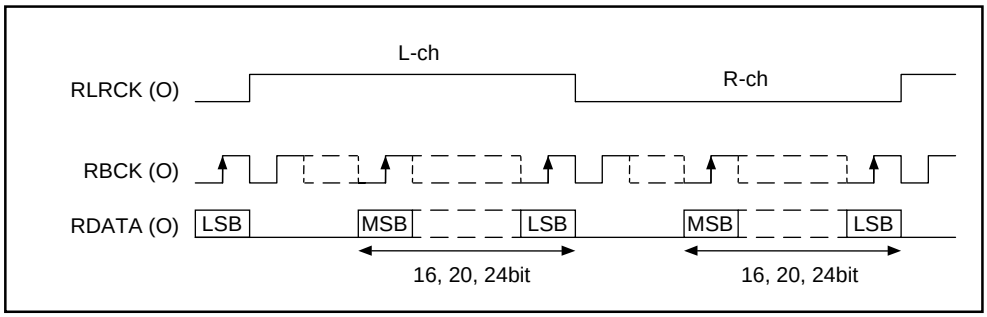
- The output format is set with OFSEL [2:0].
- The initial value of output format is I^2S.
- Right-adjusted output is valid only in the master mode. In the slave mode, data is not output correctly.
- Output data is output synchronized with the RLRCK edge immediately after the RERR output becomes "L".



(0): I^2S data output



(1): MSB-first front-loading data output

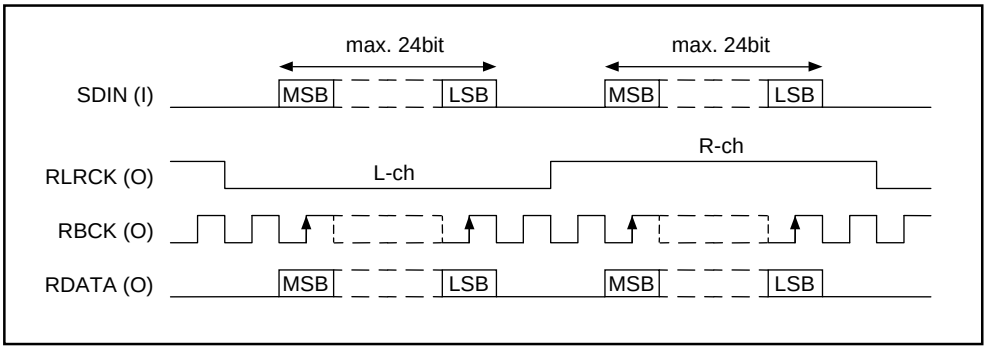


(2): MSB-first back-loading data output

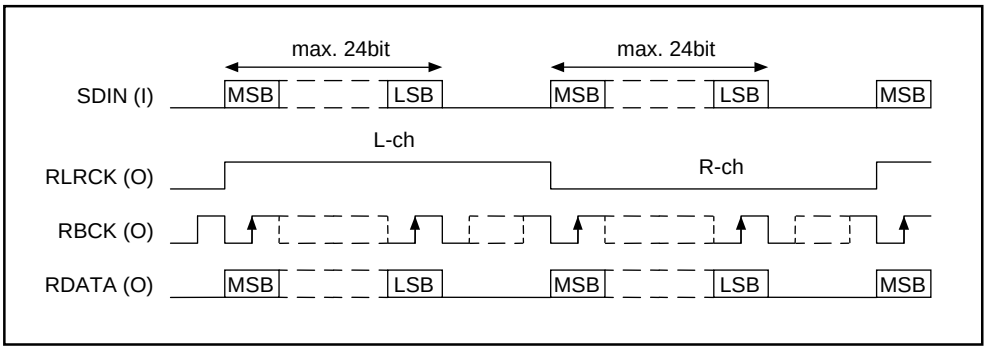
Figure 10.7 Data Output Timing

10.3.2 Serial audio data input format (SDIN)

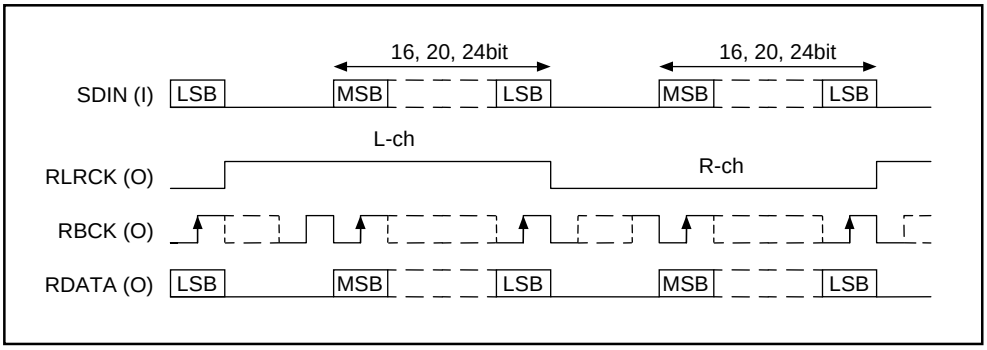
- Serial digital audio data input pin of SDIN capable of 24 bits input is provided.
- The format of the serial audio data input to SDIN and the demodulation data output format must be identical. The initial value of modulation data output is I^2S.



(0): I^2S data input



(1): MSB-first front-loading data input

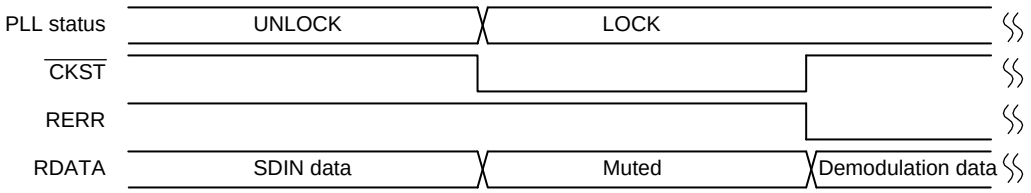


(2): MSB-first back-loading data input

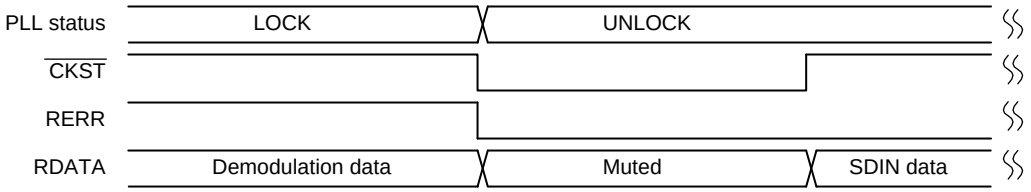
Figure 10.8 Serial Audio Data Input Timing

10.3.3 Output data switching (SDIN, RDATA)

- RDATA outputs demodulation data when the PLL is locked, and outputs SDIN input data when the PLL is unlocked. This output is automatically switched according to the PLL locked/unlocked status. For details, see the timing charts below.
- When SDIN input data is selected, switch to a clock source synchronized to the SDIN data.
- With the RDTSTA setting, the SDIN input data is output to RDATA regardless of the locked/unlocked status of the PLL.
- With the RDTMUT setting, the RDATA output data can be also muted forcibly.
- Even when the clock source is set to XIN with OCKSEL and RCKSEL, the PLL continues operating as long as the PLL is not stopped with PLLOPR. At this time, the PLL status is continuously output from RERR unless error output is forcibly set with RESTA. Moreover, the processed information can be read with the microcontroller interface regardless of the PLL status.



(a): Lock-in stage



(b): Unlock stage

Figure 10.9 Timing Chart of RDATA Output Data Switching

10.3.4 Data block diagram (RX0 to RX6, TX0, RXOUT, TDATA, RDATA, SDIN)

- The RDATA output data can be switched to SDIN input data with RDTSEL.
- The SDIN input data can be input to the modulation function with TDTSEL.
- Since the modulation output is input to the input switch multiplexer, it can be fetched from RXOUT. Using this function, it is possible to use a signal digitized with the A/D converter for digital recording output, etc.

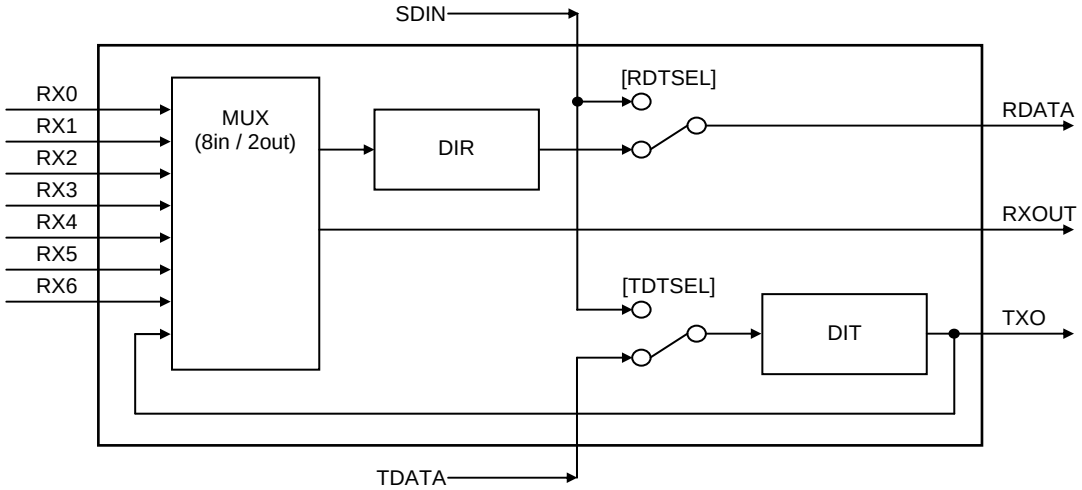


Figure 10.10 Data System Diagram

10.3.5 Calculation of input data sampling frequency

- The input data sampling frequency is calculated using the XIN clock.
- In the mode where the oscillation amplifier automatically stops according to the lock status of the PLL, the input data sampling frequency is calculated during the RERR error period and completed when the oscillation amplifier stops with holding the value. Therefore, the value remains unchanged until the PLL becomes unlocked.
- If the oscillation amplifier is in a continuous operation mode, calculation is repeated constantly. Even if sampling changes within the PLL capture range for input data whose channel status sampling information does not change, the calculation results that follow the input data can be read.
- The calculation result can be read from CCB address 0xEB and output registers DO4 to DO7 and DO8 to DO15. Registers DO4 through DO7 hold the encoded result, while DO8 through DO15 hold the calculated counter value. However, as the calculation count value is output in 8 bit units, fs capable of being calculated are greater than 24kHz. For details, see Chapter 12. Microcontroller Interface.

10.4 Error Output Processing

10.4.1 Lock error and data error output (RERR)

- RERR outputs an error flag when a PLL lock error or a data error occurs.
- It is possible to treat non-PCM data reception as an error by the RESEL setting.
- The RERR output conditions are set with RESTA. Since the PLL status can be output at all times, the PLL status can be always monitored, even when the clock source is XIN.

10.4.2 PLL lock error

- The PLL gets unlocked for input data that lost bi-phase modulation regularity, or input data for which preambles B, M, and W cannot be detected.
- RERR turns to "H" upon occurrence of a PLL lock error, and returns to "L" when data demodulation returns to normal and "H" is maintained for somewhere between 45ms and 300ms.
- The rising and falling edges of RERR are synchronized with RLRCK.

10.4.3 Input data parity error

- Odd number of errors among parity bits in input data and input parity errors are detected.
- If an input parity error occurs 9 or more times in succession, RERR turns to "H" indicating that the PLL is locked, and after holding "H" for somewhere between 45ms and 300ms, it returns to "L".
- The error flag output format can be selected with REDER, when an input parity error is output less than 9 times in succession.

10.4.4 Other errors

- Even if RERR turns to "L", the channel status bits of 24 to 27 (sampling frequency) are always fetched and the data of the previous block is compared with the current data. Moreover, the input data sampling frequency is calculated from the fs clock extracted from the input data, and the fs calculated value is compared in a same way as described above. If any difference is detected in these data, RERR is instantly made "H" and the same processing as for PLL lock errors is carried out.
- The PLL causes a lock error when the fs changes as described above. However, in order to support sources with a variable fs (for example a CD player with a variable pitch function), it is possible to set with FSERR not to output an error flag unless fs changes exceeding the PLL capture range.
  Moreover, in the FSERR setting, when the PLL is locked, RERR is turned to “L” without reflecting the fs calculation result to the error flag concerning input data within reception range by FSLIM[1:0].
- If a setting which regard non-PCM data input as an error is made with RESEL, RERR turns to “H” when non-PCM data input is detected. At this time, the PLL locked status and various output clocks are subject to the input data, but the output data is muted.

10.4.5 Data processing upon occurrence of errors (lock error, parity error)

- The data processing upon occurrence of an error is described below. If 8 or fewer input parity errors occur in succession and transfer data is PCM audio data, the data is replaced by the one saved each in L-ch and R-ch in the previous frame. However, if the transfer data is non-PCM data, the error data is output as it is. Non-PCM data is the data of when bit 1 non-PCM data detection bit of the channel status turns to "H" based on the data detected prior to the occurrence of the input parity error.
- Output data is muted when a PLL lock error occurs or a parity error occurs 9 or more times in succession.
- As for the channel status output, the data of the previous block is held in 1-bit units when a parity error occur 8 or fewer times in succession.

Table 10.5 Data Processing upon Error Occurrence

Data	PLL Lock Error	Input Parity Error (a)	Input Parity Error (b)	Input Parity Error (c)
RDATA output	"L"	"L"	Previous value data	Output
fs calculation result	"L"	Output	Output	Output
Channel status	"L"	"L"	Previous value data	Previous value data
Validity flag	"L"	"L"	Output	Output
User data	"L"	"L"	Output	Output

* Input parity error (a): If occurs 9 or more times in succession
* Input parity error (b): If occurs 8 or fewer times in succession, in case of audio data
* Input parity error (c): If occurs 8 or fewer times in succession, in case of non-PCM burst data

- Figure 10.11 shows an example of data processing upon occurrence of a parity error.

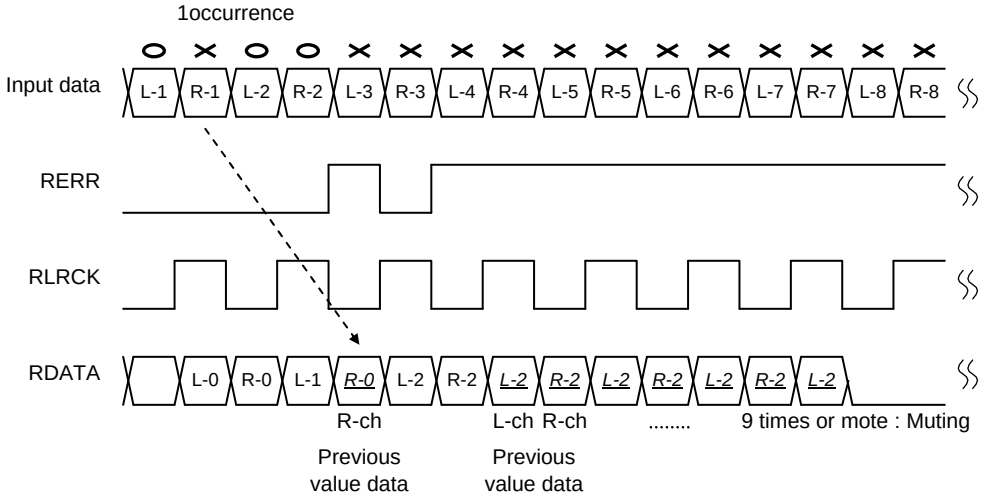


Figure 10.11 Example of Data Processing upon Parity Error Occurrence

10.4.6 Processing during error recovery

• When preambles B, M, and W are detected, PLL becomes locked and data demodulation begins.
• RDATA output data is output from the RLRCK edge after RERR turns to "L".

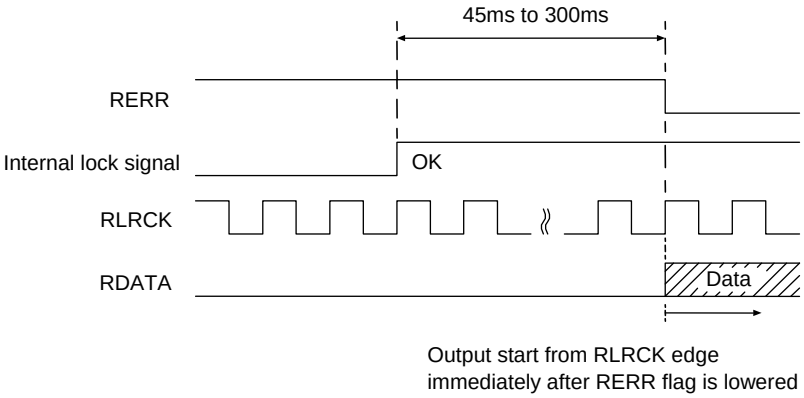


Figure 10.12 Data processing when data demodulation starts

10.5 Channel Status Data Output

10.5.1 Data delimiter bit 1 output ($\overline{\text{AUDIO}}$)

• $\overline{\text{AUDIO}}$ outputs bit 1 of the channel status that indicates whether the input bi-phase data is PCM audio data. $\overline{\text{AUDIO}}$ is immediately output upon detection of RERR even during "H" output period.
• OR-output with IEC61937 or with the DTS-CD/LD detection flag is also possible with AOSEL.

Table 10.6 $\overline{\text{AUDIO}}$ Output

$\overline{\text{AUDIO}}$	Output Conditions
L	PCM audio data (CS bit 1 = "L")
H	Non-audio data (CS bit 1 = "H")

10.5.2 Emphasis information output (EMPHA)

• EMPHA outputs shows whether there are 50/15μs emphasis parameters for consumer and broadcast studio. EMPHA is immediately output upon detection of RERR even during "H" output.

Table 10.7 EMPHA Output

EMPHA	Output Conditions
L	No pre-emphasis
H	50/15μs pre-emphasis

10.6 Other Outputs

10.6.1. Validity flag output (VO)

- The validity flag can be output from $\overline{\text{AUDIO}}$/VO by switching the contents of $\overline{\text{AUDIO}}$/VO output by VOSEL.
- The validity flags transferred in units of each sub-frame are output in the following timing.
- The validity flag is generated 0.5 to 1 frame earlier than the output data in error.

Table 10.8 VO Output

VO	Output Conditions
L	No error (not burst data)
H	Error (May be burst data)

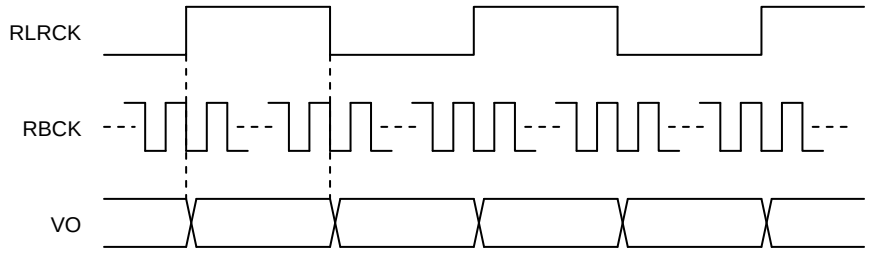


Figure 10.13 Validity Flag Output Timing

10.6.2 User data output (UO)

- User data can be output from EMPHA/UO/CO by switching the contents of EMPHA/UO/CO output by UOSEL.
- The UOSSEL setting, however, is enabled only when PESEL1 is set to 0; it is disabled if PBSEL1 is set to 1. The state of PBSEL0 has nothing to do with this processing
- The user data transferred in units of each sub-frame are output in the following timing.

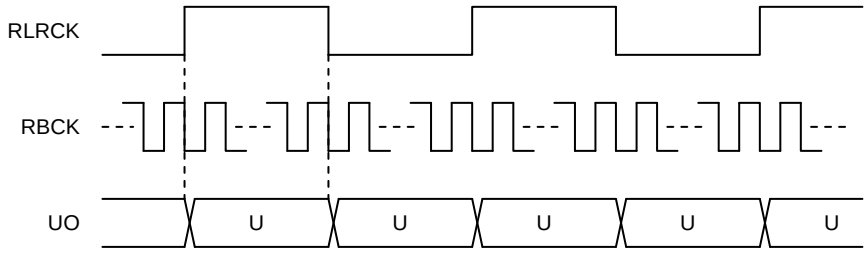


Figure 10.14 User Data Output Timing

10.6.3 Channel status data output (CO)

- Possible to output channel status data from EMPHA/UO/CO by switching PBSEL1 that performs the setting of Preamble B synchronization signal output.
- Polarity of RLRCK is uncertain because channel status data loads data and outputs them on each sub-flame. However, the timing for a period of H output of preamble B synchronization signal PB and bit 0 data output (c0 Lch, c0 Rch) of channel status is shown on the following figure.

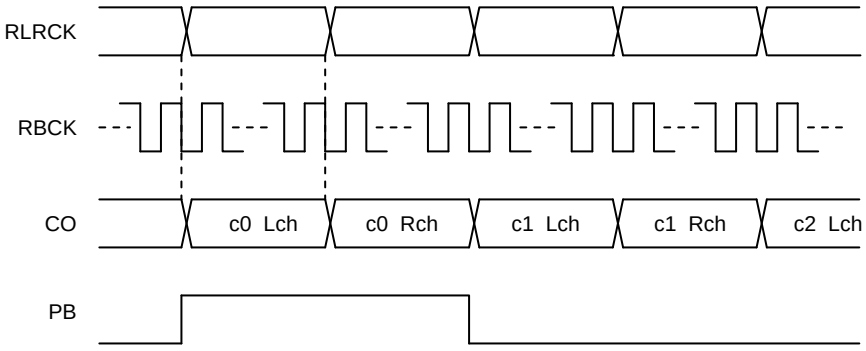


Figure 10.15 Channel Status Data Output Timing

10.6.4 Preamble B synchronization signal output (PB)

- Possible to output preambles B synchronization signal that is block synchronization of channel status from $\overline{\text{CKST}}$/PB by switching the content of $\overline{\text{CKST}}$/PB output by PBSEL [1:0].
- For the period that bit 0 data of the channel status is output, PB signal outputs H. For the otherwise period, it outputs L.
- Regarding PBSEL [1:0], possible to output preamble B synchronization signal with DIT function. However, impossible to set output preamble B with DIR function and DIT function from PB at once because they share the terminal.
- In case of setting preamble B synchronization signal output with DIR function, the channel status data is output from EMPHA/UO/CO pin, and the setting of UOSEL is invalid.

10.7 IEC61937, DTS-CD/LD Detection Flag Output

- A function to output IEC61937 and DTS-CD/LD detection flags for Non-PCM data is provided.
- When the UNPCM of non-PCM signal output setting is selected through the $\overline{\text{INT}}$ output contents setting, an interrupt signal is output from $\overline{\text{INT}}$ detecting an IEC61937 or DTS-CD/LD sync signal. Reading output register from this information can see details of Non-PCM signal.
- When bit 1 of channel status is non-PCM data ("1"), the IEC61937 sync signal is detected and output. If bit 1 is PCM data, the IEC61937 sync signal is not output.
- DTS-CD/LD sync signal detection is done based on the sync pattern and the base frequency. DTS-ES data detection is output when the DTS5.1 channel sync signal is detected and the DTS-ES sync pattern is verified.
- The IEC61937 and DTS-CD/LD detection flags are cleared when fs have changed or a PLL lock error or data error has occurred.
- Since the DTS sync signal is provided within the audio data, digital data with the same code as the DTS sync signal may exist in rare cases for regular CD/LD records that are not recorded in the DTS format. Protection using the sync pattern or base frequency is provided so that such data is not misinterpreted as DTS-CD/LD detection flags. The detection sequence is shown below.

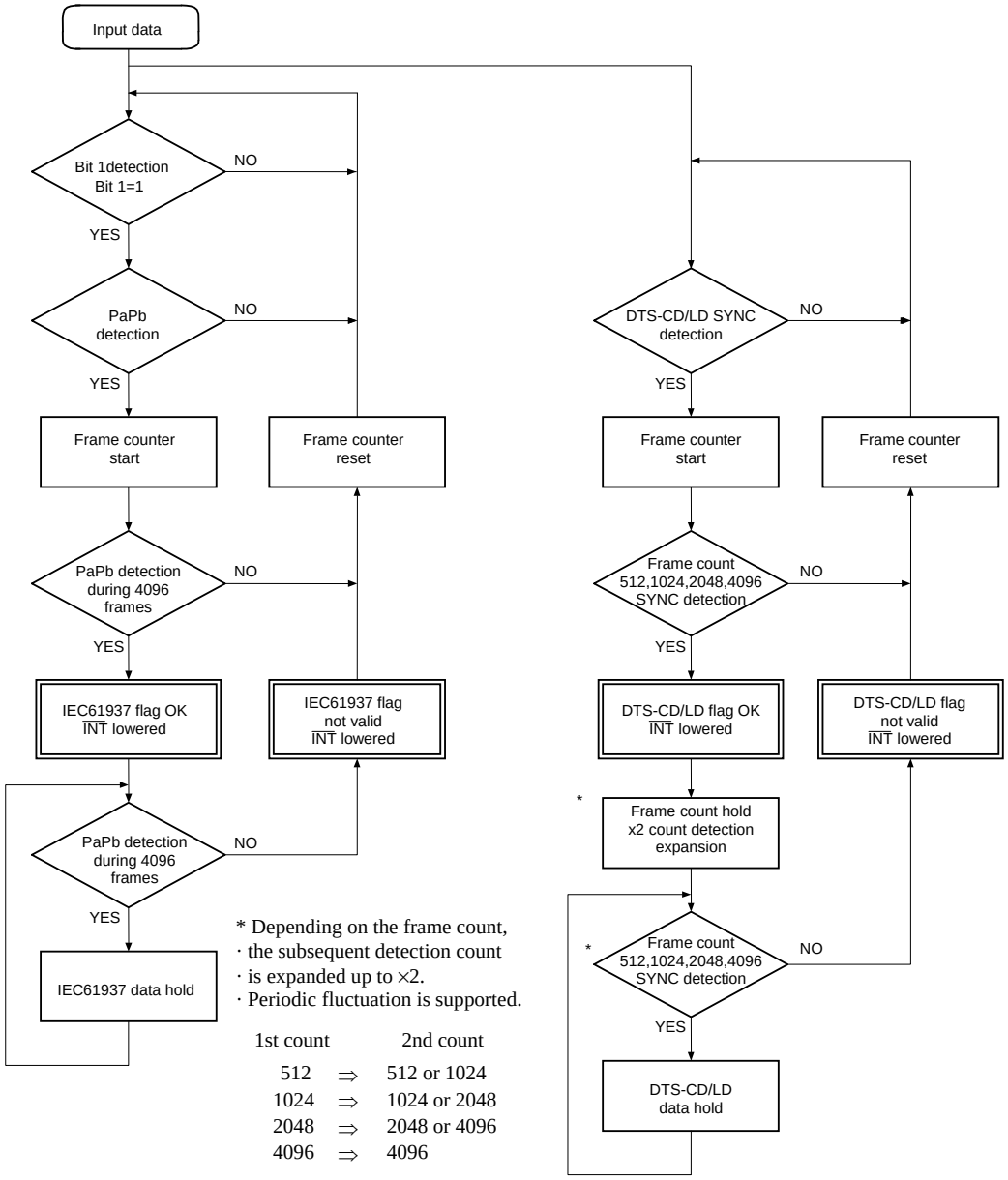


Figure 10.16 IEC61937 and DTS-CD/LD Data Detection Sequence

11. Description of Modulation Function and General-Purpose I/Os

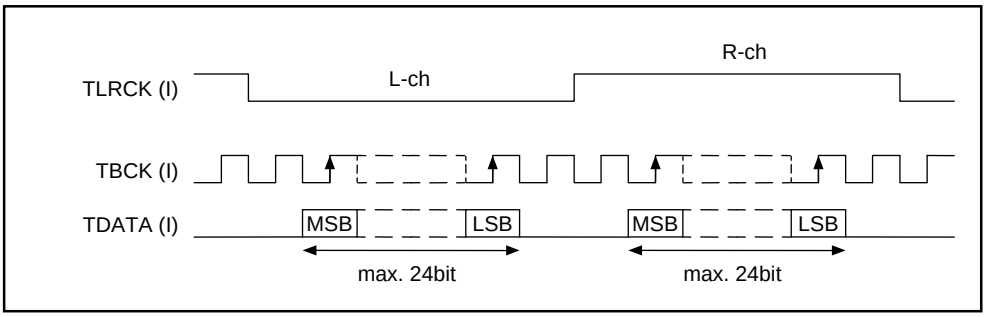
11.1 How to Use Modulation Function

11.1.1 Initial setting

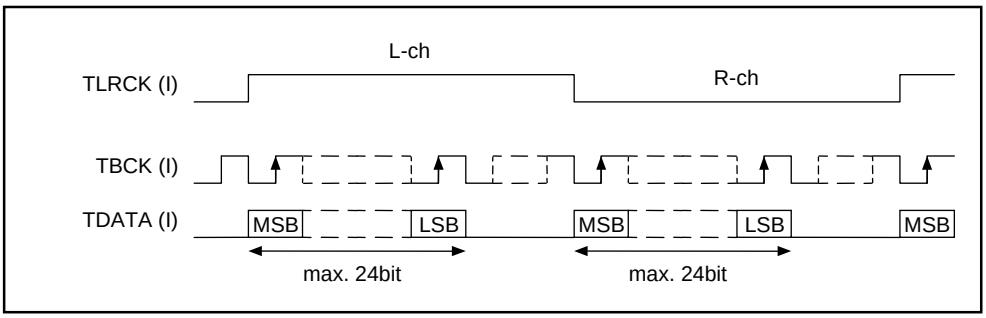
- The modulation function and general-purpose I/O port function cannot be used simultaneously because they share the same pins. To select the modulation function, pull down $\overline{INT}$ with a 10kΩ resistor. For further information about the setting, see Chapter 9.
- In the initial setting, the modulation function is stopped. To apply the modulation function, set it with TXOPR.

11.1.2 Data output (TMCK, TBCK, TLRCK, TDATA, TXO)

- Output bi-phase modulated data from TXO by inputting 256fs or 128fs clock into TMCK, 64fs clock into TBCK, fs clock into TLRCK, audio data into TDATA.
- Set TCKSEL for clock frequency to input into TMCK. However, the falling edge of TBCK is in synchronization with the rising edge for TMCK when the TMCK is set at 256fs. Also, the falling edge of TMCK is in synchronization with the falling edge of TBCK when TMCK is set at 128fs.
- The polarity of the TLRCK clock is set with TXLRP.
- Input data can be modulated in the sampling range of 32kHz to 192kHz, in the transfer rate of 4MHz to 25MHz, and up to 24-bit data.
- The initial value for the input data format is set in I^2S. Switching to MSB-first right-adjusted input is set with TXDFS.
- For the channel status, the first 48 bits of data can be written with the microcontroller interface.
- TXO is fixed to "L" by setting TXOPR to stop or TXMUT.



(0): I^2S data output



(1): MSB-first front-loading data output

Figure 11.1 Data Input Timing

11.1.3 Validity flag input (VI)

- Validity flags can be input from RX5/VI by switching the contents of RX5/VI input by VISEL.
- The timing of writing a validity flag is shown below. The validity flag can be also written with the microcontroller interface, but port settings have priority over the validity flag.
- Writing validity flags with the microcontroller interface is done using VMODE.

Table 11.1 RX5/V1 Input

RX5/VI	Output Conditions
0	No error
1	Error

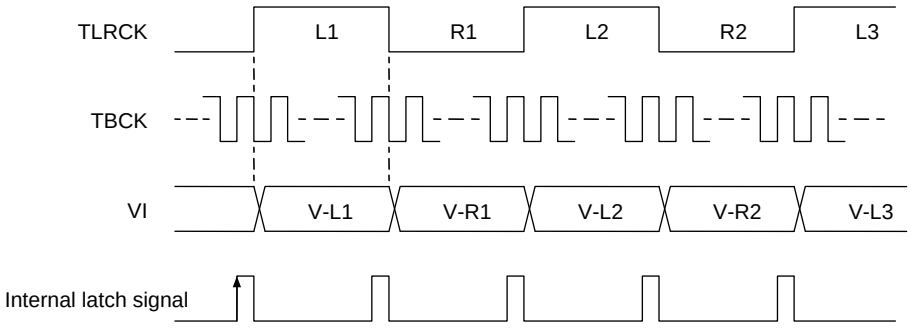


Figure 11.2 Validity Flag Input Timing

11.1.4 User data input (UI)

- User data can be input from RX6/UI by switching the contents of RX6/UI input by UISEL.
- The timing of writing the user data is shown below.
- It is also possible to write user data using the preamble B sync signal as the reference. Generation of the preamble B sync signal is configured in PBSEL[1:0] as in the case of the DIR function. After the setting, the signal is output from CKST/PB.

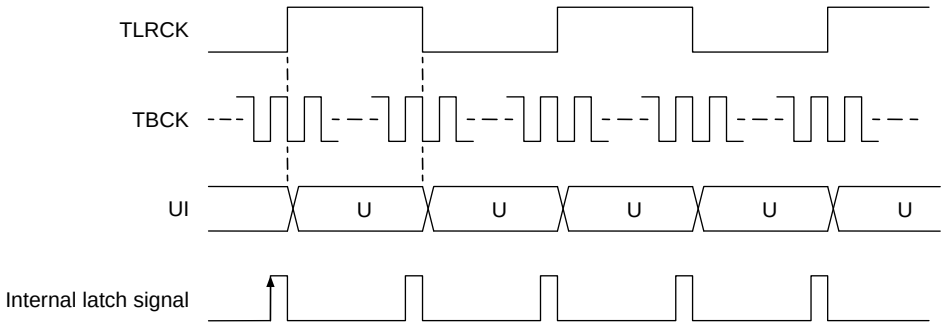


Figure 11.3 User Data Input Timing

11.1.5 Modulated output of SDIN input data

- SDIN input data is modulated and its output can be fetched from TXO and RXOUT.
- To modulate SDIN input data, set it with TDTSEL.
- Input a clock synchronized with SDIN to TMCK, TBCK, and TLRCK.
- The SDIN input data format must be identical to the setting used during modulation processing.

11.1.6 Monaural output

- It is possible to output only single channel data of the input data at half the rate of the input fs with TXMOD[1:0].
- This operation maintains the bi-phase modulation regularity, but there is no correlation between the data and preambles.
- Channel status write is synchronized with the output rate.
- The validity flag and user data are written in units of frame. Input the same data to the L and R channels.
- To process the stereo signals of two channels with this setting, two units of LC89057W-VF4A-E are required.

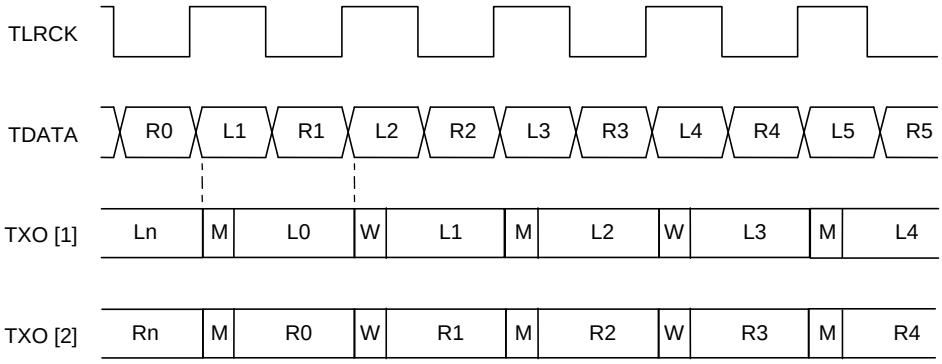


Figure 11.4 Data Modulation of Single Channel

11.2 General-Purpose I/Os (PIO0, PIO1, PIO2, PIO3 PIOEN)

11.2.1 Initial settings

- The modulation function and general-purpose parallel I/Os share the same pins and therefore they cannot be used simultaneously. To use the general-purpose I/Os, pull up $\overline{\text{INT}}$ with a 10kΩ resistor. For further information about the setting, see Chapter 9.
- The general-purpose parallel I/O applies parallel-conversion to the serial data input from the microcontroller interface, and outputs it from PIO0, PIO1, PIO2, and PIO3. The input function saves the parallel data input to PIO0, PIO1, PIO2, and PIO3 in internal registers and reads the contents of these registers with the microcontroller interface.
- 4-bit general-purpose I/Os cannot be used with both input and output mixed. Switching between input and output is done with PIOEN. When PIOEN is "H", all the general-purpose I/Os become input pins. When PIOEN is "L", all the general-purpose I/Os become output pins.

11.2.2 I/O settings

- Data handling for general-purpose I/Os is done using the microcontroller interface and write/read registers. See Chapter 12 Microcontroller Interface for details.
- General-purpose I/O writes settings (Microcontroller → Write register → General-purpose I/O output)

(1) To output data from general-purpose I/Os, set PIOEN to "L".
(2) Set the data to be output to CCB address 0xE8, command address 0x10, and input registers DI12 to DI15.
(3) During write operation, be sure to input "0" to DI8 to DI11 of modulation setting registers.
(4) The data written to PI0 to PI3 is output from the general-purpose I/Os.

- General-purpose I/O read settings (General-purpose I/O input → Read register → Microcontroller)

(1) To input data to general-purpose I/Os, set PIOEN to "H".
(2) The input data is saved in CCB address 0xEB and output registers DO0 to DO3.
(3) Data can be sent to the microcontroller by reading PO0 to PO3.

12. Microcontroller Interface ($\overline{\text{INT}}$, CL, CE, DI, DO)

12.1 Description of Microcontroller Interface

12.1.1 Interrupt output ($\overline{\text{INT}}$)

- Interrupts are output when a change has occurred in the PLL lock status or output data information.
- Interrupt output consists of the register for selecting the interrupt source, the $\overline{\text{INT}}$ pin that outputs that state transition, and the registers that store the interrupt source data.
- Normally $\overline{\text{INT}}$ outputs "L" upon occurrence of an interrupt while "H" is output. Following "L" output, it returns to "H" according to the INTOPF setting.
- INTOPF determines whether to hold the "L" pulse for a certain period and then clear it ("H"), or to clear it at a time when the output register is read.
- The interrupt sources can be selected among the following items. Multiple sources can be selected at the same time with the contents of CCB address 0xE8 and command address 0x08. $\overline{\text{INT}}$ outputs OR calculation result of the selected interrupt sources.

$\overline{\text{INT}}$ output = (selected source 1) + (selected source 2) + ··· + (selected source n)

Table 12.1 Interrupt Source Setting Contents

No.	Command Name	Description
1	ERROR	Output when RERR pin status has changed
2	INDET	Output when input data pin status has changed (subject to oscillation amplifier operation condition)
3	FSCHG	Output when input fs calculation result has changed. (subject to oscillation amplifier condition)
4	CSRNW	Output when channel status data of first 48 bits have updated
5	UNPCM	Output when $\overline{\text{AUDIO}}$ pin status has changed
6	PCRNW	Output when burst preamble Pc has been updated
7	SLIPO	Output when data is read twice during slave setting and missing data is detected
8	EMPF	Output when emphasis information has changed

- The contents of set interrupt source are saved in output registers DO8 to DO15 of CCB address 0xEA, when the source occurs. However, for the read registers for source items 1 and 5, the each status of the RERR and $\overline{\text{AUDIO}}$ pins are output at the time of reading. Other data except for source items 1 and 5 are saved in the registers upon occurrence of an interrupt source.
- Concerning source items 2 and 3, the oscillation amplifier clock is used. Therefore, if the status is monitored even while the PLL is locked, the oscillation amplifier must be set to the continuous operation mode.
- Clearing $\overline{\text{INT}}$ at the same time of readout of an output register is carried out immediately after the output register 0xEA is set.
- The pulse width of the setting in which the $\overline{\text{INT}}$ output following the occurrence of an interrupt source is set to the "L" pulse output mode is somewhere between 1/2fs and 3/2fs for one interrupt source.

12.1.2 CCB format

- The various function settings as well as information writing and reading are performed with the microcontroller interface.
- The data format of the microcontroller interface conforms to Our original serial bus format (CCB), but three-state is employed instead of open-drain for the data output format.
- Data input/output is performed following CCB address input. For the data input/output timing, see the input/output timing chart.

Table 12.2 Relationship between Register I/O Contents and CCB Addresses

Register I/O contents	R/W	CCB address	B0	B1	B2	B3	A0	A1	A2	A3
Function setting data input	Write	0xE8	0	0	0	1	0	1	1	1
CS data input	Write	0xE9	1	0	0	1	0	1	1	1
Interrupt data output	Read	0xEA	0	1	0	1	0	1	1	1
fs data output	Read	0xEB	1	1	0	1	0	1	1	1
CS data output	Read	0xEC	0	0	1	1	0	1	1	1
Pc data output	Read	0xED	1	0	1	1	0	1	1	1

12.1.3 Data write procedure

- Input is performed in the following sequence: CCB addresses of A0 to A3 and B0 to B3, chip addresses of DI0 and DI1, command addresses of DI4 to DI7, and data of DI8 to DI15. DI2 and DI3 are reserved for the system. Input must be doing "0".
- For the chip addresses, DI0 corresponds to CAL (low-order), and DI1 to CAU (high-order). For details, see section 9.2.

12.1.4 Data read procedure

- Read data is output from DO. DO is in the high impedance state when CE is "L", and begins outputting from the rising edge of CE after output setting is established at the CCB address. DO then returns to the high impedance state at the falling edge of CE.
- If DO outputs are shared using multiple LC89057W-VF4A-E units, it is possible to set the DO outputs of the LC89057W-VF4A-E units of which data is not to be read to be always in the high impedance state with DOEN. With this setting, only the targeted outputs can be read.

12.1.5 I/O timing

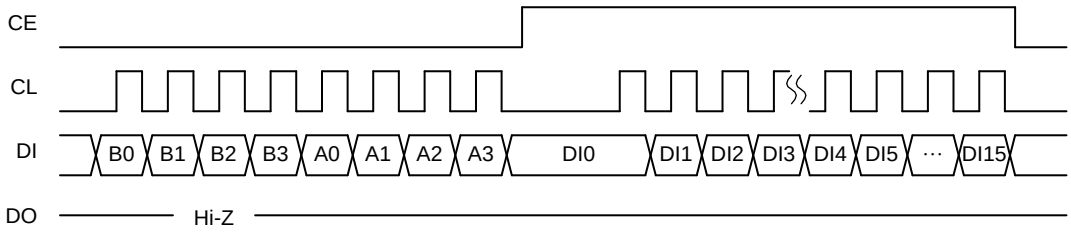


Figure 12.1 Input Timing Chart (Normal L clock)

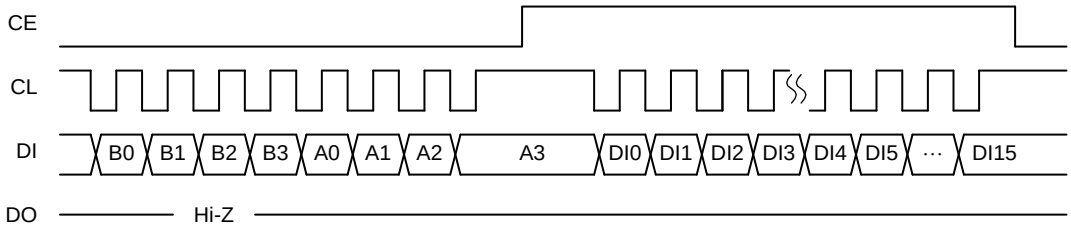


Figure 12.2 Input Timing Chart (Normal H clock)

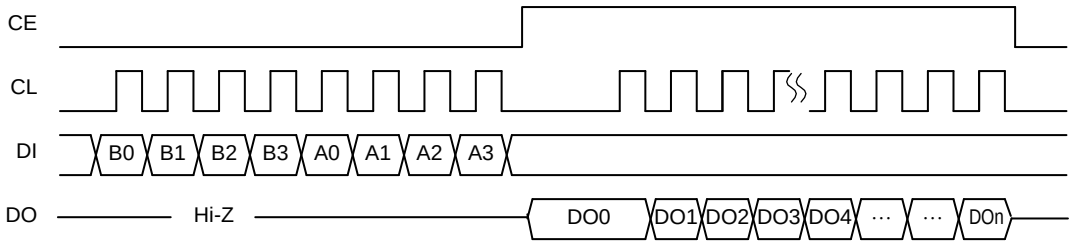


Figure 12.3 Output Timing Chart (Normal L clock)

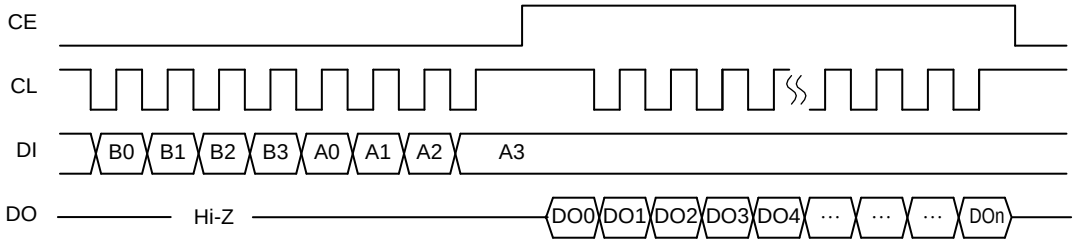


Figure 12.4 Output Timing Chart (Normal H clock, DO0 need be read with port)

12.2 Write Data

12.2.1 List of write commands

• A list of the write commands is shown below.
• To write the commands shown in the following table, set the CCB address to 0xE8.

Table 12.3 Write Register Map

Add.	Setting Items	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	All system setting	TESTM	0	TXOPR	RXOPR	INTOPF	0	DOEN	SYSRST
1	Demodulation system setting	PBSEL1	PBSEL0	FSLIM1	FSLIM0	RXMON	AOSEL	VOSEL	UOSEL
2	Master clock	AMPOPR1	AMPOPR0	EXSYNC	PLLOPR	XMSEL1	XMSEL0	XINSEL	PLLSEL
3	R system output clock	XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0
4	S system output clock	XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0
5	Source switch	0	RDTMUT	RDTSTA	RDTSEL	0	RCKSEL	OCKSEL	SELMTD
6	Data input/output	RXOFF	ROSEL2	ROSEL1	ROSEL0	ULSEL	RISEL2	RISEL1	RISEL0
7	Output format setting	SLRCKP	SBCKP	RLRCKP	RBCKP	0	OFSEL2	OFSEL1	OFSEL0
8	$\overline{\text{INT}}$source selection	EMPF	SLIPO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR
9	RERR condition setting	ERWT1	ERWT0	FSERR	RESTA	XTWT1	XTWT0	REDER	RESEL
10	Modulation system setting	P13	P12	P11	P10	0	VMODE	VISEL	UISEL
11	Modulation data setting	TCKSEL	0	TXMOD1	TXMOD0	TXMUT	TDTSEL	TWLRP	TXDFS
12	TEST	0	0	0	0	0	0	0	0
13	TEST	0	0	0	0	0	0	0	0
14	TEST	0	0	0	0	0	0	0	0
15	TEST	0	0	0	0	0	0	0	0

• The shaded parts of DI8 to DI15 in the command area are reserved bits. Input must be doing "0".
• Command addresses 0x12 to 0x15 are reserved for testing purposes. Writing to these addresses is prohibited.

12.2.2 Details of write commands

CCB address: 0xE8; Command address: 0; All system settings

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
TESTM	0	TXOPR	RXOPR	INTOPF	0	DOEN	SYSRST

SYSRST — System reset
0: Don't reset (initial value)
1: Reset circuits other than command registers

DOEN — DO pin output setting
0: Output (initial value)
1: Always high impedance state (read disabled)

INTOPF — $\overline{\text{INT}}$ pin output setting
0: Output "L" level during source occurrence (initial value)
1: Output "L" pulse during source occurrence

RXOPR — Setting of demodulation operation
0: Operate (initial value)
1: Stop

TXOPR — Setting of modulation operation
0: Stop (initial value)
1: Operate

TESTM — Test mode setting
0: Normal operation (initial value)
1: Enter test mode

• When reset by SYSRST is done or the demodulation is set to stop with RXOPR, RBCK and SBCK output "L", and RLRCK and SLRCK output "H".

CCB address: 0xE8; Command address: 1; Demodulation function: System setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
PBSEL1	PBSEL0	FSLIM1	FSLIM0	RXMON	AOSEL	VOSEL	UOSEL

UOSEL — EMPHA/UO/CO pin setting (When PBSEL1 is set to 0.)
0: EMPHA emphasis output (initial value)
1: UO user data output

VOSEL — $\overline{\text{AUDIO}}$/VO pin setting
0: $\overline{\text{AUDIO}}$ channel status bit 1 output (initial value)
1: VO validity flag output

AOSEL — Output contents at the time of setting $\overline{\text{AUDIO}}$ is set with $\overline{\text{AUDIO}}$/VO pin
0: only output channel status bit 1 (initial value)
1: output channel status bit 1, IEC61937 or DTS-CD/LD detection flag

RXMON — Setting of digital data input status monitoring
0: Don't monitor data input status (initial value)
1: Monitor data input status

FSLIM [1:0] — Setting of sampling frequency reception range for input digital data signal
00: No limit (initial value)
01: fs ≤ 96kHz
10: fs ≤ 48kHz
11: Reserved

PBSEL [1:0] — $\overline{\text{CKST}}$/PB pin setting
00: signal output of switching transition term of $\overline{\text{CKST}}$ clock (initial value)
01: Preamble B synchronization signal output with PB, DIT function
10: Preamble B synchronization signal output with PB, DIR function
11: Reserved

- In case of setting with PBSEL at 1, terminal of EMPHA/UO/CO will be Channel status data output terminal CO and the setting for UOSEL is impossible. In case of setting with PBSEL at 0, the setting for EMPHA/UO/CO terminal follows the setting for UOSEL.
- The setting of AOSEL comes into effect in the case that the bit 1 output of channel status is selected with VOSEL. In the case that 1 is selected with AOSEL, $\overline{\text{AUDIO}}$/VO terminal output high level, when either channel status bit 1 or IEC61937, non-PCM synchronous signal is detected.

CCB address: 0xE8; Command address: 2; Demodulation function: Master clock setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
AMPOPR1	AMPOPR0	EXSYNC	PLLOPR	XMSEL1	XMSEL0	XINSEL	PLLSEL

PLLSEL — PLL lock frequency setting
0: 512fs (fs ≤ 96kHz commend) (initial value)
1: 256fs

XINSEL — XIN input frequency setting
0: 12.288MHz (initial value)
1: 24.576MHz

XMSEL [1:0] — XMCK output frequency setting
00: 1/1 of XIN input frequency (initial value)
01: 1/2 of XIN input frequency
10: Reserved
11: Muted

PLLOPR — PLL (VCO) operation setting
0: Operate (initial value)
1: Stop

EXSYNC — Setting of PLL unused demodulation (external synchronization)
0: PLL used normal operation (initial value)
1: PLL unused external synchronization operation (supply 256fs clock to TMCK)

AMPOPR [1:0] — Oscillation amplifier operation setting
00: Automatic stopping of oscillation amplifier while PLL is locked (initial value)
01: Permanent continuous operation
10: Reserved
11: Stop

- If the PLL is stopped with PLLOPR while the PLL is locked, the output clocks are all muted and this muted status continues even if the PLL is unlocked.
- If the permanent continuous operation is set with AMPOPR[1:0] while the PLL is locked, RERR goes to into the error status once. It is possible to set the operation with maintaining the RERR status, if a setting with which even a changed fs is not regarded as an error due to the PLL status is made with FSERR.
- When an automatic stop mode of the oscillation amplifier is set with AMPOPR[1:0], and if the input fs changes within the PLL capture range and no lock error occurs, fs is not calculated with the oscillation amplifier stopped. For this reason, the input data fs and the fs calculation result may not be identical. However, if the channel status fs information is rewritten in line with input data changes, this information is reflected to the error flag and fs calculation of the input data is carried out. Since the fs calculation is always done when the oscillation amplifier is set to the permanent continuous operation mode, fs changes are always reflected to the error flag.

CCB address: 0xE8; Command address: 3; Demodulation function: R system output clock setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	1	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0

PRSEL [1:0] Setting of RMCK output frequency while PLL is locked
00: 1/2 of PLLSEL setting frequency (initial value)
01: 1/1 of PLLSEL setting frequency
10: 1/4 of PLLSEL setting frequency
11: Muted

XRSEL [1:0] Setting of RMCK output frequency during XIN source
00: 1/1 of XINSEL setting frequency (initial value)
01: 1/2 of XINSEL setting frequency
10: 1/4 of XINSEL setting frequency
11: Muted

XRBCK [1:0] Setting of RBCK output frequency during XIN source
00: 3.072MHz output (initial value)
01: 6.144MHz output
10: 12.288MHz output
11: Muted

XRLRCK [1:0] Setting of RLRCK output frequency during XIN source
00: 48kHz output (initial value)
01: 96kHz output
10: 192kHz output
11: Muted

• If the RMCK frequency is set lower than RBCK when the XIN source is used, 3.072MHz is output from RBCK. This also applies to SBCK.

CCB address: 0xE8; Command address: 4; Demodulation function: S system output clock setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0

PSBCK [1:0] Setting of SBCK frequency while PLL is locked
00: 64fs output (initial value)
01: 128fs output
10: 32fs output
11: Muted

PSLRCK [1:0] Setting of SLRCK frequency while PLL is locked
00: fs output (initial value)
01: 2fs output
10: fs/2 output
11: Muted

XSBCK [1:0] Setting of SBCK frequency during XIN source
00: 3.072MHz output (initial value)
01: 6.144MHz output
10: 12.288MHz output
11: Muted

XSLRCK [1:0] SLRCK output frequency setting during XIN source
00: 48kHz output (initial value)
01: 96kHz output
10: 192kHz output
11: Muted

CCB address: 0xE8; Command address: 5; Demodulation function: Clock source; RDATA output setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	RDTMUT	RDTSTA	RDTSEL	0	RCKSEL	OCKSEL	SELMTD

SELMTD — Setting of output clock source switching method
0: Switch R system and S system simultaneously according to OCKSEL (initial value)
1: Switch R system according to RCKSEL and fix S system to XIN source

OCKSEL — Clock source setting when SELMTD = 0
0: Use XIN clock as source while PLL is unlocked (initial value)
1: Use XIN clock as source regardless of PLL status

RCKSEL — Clock source setting when SELMTD = 1
0: Use XIN clock as source while PLL is unlocked (initial value)
1: Use XIN clock as source regardless of PLL status

RDTSEL — RDATA output setting while PLL is unlocked
0: Output SDIN data while PLL is unlocked (initial value)
1. Mute while PLL is unlocked

RDTSTA — RDATA output setting
0: According to RDTSEL (initial value)
1: Output SDIN input data regardless of PLL status

RDTMUT — RDATA mute setting
0: Output data selected with RDTSEL
1: Muted

- When the oscillation amplifier is set to the permanent continuous operation mode with AMPOPR[1:0] or fs changes are set not to be reflected to the error flag with FSERR, OCKSEL and RCKSEL can switch the clock source while maintaining the RERR status. However, if none of these settings is made, RERR outputs an error once when switching occurs.
- To input data to SDIN, select a clock synchronized with the SDIN input data.
- The XIN source can be switched while maintaining the PLL locked status. However, since switching between clock and data output can be set independently, it is recommended to select mute or SDIN data for the output data when XIN source is switched.
- If the oscillation amplifier is set to stop automatically when the PLL gets locked, XIN source switching from the PLL locked status is executed after the oscillation is stabilized. Moreover, switching of output data at this time is subject to XIN source switching.

CCB address: 0xE8; Command address: 6; Demodulation function: Digital data input/output port setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
RXOFF	ROSEL2	ROSEL1	ROSEL0	ULSEL	RISEL2	RISEL1	RISEL0

RISEL [2:0] Data demodulation input pin setting
000: RX0 selection (initial value)
001: RX1 selection
010: RX2 selection
011: RX3 selection
100: RX4 selection (However, VI input is performed when VISEL is set.)
101: RX5 selection (However, UI input is performed when UISEL is set.)
110: RX6 selection
111: Modulation function output (TXO output data) selection

ULSEL Setting of input pin via PLL unlock
0: Normal setting (initial value)
1: Setting of input data switching via PLL unlock

ROSEL [2:0] RXOUT output data setting
000: RX0 input data (initial value)
001: RX1 input data
010: RX2 input data
011: RX3 input data
100: RX4 input data
101: RX5/VI input data
110: RX6/UI input data
111: Modulation function output (TXO output data) selection

RXOFF Setting of RXOUT output status
0: ROSEL[2:0] selection data output (initial value)
1: "L" fixed output

• ULSEL can be set when the oscillation amplifier is set to the permanent continuous operation mode with AMPOPR[1:0]. ULSEL does not work correctly when the oscillation amplifier is stopped.

CCB address; 0xE8; Command address: 7; Demodulation function: Output data format setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	1	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
SLRCKP	SBCKP	RLRCKP	RBCKP	0	OFSEL2	OFSEL1	OFSEL0

OFSEL [2:0] Audio data output format setting
000: I^2S data output (initial value)
001: MSB-first left-justification data output
010: 24 bits MSB-first right-justification data output (master mode only)
011: 20 bits MSB-first right-justification data output (master mode only)
100: 16 bits MSB-first right-justification data output (master mode only)
101: Reserved
110: Reserved
111: Reserved

RBCKP RBCK output polarity setting
0: Falling RDATA data change (initial value)
1: Rising RDATA data change

RLRCKP RLRCK output polarity setting
0: "L" period: L-channel data; "H" period: R-channel data (initial value)
1: "L" period: R-channel data; "H" period: L-channel data

SBCKP SBCK output polarity setting
0: Falling RDATA data change (initial value)
1: Rising RDATA data change

SLRCKP SLRCK output polarity setting
0: "L" period: L-channel data; "H" period: R-channel data (initial value)
1: "L" period: R-channel data; "H" period: L-channel data

• The data output format and RLRCK output polarity could be set independently. Set the RLRCH polarity in line with each data output format.

CCB address: 0xE8; Command address: 8; Demodulation function: $\overline{\text{INT}}$ output contents setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
EMPF	SLIPO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR

ERROR
RERR signal output setting
0: Don't output (initial value)
1: Output RERR pin status change

INDET
Input data detection output setting
0: Don't output (initial value)
1: Output input data pin status change

FSCHG
Setting of updated flag output of PLL lock frequency calculation result
0: Don't output (initial value)
1: Output updated flag of PLL lock frequency calculation result

CSRNW
Output setting for updated flag of first 48-bit channel status data
0: Don't output (initial value)
1: Output update flag of first 48-bit channel status data

UNPCM
Output setting for change flag of non-PCM data detection
0: Don't output (initial value)
1: Output $\overline{\text{AUDIO}}$ pin status change

PCRNW
Output setting for updated flag of burst preamble Pc
0: Don't output (initial value)
1: Output updated flag of burst preamble Pc

SLIPO
Output setting of slip signal during slave operation
0: Don't output (initial value)
1: Output duplicate reading and a detection flag for missing of data output

EMPF
Output setting of emphasis detection flag
0: Don't output (initial value)
1: Output emphasis detection flag

- The channel status update flag compares the first 48 bits of data of the previous block with those of the current block. If these data are identical, it outputs a flag, considering the data has been updated.
- The burst preamble Pc update flag also compares the 16 bits of data of the previous block with those of the current data. If they are identical, an update flag is output.

CCB address: 0xE8, Command address: 9; Demodulation function: RERR output setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
ERWT1	ERWT0	FSERR	RESTA	XTWT1	XTWT0	REDER	RESEL

RESEL — RERR output contents setting
0: PLL lock error or data error (initial value)
1: PLL lock error or data error or non-PCM data

REDER — Setting of parity error flag output within 8 times in a row
0: Output only when non-PCM data is recognized (initial value)
1: Output only during sub-frame for which error was generated

XTWT [1:0] — Setting of clock switch wait time after PLL is unlocked
00: Clock switching after approx. 200µs from when oscillation amplifier starts (initial value)
01: Clock switching after approx. 100µs from when oscillation amplifier starts
10: Clock switching after approx. 50µs from when oscillation amplifier starts
11: Clock switching after PLL is unlocked

RESTA — RERR output condition setting
0: Output PLL status all the time (Output PLL status even during XIN source) (initial status)
1: Forcibly output error (Set "H" to RERR forcibly)

FSERR — Setting of error flag output condition according to fs change
0: Reflect fs changes to error flag (initial value)
1: Don't reflect fs changes to error flag

ERWT [1:0] — Setting of RERR wait time after PLL is locked
00: Cancel error after preamble B is counted 3 (initial value)
01: Cancel error after preamble B is counted 24
10: Cancel error after preamble B is counted 12
11: Cancel error after preamble B is counted 6

- For Non-PCM data, the data defined with AOSEL is reflected. In other words, it is identical to the detected data output to $\overline{\text{AUDIO}}$.
- Output data is muted if an error occurs due to non-PCM data with RESEL.
- The RESTA setting is not reflected to the output pins of data and clock.
- For FSERR, the fs calculation result obtained while the oscillation amplifier is stopped is not reflected. In this case, fs changes consist of only channel status fs information.
- ERWT[1:0] defines the interval of time for RERR to output error cancellation ("L") after PLL is locked. Since demodulated audio data is output after RERR cancels an error, you need to change this setting if the situation that the head of data is missing is a problem.

CCB address: 0xE8; Command address: 10; Modulation function: System setting, general-purpose I/O data input

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
PI3	PI2	PI1	PI0	0	VMODE	VISEL	UISEL

UISEL — RX6/UI pin setting
0: Input RX6 demodulation function data (initial value)
1: Input UI modulation function user data

VISEL — RX5/VI pin setting
0: Input RX5 demodulation function data (initial value)
1: Input VI modulation function validity flag

VMODE — Modulation function V flag setting
0: Write 0 (initial value)
1: Write 1

PI0 — Data input when general-purpose I/O PIO0 output is set
0: Output L (initial value)
1: Output H

PI1 — Data input when general-purpose I/O PIO1 output is set
0: Output L (initial value)
1: Output H

PI2 — Data input when general-purpose I/O PIO2 output is set
0: Output L (initial value)
1: Output H

PI3 — Data input when general-purpose I/O PIO3 output is set
0: Output L (initial value)
1: Output H

• When you use general-purpose I/O PIO0 to PIO3 as output, set PIOEN to "L".

CCB address: 0xE8; Command address: 11; Modulation function: Digital audio input/output setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	1	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
TCKSEL	0	TXMOD1	TXMOD0	TXMUT	TDTSEL	TXLRP	TXDFS

TXDFS — TDATA input data format setting
0: I^2S data input (initial value)
1: MSB-first left-justification data input

TXLRP — Setting of TLRCK input clock polarity
0: "L" period: L-channel data; "H" period: R-channel data (initial value)
1: "L" period: R-channel data; "H" period: L-channel data

TDTSEL — Input data setting
0: TDATA input data (initial value)
1: SDIN input data

TXMUT — TXO output setting
0: modulation data output (initial value)
1: "L" fixed output

TXMOD [1:0] — Mode setting
00: Normal operation (L-channel, R-channel stereo mode) (initial value)
01: L-channel continuity (time-division mode)
10: R-channel continuity (time-division mode)
11: reserved

TCKSEL — TMCK input clock frequency setting
0: 256fs (initial value)
1: 128fs

• In case of inputting 256fs clock into TMCK, the falling edge of TBCK should be in synchronized with the rising edge of TMCK. Also, in case of inputting 128fs clock into TMCK, the falling edge of TBCK is in synchronized with the falling of TMCK.

12.2.3 Channel status data write

- For channel status data write with the modulation function, set the CCB address to 0xE9.
- DI0 to DI7 are not channel status bits. Be sure to input a chip address to DI0 and DI1. Input "0" to DI2, DI3, and DI7 because they are reserved by the system. Write length of the channel status data is determined with DI4 to DI6. This setting is possible up to 48 bits in units of 8 bits.
- After CE rises, input a clock combined DI0 to DI7 and write data length to CL clock to make CE “L”. For example, if you write data up to the bit 15 by DI4 to DI6, CL must be 24 clocks while CE is rising. If this setting goes wrong, correct writing is not expected.
- Input data is written from preamble B where CE has become "L".

Table 12.3 Relation between Setting Register of Input Data Length and Data Length

DI6	DI5	DI4	Feasible Data Range for Input
0	0	0	Bit 0 to bit 7
0	0	1	Bit 0 to bit 15
0	1	0	Bit 0 to bit 23
0	1	1	Bit 0 to bit 31

DI6	DI5	DI4	Feasible Data Range for Input
1	0	0	Bit 0 to bit 39
1	0	1	Bit 0 to bit 47
1	1	0	Reserved
1	1	1	Reserved

Table 12.4 Input Setting -Setting of Modulation Function Channel Status Data- (CCB address : 0xE9)

Register	Bit No.	Description
DI0	CAL	Lower chip address
DI1	CAU	Higher chip address
DI2	0	Reserved
DI3	0	
DI4	0	Data length setting
DI5	0	
DI6	0	
DI7	0	Reserved
DI8	Bit 0	Application
DI9	Bit 1	Control
DI10	Bit 2	
DI11	Bit 3	
DI12	Bit 4	
DI13	Bit 5	
DI14	Bit 6	Not defined
DI15	Bit 7	
DI16	Bit 8	Category code
DI17	Bit 9	
DI18	Bit 10	
DI19	Bit 11	
DI20	Bit 12	
DI21	Bit 13	
DI22	Bit 14	
DI23	Bit 15	
DI24	Bit 16	Source number
DI25	Bit 17	
DI26	Bit 18	
DI27	Bit 19	

Register	Bit No.	Description
DI28	Bit 20	Channel number
DI29	Bit 21	
DI30	Bit 22	
DI31	Bit 23	
DI32	Bit 24	Sampling frequency
DI33	Bit 25	
DI34	Bit 26	
DI35	Bit 27	
DI36	Bit 28	Clock accuracy
DI37	Bit 29	
DI38	Bit 30	Not defined
DI39	Bit 31	
DI40	Bit 32	Word length
DI41	Bit 33	
DI42	Bit 34	
DI43	Bit 35	
DI44	Bit 36	Not defined
DI45	Bit 37	
DI46	Bit 38	
DI47	Bit 39	
DI48	Bit 40	
DI49	Bit 41	
DI50	Bit 42	
DI51	Bit 43	
DI52	Bit 44	
DI53	Bit 45	
DI54	Bit 46	
DI55	Bit 47	

12.3 Read Data

12.3.1 List of read commands

• It is possible to read the following items.
  – Monitor output of digital data input status
  – Interrupt data output
  – Output of general-purpose I/O input data
  – Output of fs calculation result and fs counter data (8 bits)
  – Output of first 48 bits of channel status
  – Output of burst preamble Pc data
• CCB address 0xEB and output registers DO16 to DO23 are for testing.

Table 12.5 Read Register Map

Read Register Name	0xEA	0xEB	0xEC	0xED
DO0	RXDET0	PO0	CS bit 0	Pc bit 0
DO1	RXDET1	PO1	CS bit 1	Pc bit 1
DO2	RXDET2	PO2	CS bit 2	Pc bit 2
DO3	RXDET3	PO3	CS bit 3	Pc bit 3
DO4	RXDET4	FSC0	CS bit 4	Pc bit 4
DO5	RXDET5	FSC1	CS bit 5	Pc bit 5
DO6	RXDET6	FSC2	CS bit 6	Pc bit 6
DO7	RXDET7	FSC3	CS bit 7	Pc bit 7
DO8	OERROR	FSDAT0	CS bit 8	Pc bit 8
DO9	OINDET	FSDAT1	CS bit 9	Pc bit 9
DO10	OFSCHG	FSDAT2	CS bit 10	Pc bit 10
DO11	OCSRNW	FSDAT3	CS bit 11	Pc bit 11
DO12	OUNPCM	FSDAT4	CS bit 12	Pc bit 12
DO13	OPCRNW	FSDAT5	CS bit 13	Pc bit 13
DO14	OSLIPO	FSDAT6	CS bit 14	Pc bit 14
DO15	OEMPF	FSDAT7	CS bit 15	Pc bit 15
DO16	CSBITI	TEST0	CS bit 16	–
DO17	IEC1937	TEST1	CS bit 17	–
DO18	DTS51	TEST2	CS bit 18	–
DO19	DTSES	TEST3	CS bit 19	–
DO20	F0512	TSET4	CS bit 20	–
DO21	F1024	TEST5	CS bit 21	–
DO22	F2048	TEST6	CS bit 22	–
DO23	F4096	TEST7	CS bit 23	–
DO24	–	–	CS bit 24	–
…	–	–	…	–
DO46	–	–	CS bit 46	–
DO47	–	–	CS bit 47	–

12.3.2 Read register 1 (input detection, interrupt flag, IEC61937 flag, DTS-CD flag)

CCB address: 0xEA, contents of read register output

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
RXDET7	RXDET6	RXDET5	RXDET4	RXDET3	RXDET2	RXDET1	RXDET0

RXDET0 RX0 input detection
0: No input data in RX0
1: Input data exist in RX0

RXDET1 RX1 input detection
0: No input data in RX1
1: Input data exist in RX1

RXDET2 RX2 input detection
0: No input data in RX2
1: Input data exist in RX2

RXDET3 RX3 input detection
0: No input data in RX3
1: Input data exist in RX3

RXDET4 RX4 input detection
0: No input data in RX4
1: Input data exist in RX4

RXDET5 RX5 input detection
0: No input data in RX5
1: Input data exist in RX5

RXDET6 RX6 input detection
0: No input data in RX6
1: Input data exist in RX6

RXDET7 Data detection of modulation function output TXO
0: No data in modulation function output TXO
1: Data exist in modulation function output TXO

• For readout of RXDET[7:0], RXMON must be set to "H" beforehand.

CCB address; 0xEA; Contents of Read register output

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8
OEMPF	OSLIPO	OPCRNW	OUNPCM	OCSRNW	OFSCHG	OINDET	OERROR

OERROR
RERR output (Output status during readout)
0: No transfer error while PLL is locked
1: Transfer error exist or PLL is unlocked

OINDET
Status change of data input pin (clear after readout)
0: No change in status of data input pin
1: Change exists in status of data input pin

OFSCHG
Result of updating input fs calculation (clear after readout)
0: No update of input fs calculation
1: Input fs calculation is updated

OCSRNW
Update result of first 48 bits channel status (clear after readout)
0: Not updated
1: Updated

OUNPCM
$\overline{\text{AUDIO}}$ output (output of status during readout)
0: Non-PCM signal not detected
1: Non-PCM signal detected

OPCRNW
Update result of burst preamble Pc (clear after readout)
0: Not updated
1: Updated

OSLIPO
Detection of duplicate reading and missing data during slave operation (clear after readout)
0: Not detected
1: duplicate reading and missing data detected

OEMPF
Channel status emphasis detection (output of status during readout)
0: No pre-emphasis
1: 50/15μs pre-emphasis exists

• Concerning OERROR and OUNPCM, the status of RERR and $\overline{\text{AUDIO}}$ that are subject to RESEL and AOSEL setting are read regardless of the $\overline{\text{INT}}$output setting.

CCB address: 0xEA; Contents of read register output

DO23	DO22	DO21	DO20	DO19	DO18	DO17	DO16
F4096	F2048	F1024	F0512	DTSES	DTS51	IEC1937	CSBIT1

CSBIT1 — Channel status bit 1 detection
0: PCM
1: Non-PCM

IEC1937 — IEC61937 burst preamble detection
0: Pa, Pb not detected
1: Pa, Pb detected

DTS51 — DTS-CD/LD 5.1 channel sync signal detection
0: DTS-CD/LD sync signal not detected
1: DTS-CD/LD sync signal detected

DTSES — DTS ES-CD/LD 6.1 channel sync signal detection
0: DTS ES-CD/LD sync signal not detected
1: DTS ES-CD/LD sync signal detected

F0512 — DTS-CD/LD IEC60958 frame interval
0: Sync signal is not 512 nor 1024 frame interval
1: Sync signal is 512 or 1024 frame interval

F1024 — DTS-CD/LD IEC60958 frame interval
0: Sync signal is not 1024 nor 2048 frame interval
1: Sync signal is 1024 or 2048 frame interval

F2048 — DTS-CD/LD IEC60958 frame interval
0: Sync signal is not 2048 nor 4096 frame interval
1: Sync signal is 2048 or 4096 frame interval

F4096 — DTS-CD/LD IEC60958 frame interval
0: Sync signal is not 4096 frame interval
1: Sync signal is 4096 frame interval

12.3.3 Read register 2 (Contents of general-purpose I/O input, fs calculation result, fs counter data)

CCB address: 0xEB, Contents of read register output

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
FSC3	FSC2	FSC1	FSC0	PO3	PO2	PO1	PO0

PO0 Contents of read data output when general-purpose I/O PO0 input is set
0: PIO0 input = "L"
1: PIO0 input = "H"

PO1 Contents of read data output when general-purpose I/O PIO1 input is set
0: PIO1 input = "L"
1: PIO1 input = "H"

PO2 Contents of read data output when general-purpose I/O PIO2 input is set
0: PIO2 input = "L"
1: PIO2 input = "H"

PO3 Contents of read data output when general-purpose I/O PIO3 input is set
0: PIO3 input = "L"
1: PIO3 input = "H"

FSC [3:0] Input data fs calculation result
"xxxx": See code table.

Table 12.6 Code Table of Input fs Calculation Result (Ta = 25°C, AV_{DD} = DV_{DD} = 3.3 V)

FSC3	FSC2	FSC1	FSC0	Target Frequency	Calculation Range (Design Value)
0	0	0	0	Out of range	–
0	0	0	1	–	–
0	0	1	0	–	–
0	0	1	1	–	–
0	1	0	0	16kHz	15.4k to 16.6kHz
0	1	0	1	22.05kHz	21.2k to 22.9kHz
0	1	1	0	24kHz	23.1k to 24.9kHz
0	1	1	1	32kHz	30.8k to 33.3kHz
1	0	0	0	44.1kHz	42.4k to 45.8kHz
1	0	0	1	48kHz	46.2k to 49.9kHz
1	0	1	0	64kHz	61.5k to 66.7kHz
1	0	1	1	88.2kHz	85.4k to 91.7kHz
1	1	0	0	96kHz	93.1k to 100.7kHz
1	1	0	1	128kHz	122.9k to 133.5kHz
1	1	1	0	176.4kHz	170.7k to 180.7kHz
1	1	1	1	192kHz	186.2k to 198.1kHz

CCB address: 0xEB; Contents of Read register output

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8
FSDAT7	FSDAT6	FSDAT5	FSDAT4	FSDAT3	FSDAT2	FSDAT1	FSDAT0

FSDAT [7:0] fs counter data output

• FSDAT [7:0] is the fs calculation counter value. The data length is 8 bits, FSDAT0 is LSB, and FSDAT7 is MSB.
• The relation between the count value and fs is expressed by the following equation.
fs = 6144/FSDAT (kHz)
• Since fs is calculated with 6.144MHz-clock, the calculation accuracy is subject to this clock.
• The calculation counter value is 8-bit output, so the fs capable of calculating is 24kHz or higher.

12.3.4 Read register 3 (readout of first 48 bits of channel status)

• The first 48 bits of channel status can be read with the demodulation function.
• The readout channel status data is output with LSB first.
• For readout, set the CCB address to 0xEC.
• The channel status data cannot be updated after the CCB address is set.
• The relation between the read registers and the channel status data is shown below.

Table 12.7 Read Registers of First 48 bits of Channel Status

Register	Bit No.	Contents
DO0	Bit 0	Application
DO1	Bit 1	Control
DO2	Bit 2	
DO3	Bit 3	
DO4	Bit 4	
DO5	Bit 5	
DO6	Bit 6	Not defined
DO7	Bit 7	
DO8	Bit 8	Category code
DO9	Bit 9	
DO10	Bit 10	
DO11	Bit 11	
DO12	Bit 12	
DO13	Bit 13	
DO14	Bit 14	
DO15	Bit 15	
DO16	Bit 16	Source number
DO17	Bit 17	
DO18	Bit 18	
DO19	Bit 19	
DO20	Bit 20	Channel number
DO21	Bit 21	
DO22	Bit 22	
DO23	Bit 23	

Register	Bit No.	Contents
DO24	Bit 24	Sampling frequency
DO25	Bit 25	
DO26	Bit 26	
DO27	Bit 27	
DO28	Bit 28	Clock accuracy
DO29	Bit 29	
DO30	Bit 30	Not defined
DO31	Bit 31	
DO32	Bit 32	Word length
DO33	Bit 33	
DO34	Bit 34	
DO35	Bit 35	
DO36	Bit 36	Not defined
DO37	Bit 37	
DO38	Bit 38	
DO39	Bit 39	
DO40	Bit 40	
DO41	Bit 41	
DO42	Bit 42	
DO43	Bit 43	
DO44	Bit 44	
DO45	Bit 45	
DO46	Bit 46	
DO47	Bit 47	

12.3.5 Read register 4 (burst preamble Pc data)

• The burst preamble Pc data can be read with the demodulation function.
• The 16 bit-data of burst preamble Pc are output with LSB first.
• For readout, set the CCB address to OxED.
• The relation between the read register and burst preamble Pc data is shown below.

Table 12.8 Burst Preamble Pc Read Registers

Register	Bit No.	Contents
DO0	Bit 0	Data type
DO1	Bit 1	
DO2	Bit 2	
DO3	Bit 3	
DO4	Bit 4	
DO5	Bit 5	Reserved
DO6	Bit 6	
DO7	Bit 7	Error
DO8	Bit 8	Data type dependent
DO9	Bit 9	Information
DO10	Bit 10	
DO11	Bit 11	
DO12	Bit 12	
DO13	Bit 13	Bit stream number
DO14	Bit 14	
DO15	Bit 15	

12.4 Burst Preamble Pc Field

• The burst preamble Pc field is shown below.
• For the latest information, refer to official specifications.

Table 12.9 Burst Preamble Pc Field

Register	Value	Contents
DO4 to 0	0	NULL data
	1	Dolby AC-3 data
	2	Reserved
	3	Pause
	4	MPEG-1, layer 1 data
	5	MPEG-1, layer 2, 3 data, or non-extended MPEG-2
	6	Extended MPEG-2 data
	7	Reserved
	8	MPEG-2, layer 1, low sampling rate
	9	MPEG-2, layer 2, 3, low sampling rate
	10	Reserved
	11	DTS type1
	12	DTS type2
	13	DTS type3
	14	ATRAC
	15	ATRACK2/3
	16 to 26	Reserved
	27	Reserved (MPEG-4, AAC data)
	28	MPEG-2, AAC data
	29 to 31	Reserved
DO6, 5	0	Reserved (set to "0")
DO7	0	Error flag indicating effective burst payload
	1	Error flag indicating burst payload error
DO12 to 8		Data type dependent information
DO15 to 13	0	Bit stream number. (set to "0")

13. Application Example

13.1 Basic Connection Diagram

- Connect a de-coupling capacitance (0.1µF) as close as possible to the power supply pin. Use a ceramic capacitor with high-frequency characteristics for this capacitance.
- Use a capacitor with a low temperature coefficient for the PLL loop filter.

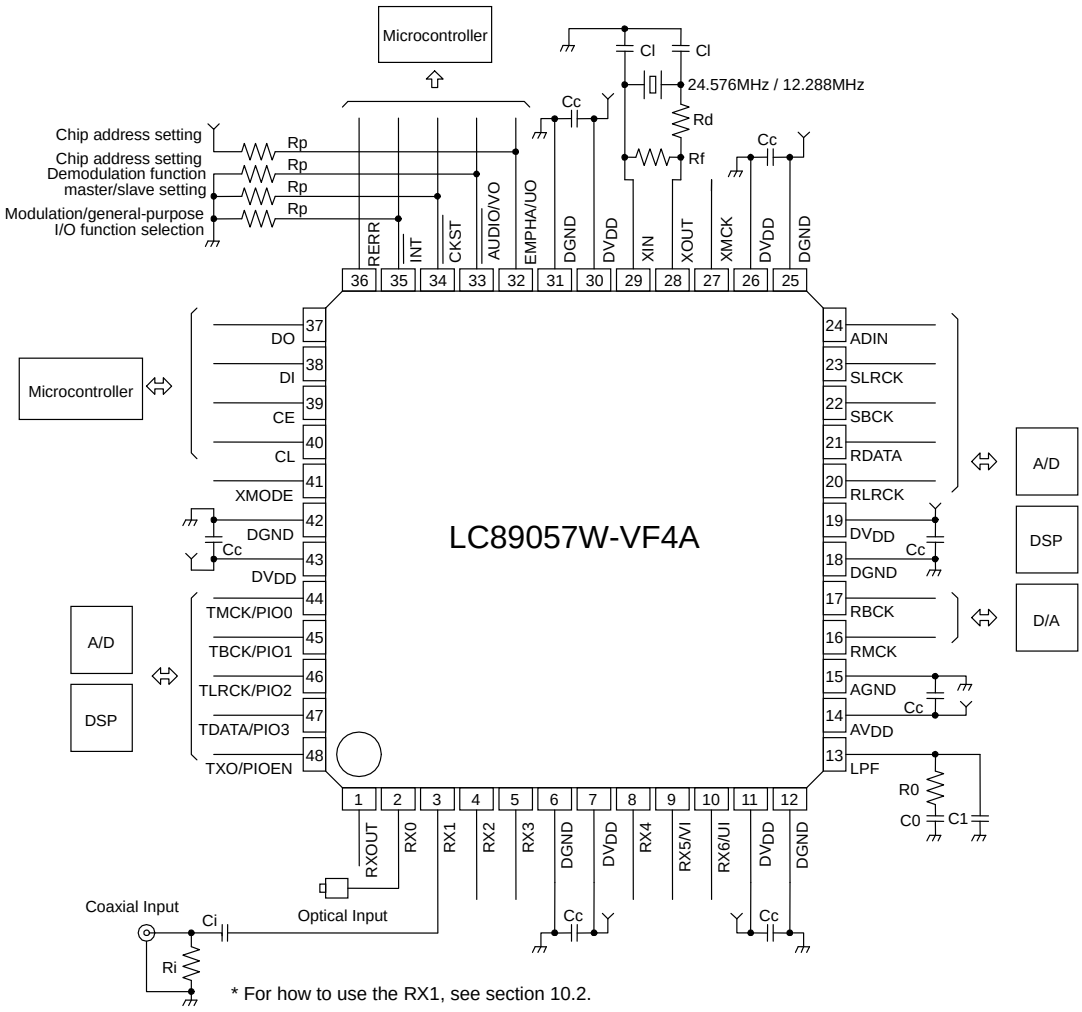


Table 13.1 Recommended Circuit Parameters (**: See Section 10.1.1)

Element Symbol	Recommended Parameter	Application	Remarks
Cc	0.1µF	Power supply de-coupling	Ceramic capacitor
Rp	10kΩ	Function setting	Pull-down/pull-up resistor
C1	1pF to 33pF	Quarts resonator load	Ceramic capacitor with NP0 characteristics
Rf	1MΩ	Oscillation amplifier feedback	
Rd	220Ω	Oscillation amplifier current limit	
Ci	0.1µF	Coaxial input DC cut	Ceramic capacitor
Ri	75Ω	Coaxial input termination	
C0	**	PLL loop filter	
C1	**	PLL loop filter	
R0	**	PLL loop filter	