Operating Conditions at Ta = 25°C,

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		13.2	V
Recommended load resistance	R_L		4	Ω
Operating voltage range	V_{CC} op		5 to 16	V
Operating load resistance range	R_L op	Under conditions where maximum ratings are not exceeded	2 to 8	Ω

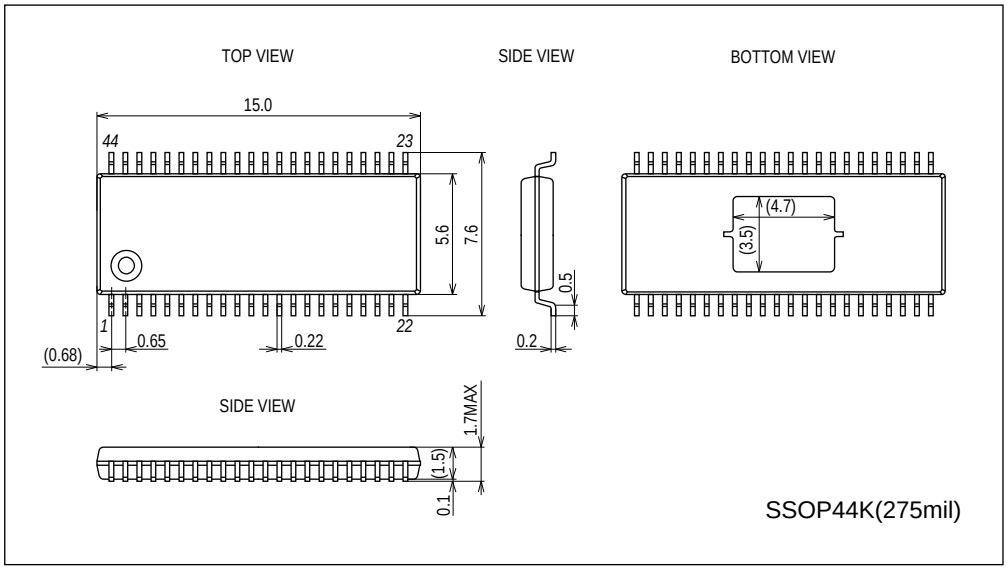
Electrical Characteristics at Ta = 25°C, V_{CC} = 13.2V, R_L = 4Ω, f = 1 kHz, Rg = 600Ω, Specified board/specified circuit

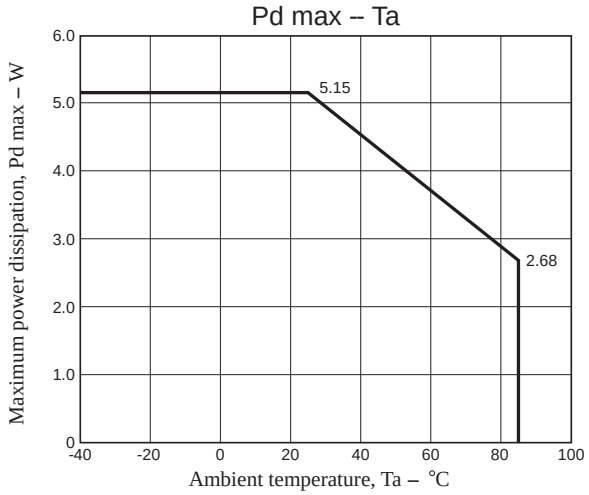
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}			65	130	mA
Voltage gain	V_G	V_O = 0dBm	43	45	47	dB
Output power	P_O1	13.2 V / 4Ω, THD = 10%	4	5		W
	P_O2	14.4 V / 4Ω, THD = 10%	5	6		W
Total harmonic distortion	THD	V_O = 2Vrms		0.1	1.0	%
Output noise voltage	V_{NO}	Rg = 0Ω, BPF = 20 Hz to 20 kHz		0.15	0.5	mV
Ripple rejection ratio	SVRR1	Rg = 0Ω, BPF = 20 Hz to 20 kHz V_R = 0dBm, f_R = 100Hz	30	40		dB
	SVRR2	Rg = 0Ω, BPF = 20 Hz to 20 kHz V_R = 0dBm, f_R = 1kHz		47		dB
Over-voltage attack	$V_{CC}X$	Rg = 0Ω		21.5		V
Starting time	t_S			0.35		s
Input resistance	R_{IN}			50		kΩ
Roll-off frequency	f_L			40		Hz
	f_H			90		kHz

Package Dimensions

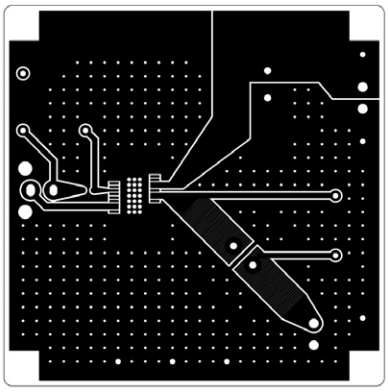
unit : mm (typ)

3333

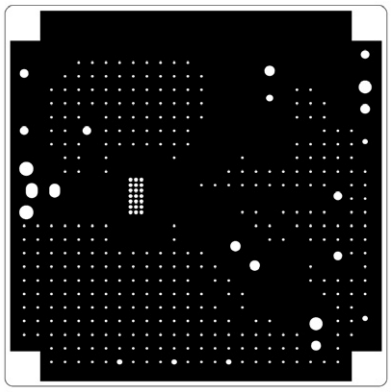




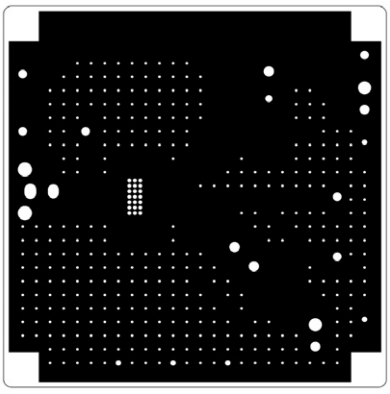
Board specifications of the Pdmax - Ta measurement
(LA4425PV specified PCB)
Size: 70mm × 70mm × 1.6mm^3 (Four layer boards)
Copper foil thickness: L1/L4=18µm, L2/L3=35µm
Materials: FR-4 (Glass cloth matrix epoxy resin)



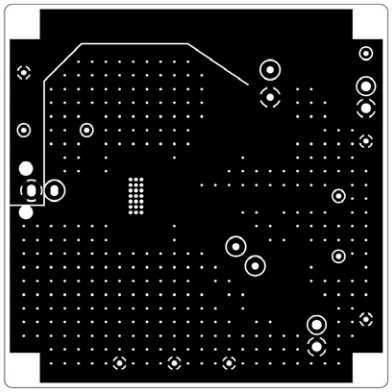
L1: Figure of copper wiring pattern



L2: Figure of copper wiring pattern



L3: Figure of copper wiring pattern

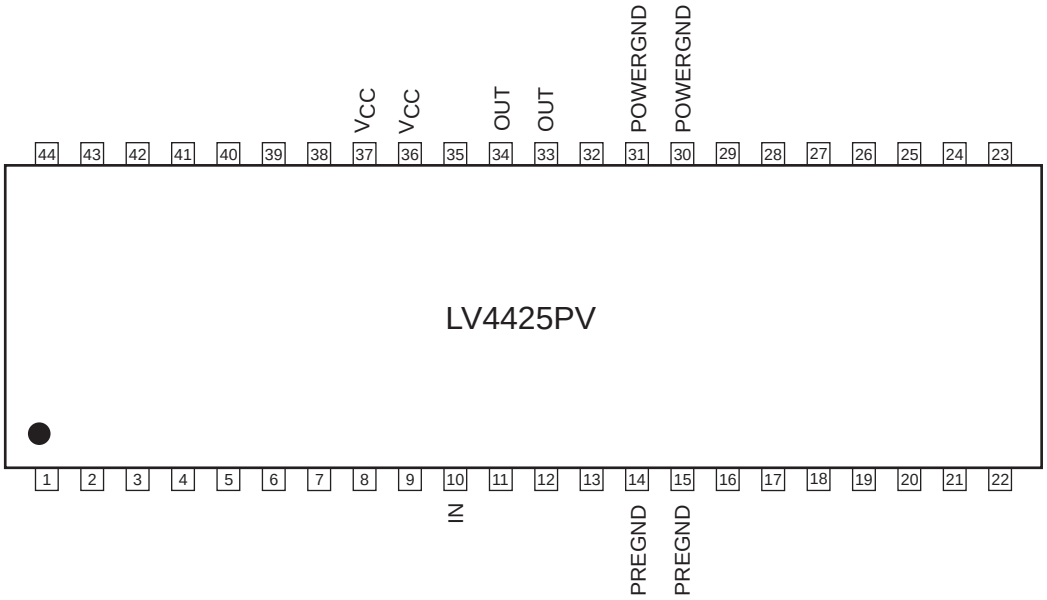


L4: Figure of copper wiring pattern

Notes:
The data for the case with the exposed die-pad substrate mounted shows the values when 95% or more of the Exposed Die-Pad is wet.

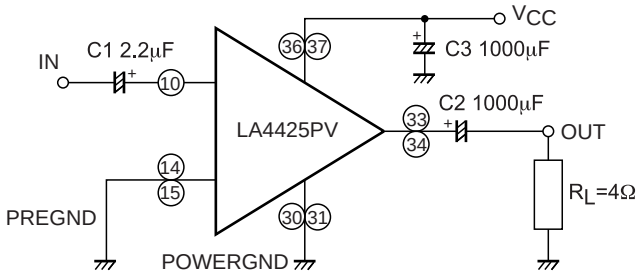
1. For the set design, employ the derating design with sufficient margin.
2. Stresses to be derated include the voltage, current, junction temperature, power loss, and mechanical stresses such as vibration, impact, and tension.
   Accordingly, the design must ensure these stresses to be as low or small as possible.
   The guideline for ordinary derating is shown below:
   (1) Maximum value 80% or less for the voltage ratings
   (2) Maximum value 80% or less for the current ratings
   (3) Maximum value 80% or less for the temperature ratings
3. After the set has been designed, be sure to verify the design with the actual product. Confirm the solder joint state and verify also the reliability of solder joint for the Exposed Die-Pad, etc. Any void or deterioration, if observed in the solder joint of these parts, causes deteriorated thermal conduction, possibly resulting in thermal destruction of IC.

Pin Assignment



- Connect exposed die pad on the back side to GND with a large pattern.
- Pins whose names are not given next to the pin numbers are all “NC pins” that are not connected to the chip inside the package, and they must not be used as relay pins.

Application Circuit Example



- On-chip overvoltage protection
- On-chip thermal protection
- On-chip pop noise reducing circuit
- On-chip output D.C. short protection

Pin Voltage at V_{CC} = 13.2V

Characteristics	Input	Pre GND	Power GND	Output	V_{CC}
Pin No.	10	14, 15	30, 31	33, 34	36, 37
Pin voltage (reference value)	(≈ $2V_{BE}$) 1.4V	0V	0V	(≈ $1/2V_{CC}$) 6.5V	(V_{CC}) 13.2V

IC Usage Notes

- Maximum ratings
  If the IC is used in the vicinity of the maximum ratings, even a slight variation in conditions may cause the maximum ratings to be exceeded, thereby leading to a breakdown.

- Printed circuit board
  When drawing the printed circuit pattern, refer to the sample printed circuit pattern. Be careful not to form a feedback loop between input and output.
  Always use both pins of the Pre GND, Power GND, OUT and V_{CC} when designing the layout.

- Exposed Die-Pad
  The exposed die pad on the back side of the IC must be connected to GND with a large pattern surface area.

- Load Resistance and Misoperation
  It should be noted that when $R_L < 2\Omega$ and V_{CC} is high, and the switch is turned "ON" when setting is for a signal (THD = 10%), the ground detector (current × voltage Schmitt circuit) operates momentarily.

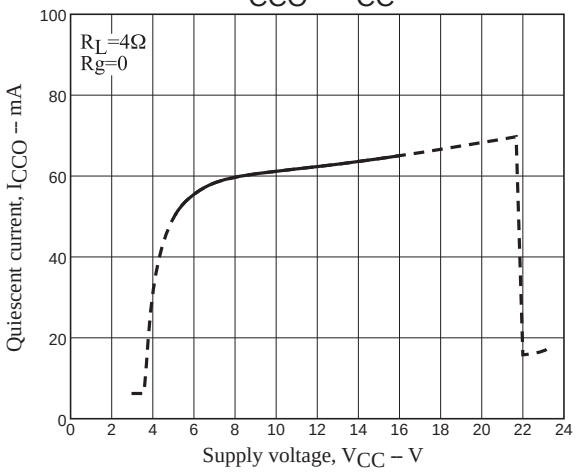
- Starting Time (t_S)
  This is set at 0.35sec/typ, but it can be made shorter by making input capacitor Ci smaller, or longer by making it larger.

- Pop noise
  The pop noise prevention circuit operates to reduce pop until Rg reaches 50kΩ. However, if Rg is left open, the charging route of input capacitor Ci is lost, so the pop noise reduction circuit stops operating and click noises become louder.

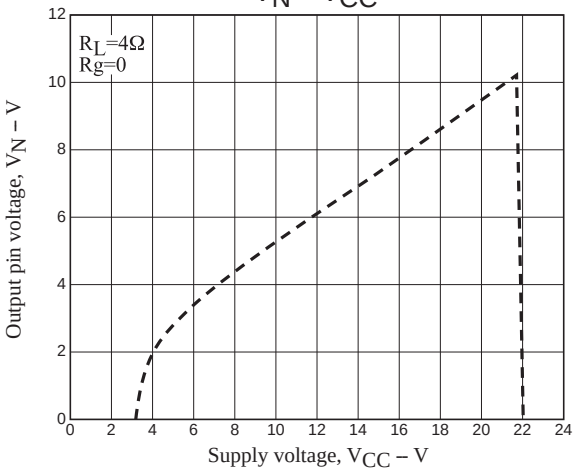
- VG/OSC
  The voltage gain is fixed at 45dB inside the IC. It is impossible to change it externally.
  Phase compensation capacitors (350pF/total) are connected between individual stages inside the IC, and the open loop gain is low. In addition, the upper and lower drives are made equivalent so that final stage current gain is adjusted, providing a measure against unwanted high-frequency parasitic oscillation peculiar to power IC's.

- BTL Connection
  Connection is impossible with IC alone.

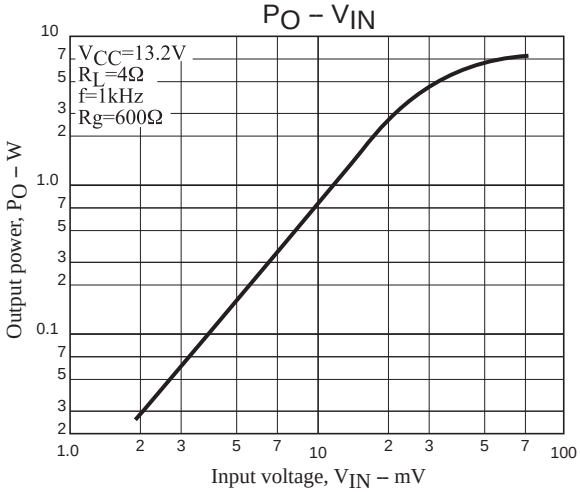
I_{CCO} – V_{CC}



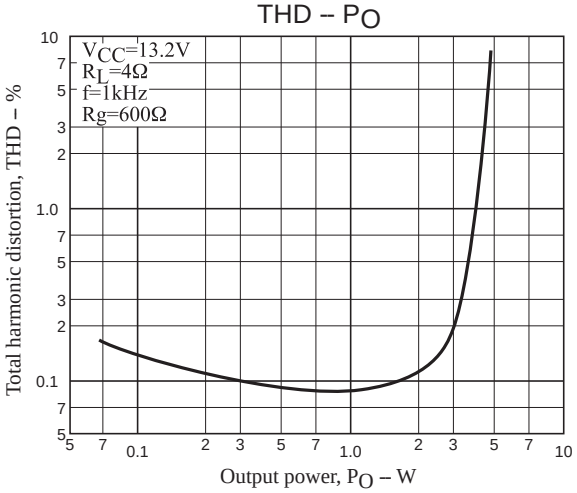
V_N – V_{CC}



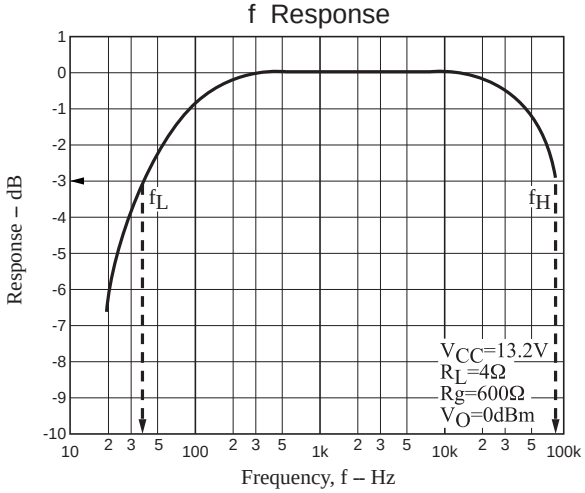
P_O – V_{IN}



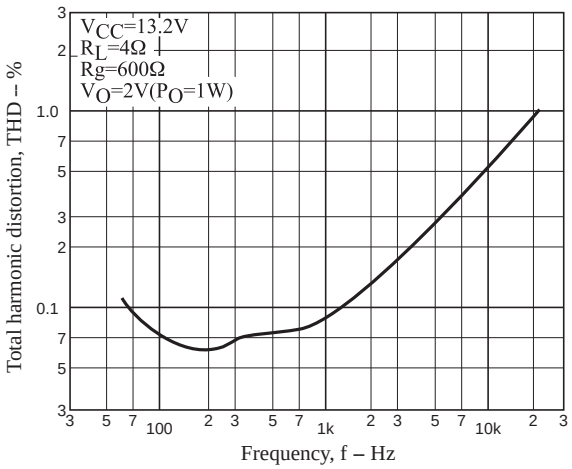
THD – P_O



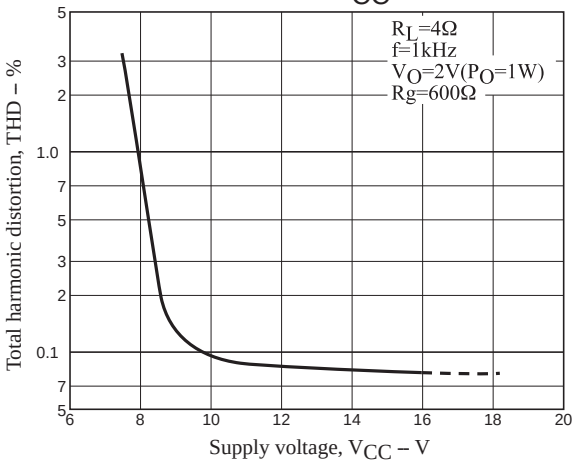
f Response



THD – f



THD – V_{CC}



P_O – V_{CC}