IS61WV51216ALL
IS61WV51216BLL
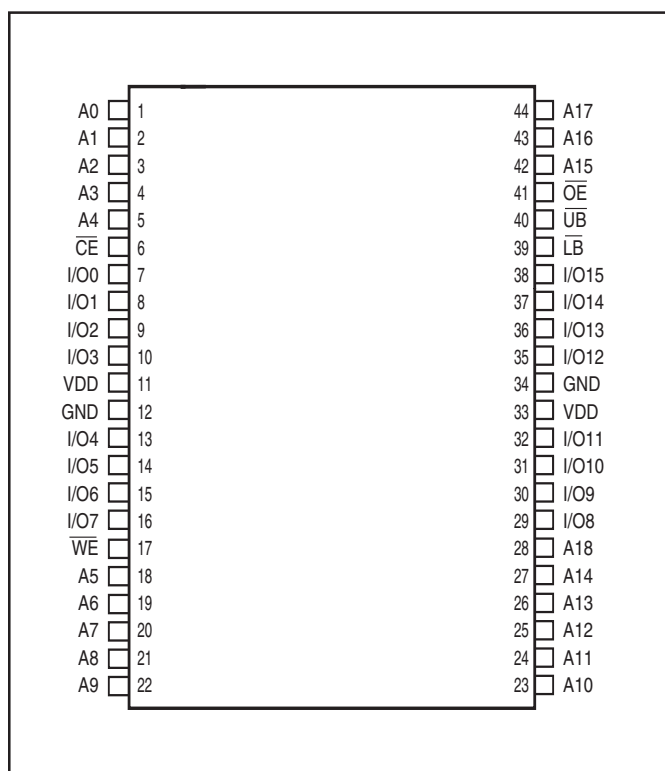# IS64WV51216BLL

ISSI®

48-pin mini BGA (9mmx11mm)

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O_8	$\overline{UB}$	A3	A4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A5	A6	I/O_1	I/O_2
D	GND	I/O_{11}	A17	A7	I/O_3	VDD
E	VDD	I/O_{12}	NC	A16	I/O_4	GND
F	I/O_{14}	I/O_{13}	A14	A15	I/O_5	I/O_6
G	I/O_{15}	NC	A12	A13	$\overline{WE}$	I/O_7
H	A18	A8	A9	A10	A11	NC

PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

PIN CONFIGURATIONS

44-Pin TSOP (Type II)

A0	1	44	A17
A1	2	43	A16
A2	3	42	A15
A3	4	41	$\overline{OE}$
A4	5	40	$\overline{UB}$
$\overline{CE}$	6	39	$\overline{LB}$
I/O0	7	38	I/O15
I/O1	8	37	I/O14
I/O2	9	36	I/O13
I/O3	10	35	I/O12
VDD	11	34	GND
GND	12	33	VDD
I/O4	13	32	I/O11
I/O5	14	31	I/O10
I/O6	15	30	I/O9
I/O7	16	29	I/O8
$\overline{WE}$	17	28	A18
A5	18	27	A14
A6	19	26	A13
A7	20	25	A12
A8	21	24	A11
A9	22	23	A10

PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
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$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	V_{DD} Current
						I/O PIN		
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to $V_{DD} + 0.5$	V
V_{DD}	V_{DD} Relates to GND	-0.3 to 4.0	V
T_{STG}	Storage Temperature	-65 to $+150$	°C
P_T	Power Dissipation	1.0	W

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{OUT} = 0V$	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A = 25°C$, f = 1 MHz, $V_{DD} = 3.3V$.

OPERATING RANGE (V$_{DD}$) (IS61WV51216ALL)

Range	Ambient Temperature	V$_{DD}$ (20 ns)
Commercial	0°C to +70°C	1.65V-2.2V
Industrial	−40°C to +85°C	1.65V-2.2V
Automotive	−40°C to +125°C	1.65V-2.2V

OPERATING RANGE (V$_{DD}$) (IS61WV51216BLL)[1]

Range	Ambient Temperature	V$_{DD}$ (8 ns)	V$_{DD}$ (10 ns)
Commercial	0°C to +70°C	3.3V ± 5%	2.4V-3.6V
Industrial	−40°C to +85°C	3.3V ± 5%	2.4V-3.6V

Note:
1. When operated in the range of 2.4V-3.6V, the device meets 10ns. When operated in the range of 3.3V ± 5%, the device meets 8ns.

OPERATING RANGE (V$_{DD}$) (IS64WV51216BLL)

Range	Ambient Temperature	V$_{DD}$ (10 ns)
Automotive	−40°C to +125°C	2.4V-3.6V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 3.3V $\pm$ 5%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.4V-3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–1	1	µA

Note:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.65V-2.2V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.65-2.2V	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.65-2.2V	—	0.2	V
V_{IH}	Input HIGH Voltage		1.65-2.2V	1.4	V_{DD} + 0.2	V
V_{IL}[1]	Input LOW Voltage		1.65-2.2V	–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{IL} (min.) = –0.3V DC; V_{IL} (min.) = –2.0V AC (pulse width < 10 ns). Not 100% tested.
V_{IH} (max.) = V_{DD} + 0.3V DC; V_{IH} (max.) = V_{DD} + 2.0V AC (pulse width < 10 ns). Not 100% tested.

AC TEST CONDITIONS (HIGH SPEED)

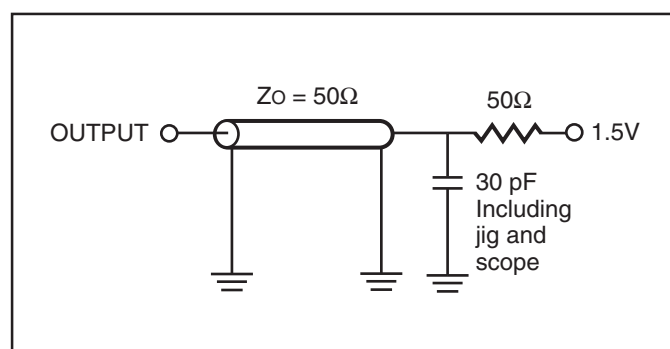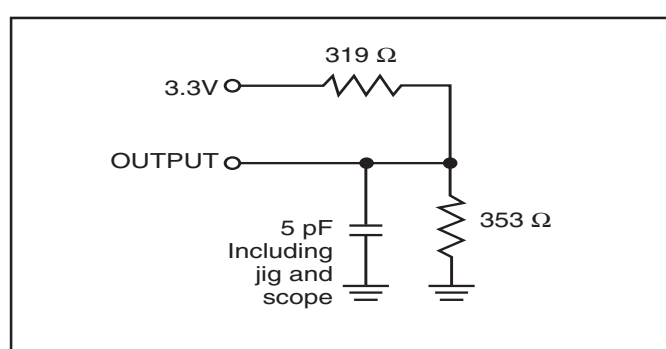| Parameter	Unit (2.4V-3.6V)	Unit (3.3V $\pm$ 5%)	Unit (1.65V-2.2V)
Input Pulse Level	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.3V	0.4V to V_{DD}-0.2V
Input Rise and Fall Times	1.5ns	1.5ns	1.5ns
Input and Output Timing and Reference Level (V_{Ref})	$V_{DD}/2$	$V_{DD}/2 + 0.05$	$V_{DD}/2$
Output Load	See Figures 1 and 2	See Figures 1 and 2	See Figures 1 and 2

AC TEST LOADS

Figure 1.

Figure 2.

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POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-8 Min.	-8 Max.	-10 Min.	-10 Max.	-20 Min.	-20 Max.	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX}	Com.	—	110	—	90	—	50	mA
			Ind.	—	115	—	95	—	60	
			Auto.	—	—	—	140	—	100	
			typ.[2]			60				
$I_{CC}1$	Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = 0	Com.	—	85	—	85	—	45	mA
			Ind.	—	90	—	90	—	55	
			Auto.	—	—	—	110	—	90	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com.	—	30	—	30	—	30	mA
			Ind.	—	35	—	35	—	35	
			Auto.	—	—	—	70	—	70	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0	Com.	—	20	—	20	—	15	mA
			Ind.	—	25	—	25	—	20	
			Auto.	—	—	—	60	—	60	
			typ.[2]			4				

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-10 Min.	-10 Max.	Unit
t_{RC}	Read Cycle Time	8	—	10	—	ns
t_{AA}	Address Access Time	—	8	—	10	ns
t_{OHA}	Output Hold Time	2.5	—	2.5	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	8	—	10	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5.5	—	6.5	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	3	—	4	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	3	0	4	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{BA}	$\overline{LB}, \overline{UB}$ Access Time	—	5.5	—	6.5	ns
t_{HZB}[2]	$\overline{LB}, \overline{UB}$ to High-Z Output	0	3	0	3	ns
t_{LZB}[2]	$\overline{LB}, \overline{UB}$ to Low-Z Output	0	—	0	—	ns
t_{PU}	Power Up Time	0	—	0	—	ns
t_{PD}	Power Down Time	—	8	—	10	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

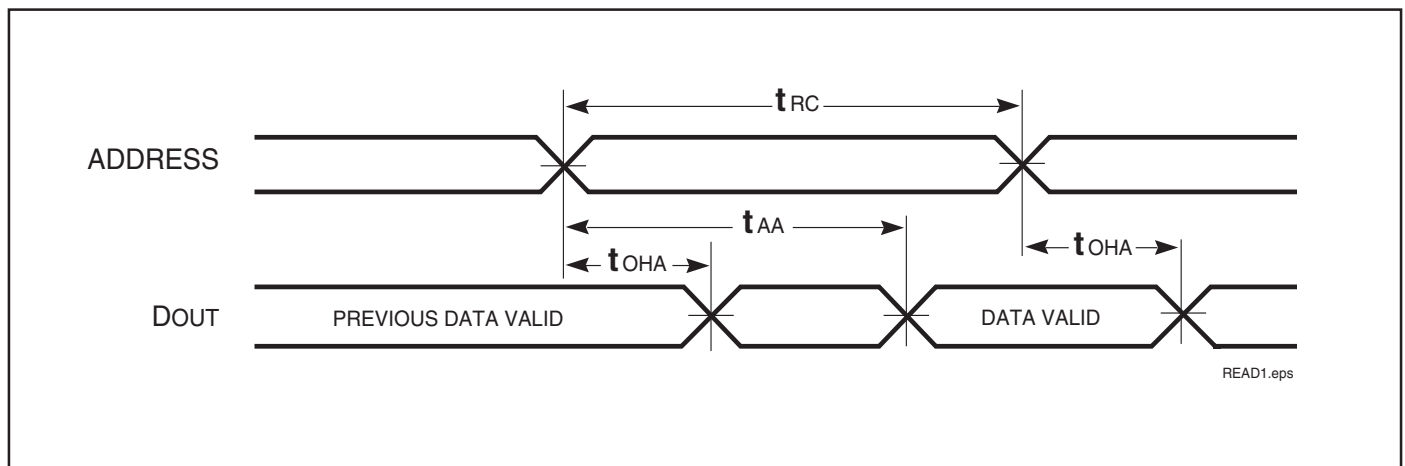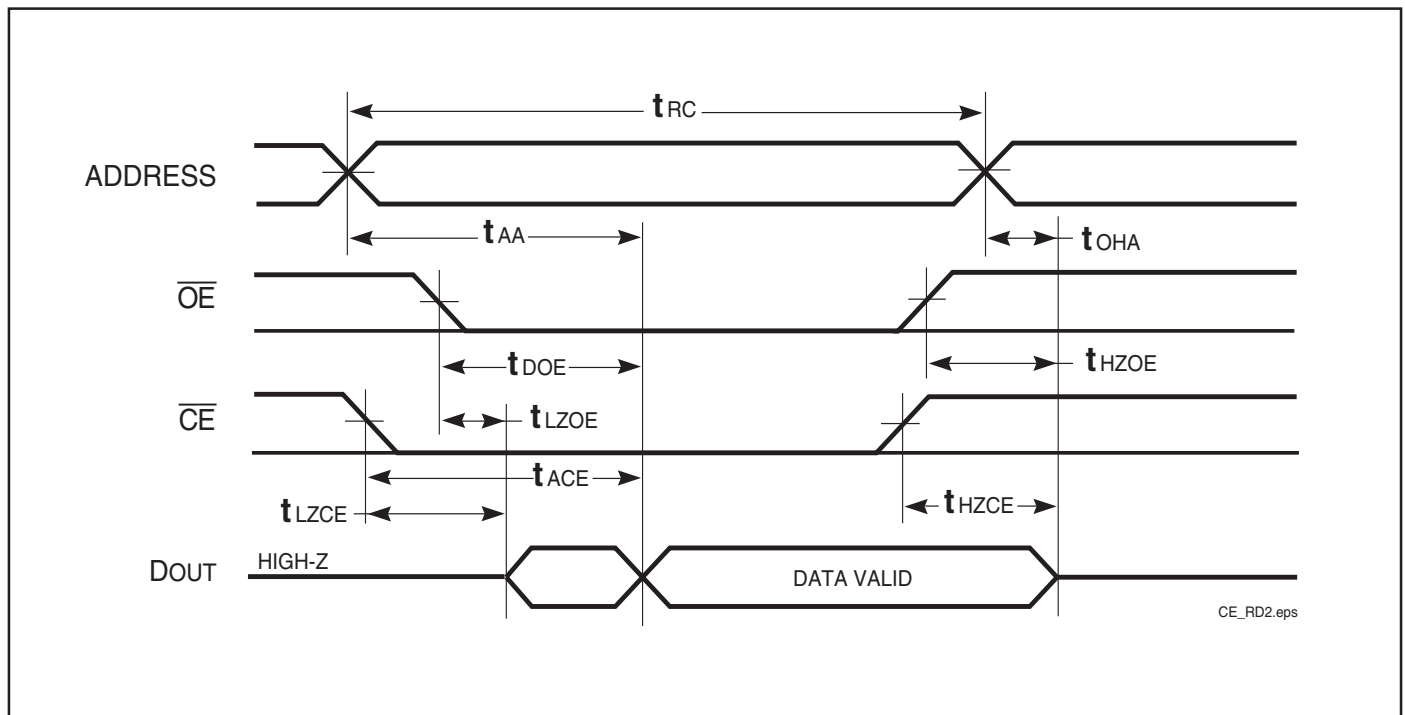## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-20 ns Min.	-20 ns Max.	Unit
t_{RC}	Read Cycle Time	20	—	ns
t_{AA}	Address Access Time	—	20	ns
t_{OHA}	Output Hold Time	2.5	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	8	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	8	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	8	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	8	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	ns

Notes:
1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

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AC WAVEFORMS
READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)

READ1.eps

READ CYCLE NO. 2[1,3] ($\overline{CE}$ and $\overline{OE}$ Controlled)

CE_RD2.eps

Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-8 Min.	-8 Max.	-10 Min.	-10 Max.	Unit
t_{WC}	Write Cycle Time	8	—	10	—	ns
t_{SCE}	$\overline{CE}$ to Write End	6.5	—	8	—	ns
t_{AW}	Address Setup Time to Write End	6.5	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	6.5	—	8	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width	6.5	—	8	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	8.0	—	10	—	ns
t_{SD}	Data Setup to Write End	5	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write. Shaded area product in development

## WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-20 ns Min.	Max.	Unit
t_{WC}	Write Cycle Time	20	—	ns
t_{SCE}	$\overline{CE}$ to Write End	12	—	ns
t_{AW}	Address Setup Time to Write End	12	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	12	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	12	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	17	—	ns
t_{SD}	Data Setup to Write End	9	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	9	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	3	—	ns

Notes:

1. Test conditions for IS61WV51216ALL/BLL assume signal transition times of 1.5ns or less, timing reference levels of 1.25V, input pulse levels of 0.4V to V_{DD}-0.3V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
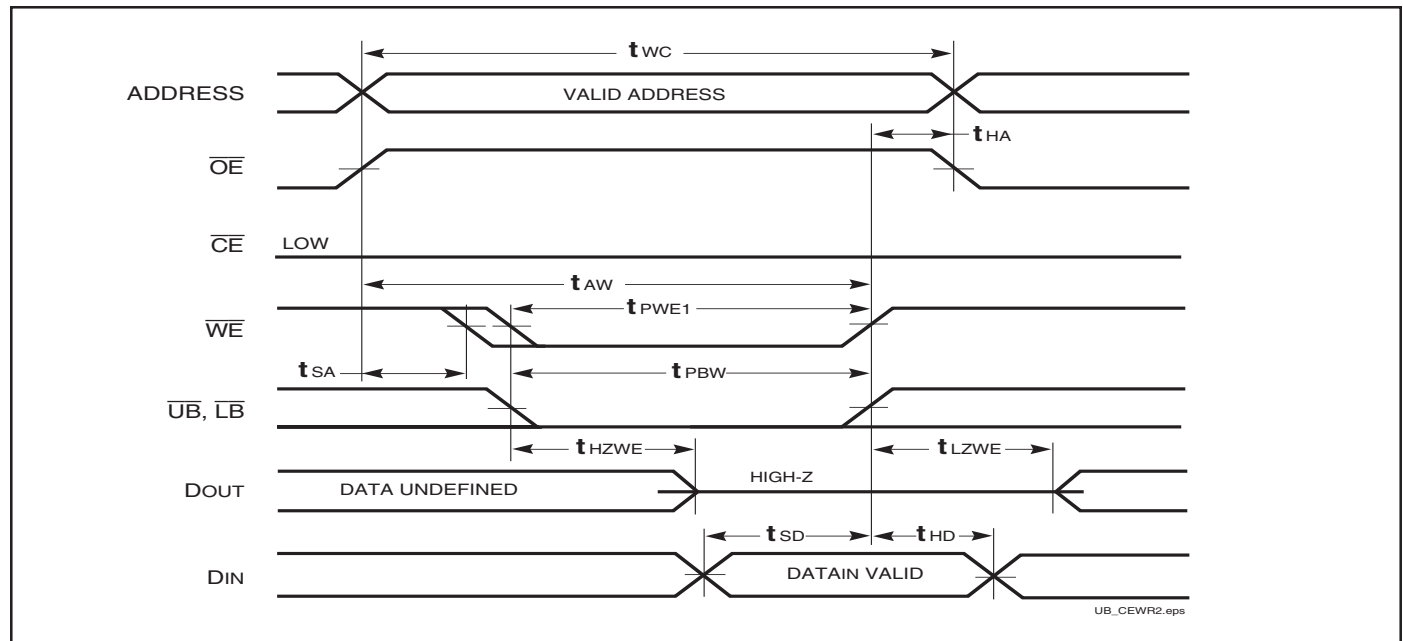
AC WAVEFORMS

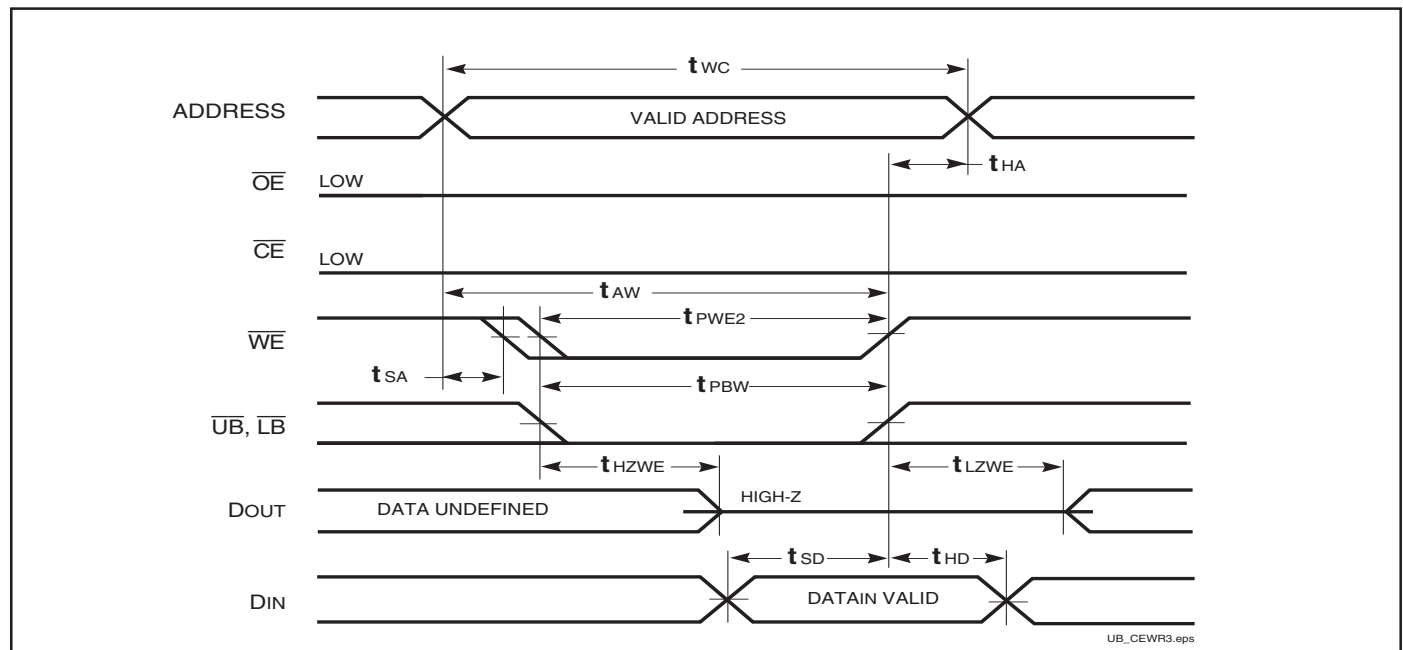**WRITE CYCLE NO. 1**[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

CE_WR1.eps
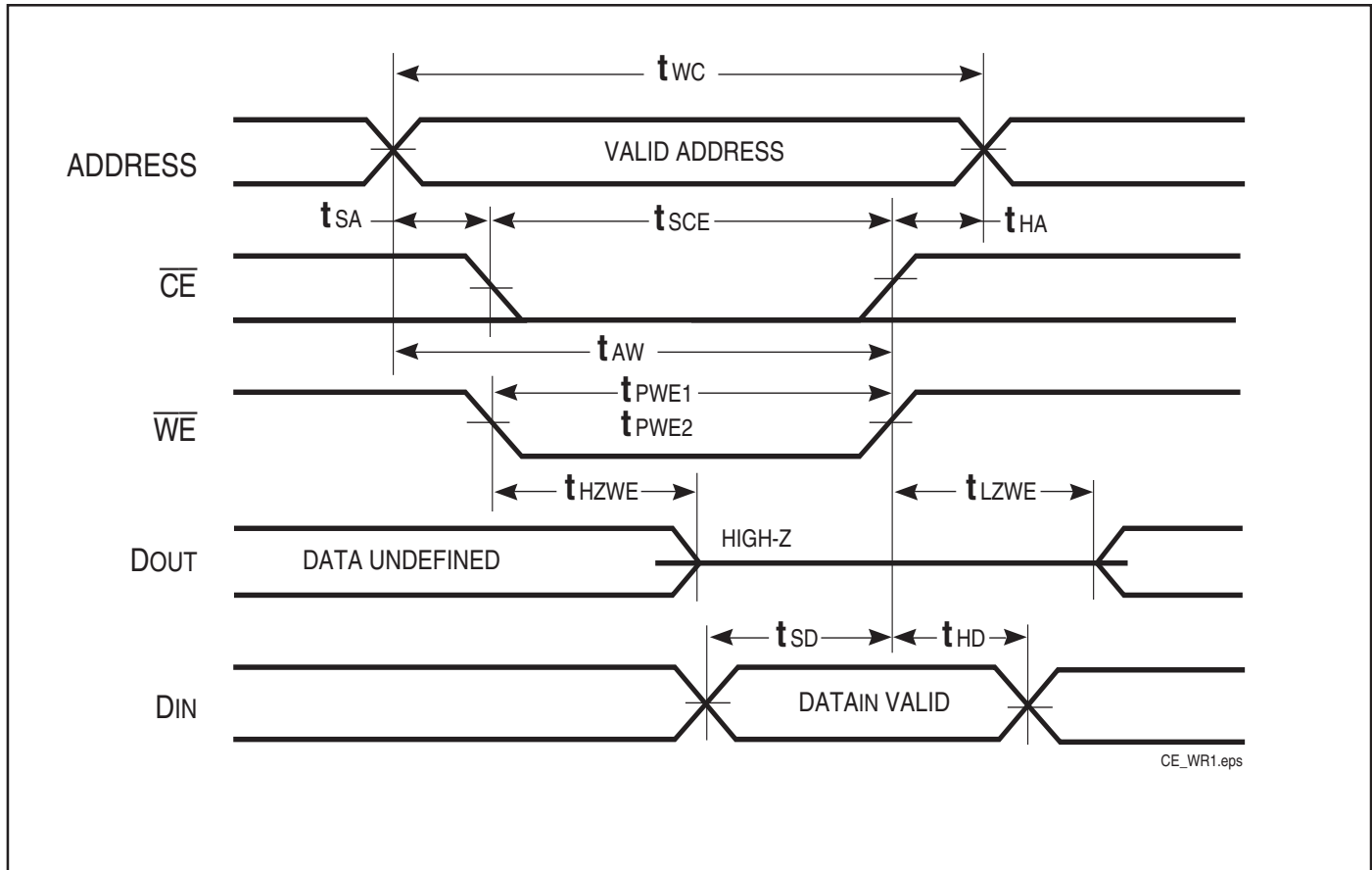
AC WAVEFORMS

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled. $\overline{OE}$ is HIGH During Write Cycle) [1,2]

ADDRESS — VALID ADDRESS
t_{WC}
t_{HA}
$\overline{OE}$
$\overline{CE}$ LOW
t_{AW}
t_{PWE1}
$\overline{WE}$
t_{SA}
t_{PBW}
$\overline{UB}, \overline{LB}$
t_{HZWE}
t_{LZWE}
Dout DATA UNDEFINED HIGH-Z
t_{SD}
t_{HD}
DIN DATAIN VALID

UB_CEWR2.eps

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled. $\overline{OE}$ is LOW During Write Cycle) [1]

ADDRESS VALID ADDRESS
t_{WC}
t_{HA}
$\overline{OE}$ LOW
$\overline{CE}$ LOW
t_{AW}
t_{PWE2}
$\overline{WE}$
t_{SA}
t_{PBW}
$\overline{UB}, \overline{LB}$
t_{HZWE}
t_{LZWE}
Dout DATA UNDEFINED HIGH-Z
t_{SD}
t_{HD}
DIN DATAIN VALID

UB_CEWR3.eps

AC WAVEFORMS

### WRITE CYCLE NO. 4 ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled, Back-to-Back Write) [1,3]
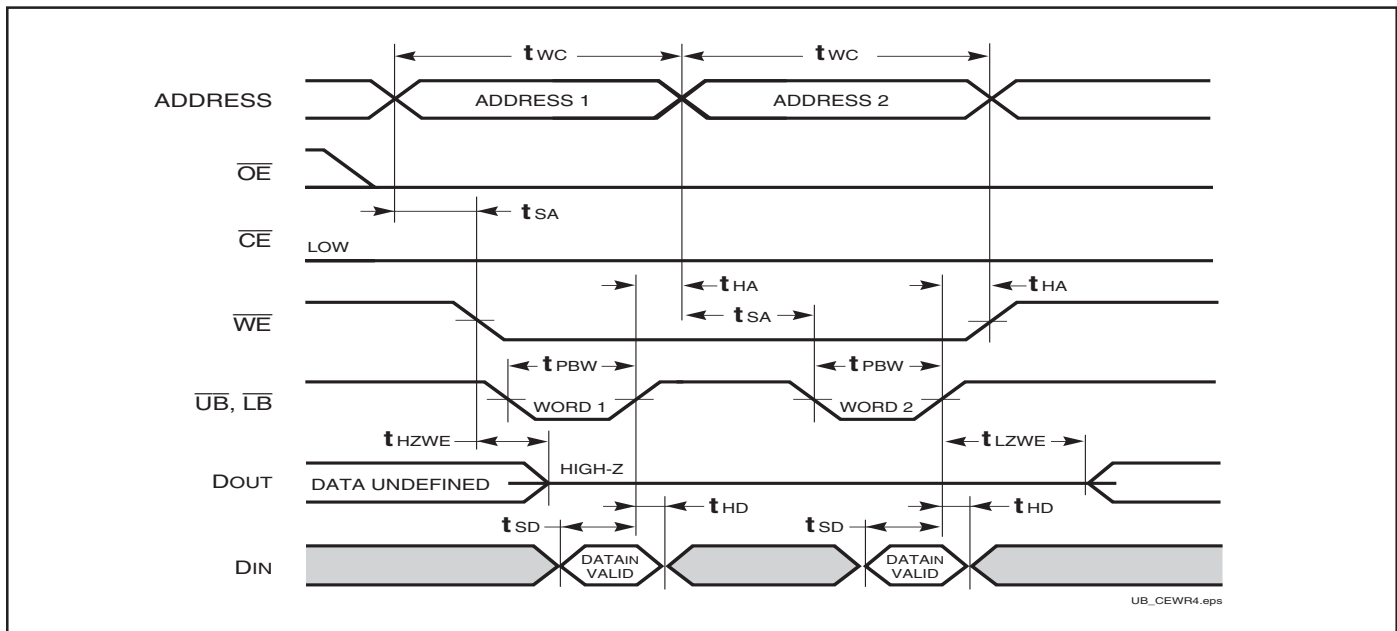
Notes:
1. The internal Write time is defined by the overlap of $\overline{\text{CE}}$ = LOW, $\overline{\text{UB}}$ and/or $\overline{\text{LB}}$ = LOW, and $\overline{\text{WE}}$ = LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA}, t_{HA}, t_{SD}, and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{\text{OE}}$ HIGH for a minimum of 4 ns before $\overline{\text{WE}}$ = LOW to place the I/O in a HIGH-Z state.
3. $\overline{\text{WE}}$ may be held LOW across many address cycles and the $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins can be used to control the Write function.

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DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		1.2	3.6	V
I_{DR}	Data Retention Current	$V_{DD} = 1.2V$, $\overline{CE} \geq V_{DD} - 0.2V$	Ind.	—	20	mA
			Auto.	—	50	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)
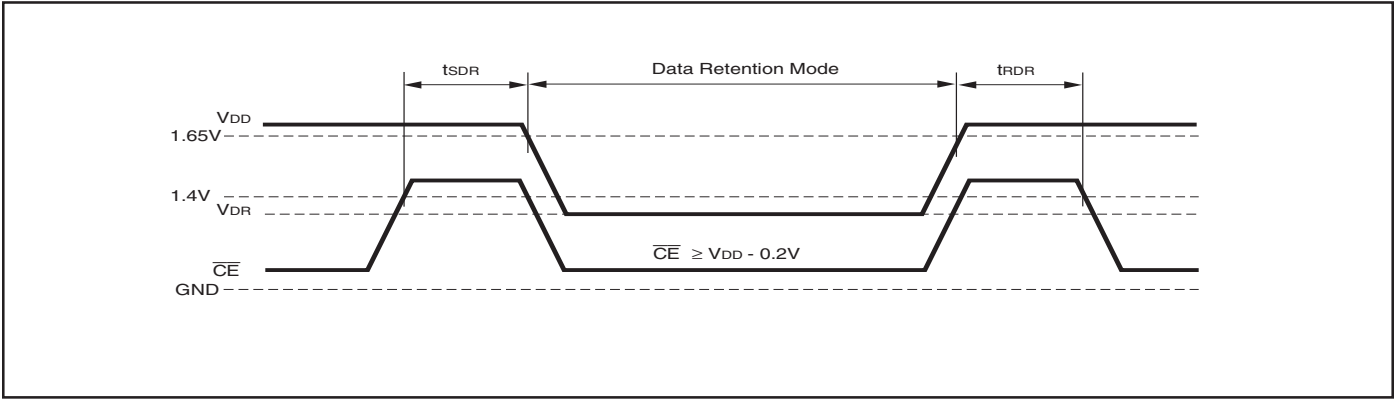
ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Voltage Range: 2.4V to 3.6V

Speed (ns)	Order Part No.	Package
10 (8[1])	IS61WV51216BLL-10MI	48 mini BGA (9mm x 11mm)
	IS61WV51216BLL-10MLI	48 mini BGA (9mm x 11mm), Lead-free
	IS61WV51216BLL-10TI	TSOP (Type II)
	IS61WV51216BLL-10TLI	TSOP (Type II), Lead-free

Note:
1. Speed = 8ns for V_{DD} = 3.3V $\pm$ 5%. Speed = 10ns for V_{DD} = 2.4V - 3.6V

**Industrial Range: -40°C to +85°C**

Voltage Range: 1.65V to 2.2V

Speed (ns)	Order Part No.	Package
20	IS61WV51216ALL-20MI	48 mini BGA (9mm x 11mm)
	IS61WV51216ALL-20TI	TSOP (Type II)

Automotive Range: -40°C to +125°C

Voltage Range: 2.4V to 3.6V

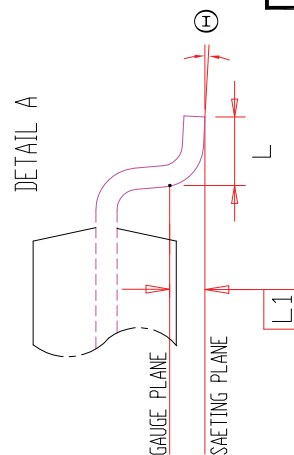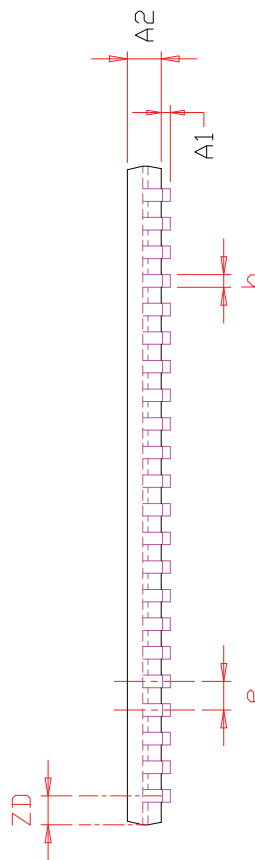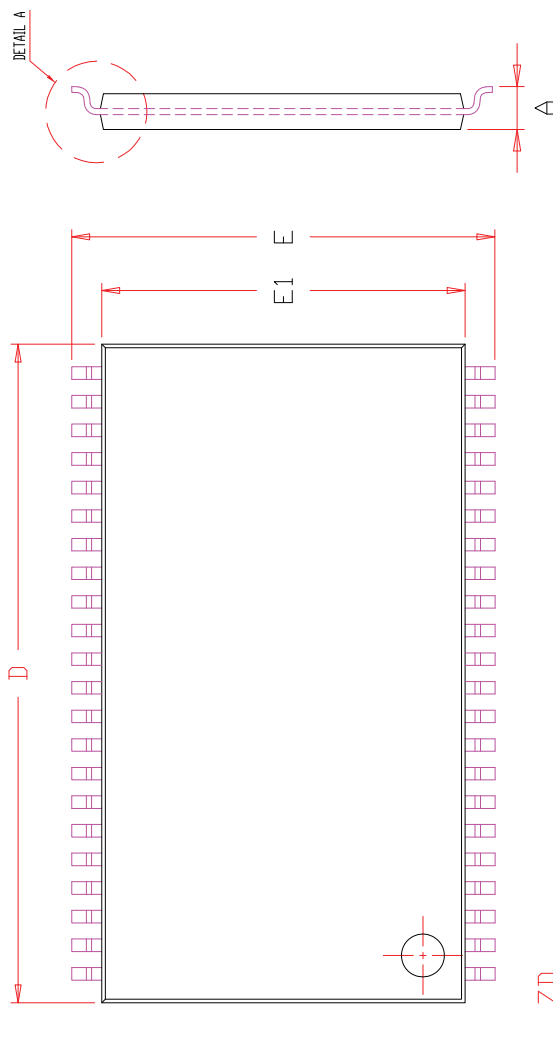| Speed (ns)	Order Part No.	Package
10	IS64WV51216BLL-10MA3	48 mini BGA (9mm x 11mm)
	IS64WV51216BLL-10MLA3	48 mini BGA (9mm x 11mm), Lead-free
	IS64WV51216BLL-10CTA3	TSOP (Type II), Copper Leadframe
	IS64WV51216BLL-10CTLA3	TSOP (Type II), Lead-free, Copper Leadframe
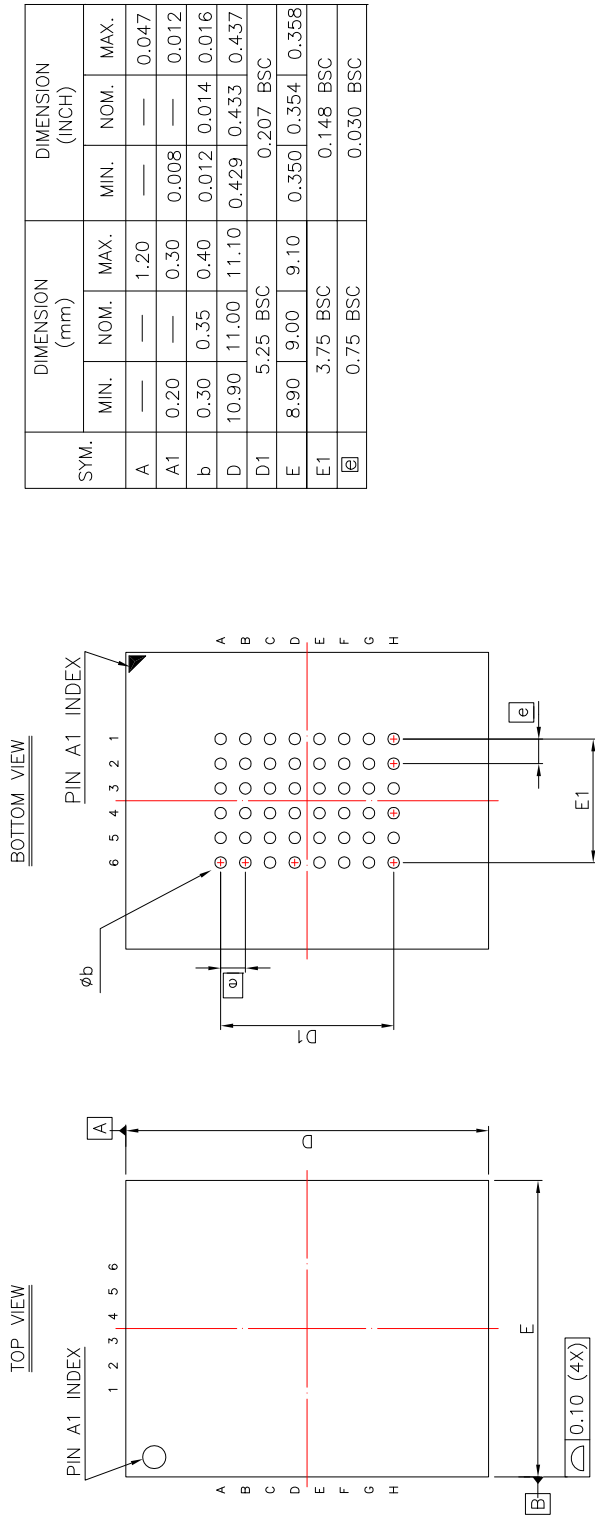
SYM.	DIMENSION (mm)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
b	0.30	0.35	0.40	0.012	0.014	0.016
D	10.90	11.00	11.10	0.429	0.433	0.437
D1	5.25 BSC			0.207 BSC		
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC			0.030 BSC		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

REV. **B**

DATE 08/21/2008

TITLE **48L 9x11mm TF-BGA**
Package Outline

BOTTOM VIEW

PIN A1 INDEX

TOP VIEW

PIN A1 INDEX

SEATING PLANE

IS61WV51216ALL
IS61WV51216BLL
IS64WV51216BLL

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
θ	0	—	8°	0	—	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

DETAIL A

GAUGE PLANE

SAETING PLANE

TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE	06/04/2008

Integrated Silicon Solution, Inc. — www.issi.com

Rev. F
10/01/09