1.2 DDR3 SDRAM package ballout 96-ball BGA – x16 (Two Ranks)

	1	2	3	4	5	6	7	8	9
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS
B	VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ
G	VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ
J	ODT1	VSS	RAS#				CK	VSS	CKE1
K	ODT0	VDD	CAS#				CK#	VDD	CKE0
L	CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1
M	VSS	BA0	BA2				NC	VREFCA	VSS
N	VDD	A3	A0				A12/BC#	BA1	VDD
P	VSS	A5	A2				A1	A4	VSS
R	VDD	A7	A9				A11	A6	VDD
T	VSS	RESET#	A13				A14	A8	VSS

Notes:
1. NC balls have no internal connection.

1.3 Pinout Description - JEDEC Standard

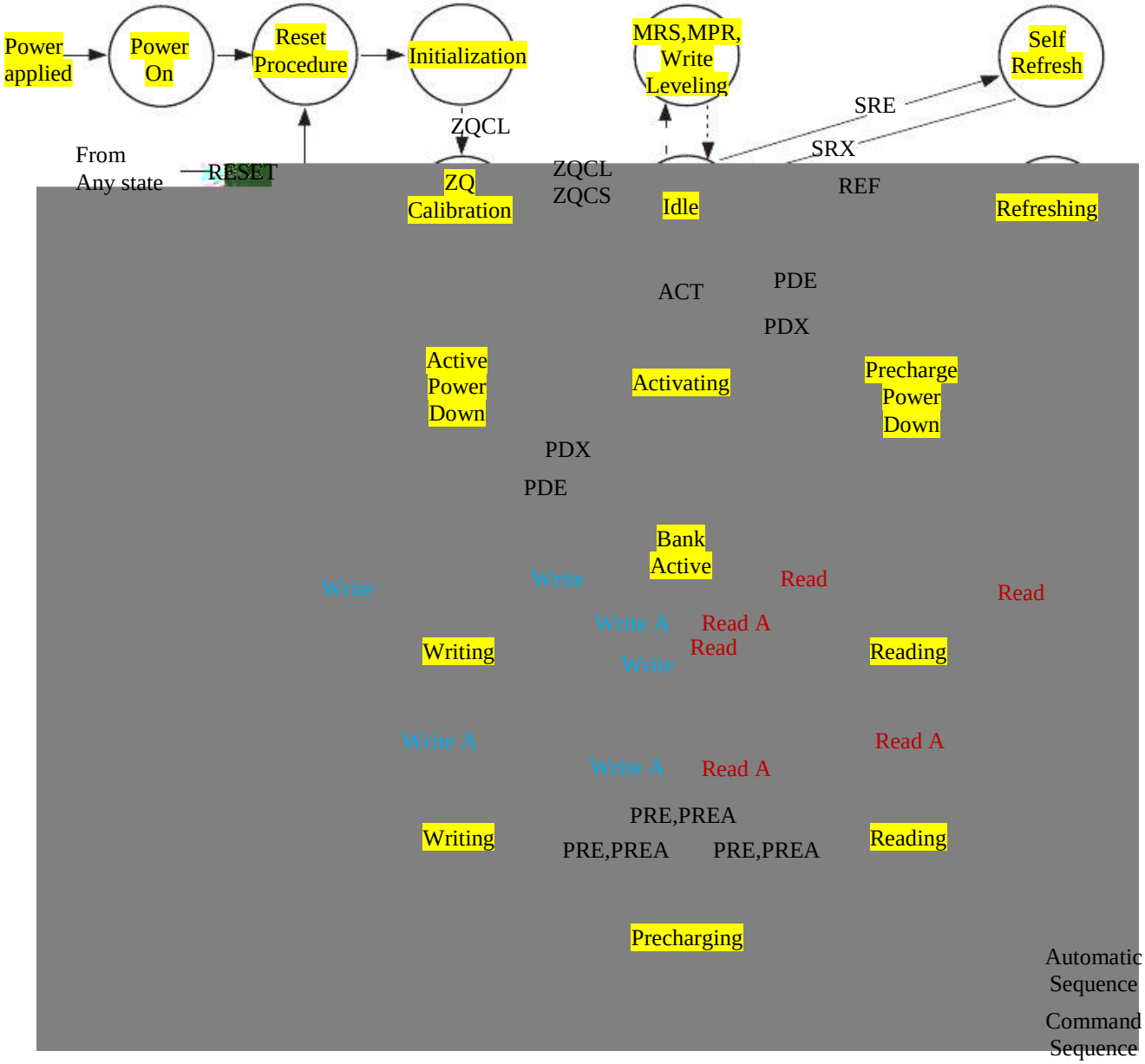
Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE, (CKE0, CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#, (CS0#, CS1#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT,(ODT0,ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#. CAS#. WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A14	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e., 1.20V for DC high and 0.30V for DC low.
DQ(DQL, DQU)	Input / Output	Data Input/ Output: Bi-directional data bus.
DQS, DQS#, (DQSU, DQSU#, DQSL, DQSL#)	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.5 V +/- 0.075 V for standard voltage or 1.35V +0.1V, -0.067V for low voltage
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.5 V +/- 0.075 V for standard voltage or 1.35V +0.1V, -0.067V for low voltage

VSS	Supply	Ground
VREFDQ	Supply	Reference voltage for DQ
VREFCA	Supply	Reference voltage for CA
ZQ,(ZQ0, ZQ1)	Supply	Reference Pin for ZQ

Note: Input only pins (BA0-BA2, A0-A14, RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination.

2. FUNCTION DESCRIPTION

2.1 Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short		

9.6 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see corresponding tables) to the ΔtDS and ΔtDH (see corresponding tables) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of V IH(ac) min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac) max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to VREF(dc) level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc) max and the first crossing of VREF(dc) . Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc) min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V REF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac) .

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

9.6.1 Data Setup and Hold Base-Values

	Symbol	Reference	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	Units
DDR3	tDS(base) AC175	VIH/L(ac), SR= 1V/ns	120	70	-	-	-	ps
	tDS(base) AC150	VIH/L(ac), SR= 1V/ns	170	120	75	55	-	ps
	tDS(base) AC135	VIH/L(ac), SR= 1V/ns	210	160	105	85	-	ps
	tDS(base) AC135	VIH/L(ac), SR= 2V/ns	-	-	-	-	113	ps
	tDH(base) DC100	VIH/L(dc), SR= 1V/ns	205	155	120	100	-	ps
	tDH(base) DC100	VIH/L(dc), SR= 2V/ns	-	-	-	-	125	ps
DDR3L	tDS(base) AC160	VIH/L(ac), SR= 1V/ns	135	85	-	-	-	ps
	tDS(base) AC135	VIH/L(ac), SR= 1V/ns	185	135	90	70	-	ps
	tDS(base) AC130	VIH/L(ac), SR= 2V/ns	-	-	-	-	115	ps
	tDH(base) DC90	VIH/L(dc), SR= 1V/ns	215	165	130	110	-	ps
	tDH(base) DC90	VIH/L(dc), SR= 2V/ns	-	-	-	-	130	ps

Note: AC/DC referenced for 2V/ns DQ-slew rate and 4V/ns DQS slew rate, or 1V/ns DQ-slew rate and 2V/ns DQS slew rate, as shown.

9.6.2 Derating values [ps] for DDR3L-800/1066 tDS/tDH - AC/DC based AC160

AC160 Threshold -> VIH(ac) = VREF(dc) + 160mV, VIL(ac) = VREF(dc) - 160mV																	
DDR3L		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	80	45	80	45	80	45	-	-	-	-	-	-	-	-	-	-
	1.5	53	30	53	30	53	30	61	38	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-1	-3	-1	-3	7	5	15	13	23	21	-	-	-	-
	0.8	-	-	-	-	-3	-8	5	1	13	9	21	17	29	27	-	-
	0.7	-	-	-	-	-	-	3	-5	11	3	19	11	27	21	35	37
	0.6	-	-	-	-	-	-	-	-	8	-4	16	4	24	14	32	30
	0.5	-	-	-	-	-	-	-	-	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-8	-11	0	5

9.6.3 Derating values [ps] for DDR3L-800/1066/1333/1600 tDS/tDH - AC/DC based AC135 Threshold

AC135 Threshold -> VIH(ac) = VREF(dc) + 135mV, VIL(ac) = VREF(dc) - 135mV																	
DDR3L		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	68	45	68	45	68	45	-	-	-	-	-	-	-	-	-	-
	1.5	45	30	45	30	45	30	53	38	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-3	2	-3	10	5	18	13	26	21	-	-	-	-
	0.8	-	-	-	-	3	-8	11	1	19	9	27	17	35	27	-	-
	0.7	-	-	-	-	-	-	14	-5	22	3	30	11	38	21	46	37
	0.6	-	-	-	-	-	-	-	-	25	-4	33	4	41	14	49	30
	0.5	-	-	-	-	-	-	-	-	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-11	38	5

9.6.4 Derating values [ps] for DDR3L-1866 tDS/tDH - AC/DC based AC130 Threshold

AC130 Threshold -> VIH(ac) = VREF(dc) + 130mV, VIL(ac) = VREF(dc) - 130mV																									
DDR3L		DQS, DQS# Differential Slew Rate																							
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	4	33	23	33	23	33	23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	28	19	28	19	28	19	28	19	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3	22	15	22	15	22	15	22	15	22	15	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	13	9	13	9	13	9	13	9	13	9	-	-	-	-	-	-	-	-	-	-	-	-
	2	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-22	-15	-22	-15	-22	-15	-22	-15	-14	-7	-	-	-	-	-	-	-	-
	1	-	-	-	-	-	-	-	-	-65	-45	-65	-45	-65	-45	-57	-37	-49	-29	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-62	-48	-62	-48	-54	-40	-46	-32	-38	-24	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-61	-53	-53	-45	-45	-37	-37	-29	-29	-19	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-49	-50	-41	-42	-33	-34	-25	-24	-17	-8
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-37	-49	-29	-41	-21	-31	-13	-15
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-31	-51	-23	-41	-15	-25
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-28	-56	-20	-40

9.6.5 Derating values [ps] for DDR3-800/1066 tDS/tDH - AC/DC based AC175 Threshold

AC175 Threshold -> VIH(ac) = VREF(dc) + 175mV, VIL(ac) = VREF(dc) - 175mV																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

9.6.6 Derating values [ps] for DDR3-800/1066/1333/1600 tDS/tDH - AC/DC based AC150 Threshold

AC150 Threshold -> VIH(ac) = VREF(dc) + 150mV, VIL(ac) = VREF(dc) - 150mV																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

9.6.7 Derating values [ps] for DDR3-1866/2133 tDS/tDH - AC/DC based AC135 Threshold

AC135 Threshold -> VIH(ac) = VREF(dc) + 135mV, VIL(ac) = VREF(dc) - 135mV DC100 Threshold -> VIH(dc) = VREF(dc) + 100mV, VIL(dc) = VREF(dc) - 100mV																							
DDR3		DQS, DQS# Differential Slew Rate																					
		8.0V/ns		7.0V/ns		6.0V/ns		5.0V/ns		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	4	34	25	34	25	34	25	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	29	21	29	21	29	21	29	21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3	23	17	23	17	23	17	23	17	23	17	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	14	10	14	10	14	10	14	10	14	10	-	-	-	-	-	-	-	-	-	-	-	-
	2	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-23	-17	-23	-17	-23	-17	-23	-17	-15	-9	-	-	-	-	-	-	-	-
	1	-	-	-	-	-	-	-	-	-68	-50	-68	-50	-68	-50	-60	-42	-52	-34	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-66	-54	-66	-54	-58	-46	-50	-38	-42	-30	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-64	-60	-56	-52	-48	-44	-40	-36	-32	-26	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-53	-59	-45	-51	-37	-43	-29	-33	-21	-17
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-43	-61	-35	-53	-27	-43	-19	-27
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-39	-66	-31	-56	-23	-40
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-36	-76	-30	-60

9.6.8 Derating values [ps] for DDR3-800/1066/1333/1600 tDS/tDH - AC/DC based AC135 Threshold

AC135 Threshold -> VIH(ac) = VREF(dc) + 135mV, VIL(ac) = VREF(dc) - 135mV DC100 Threshold -> VIH(dc) = VREF(dc) + 100mV, VIL(dc) = VREF(dc) - 100mV																	
DDR3		DQS, DQS# Differential Slew Rate															
		4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew Rate V/ns	2	68	50	68	50	68	50	-	-	-	-	-	-	-	-	-	-
	1.5	45	34	45	34	45	34	53	42	-	-	-	-	-	-	-	-
	1	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-4	2	-4	10	4	18	12	26	20	-	-	-	-
	0.8	-	-	-	-	3	-10	11	-2	19	6	27	14	35	24	-	-
	0.7	-	-	-	-	-	-	14	-8	22	0	30	8	38	18	46	34
	0.6	-	-	-	-	-	-	-	-	25	-10	33	-2	41	8	49	24
	0.5	-	-	-	-	-	-	-	-	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-26	38	-10

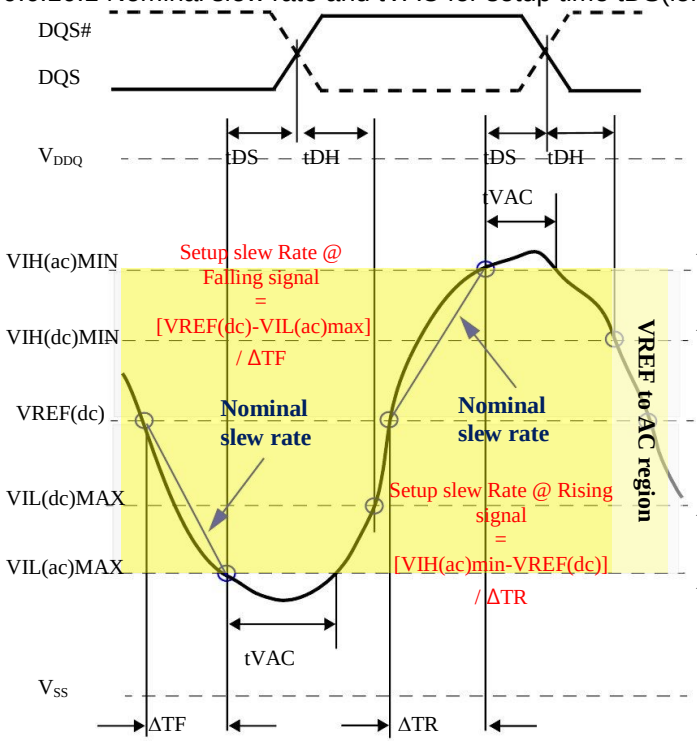
9.6.9 Required minimum time tVAC [ps] above VIH(ac) {below VIL(ac)} for valid DQ transition

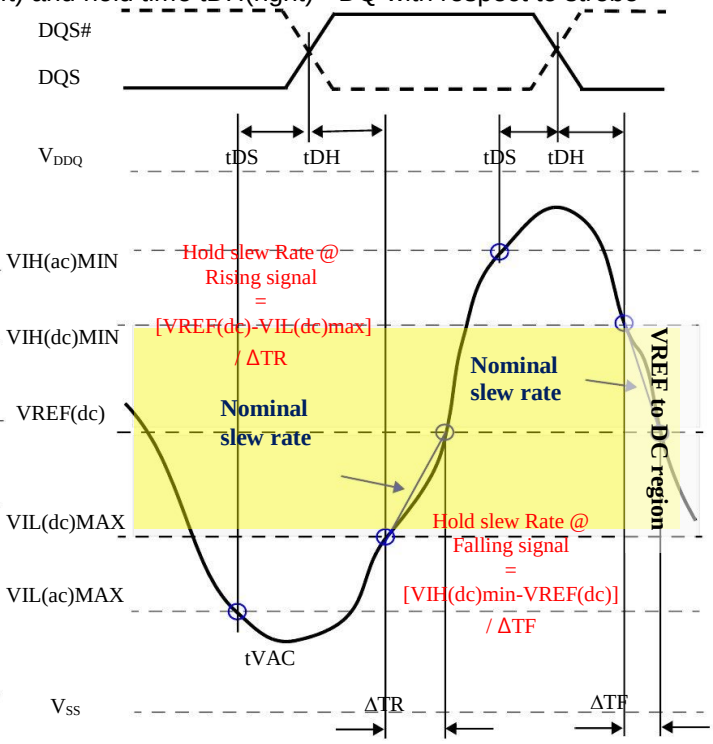
Slew Rate [V/ns]	DDR3					DDR3L		
	800/1066	800/1066/1333/1600	800/1066/1333/1600	1866	2133	800/1066	800/1066/1333/1600	1866
	AC175	AC150	AC135			AC160	AC135	AC130
> 2.0	75	105	113	93	73	165	113	95
2	57	105	113	93	73	165	113	95
1.5	50	80	90	70	50	138	90	73
1	38	30	45	25	5	85	45	30
0.9	34	13	30	Note	Note	67	30	16
0.8	29	Note	11	Note	Note	45	11	Note
0.7	Note	Note	Note	-	-	16	Note	-
0.6	Note	Note	Note	-	-	Note	Note	-
0.5	Note	Note	Note	-	2	Note	Note	-
< 0.5	Note	Note	Note	-	-	Note	Note	-

Note:
The rising input signal shall become equal to or greater than VIH(ac) level; and the falling input signal shall become equal to or less than VIL(ac) level.

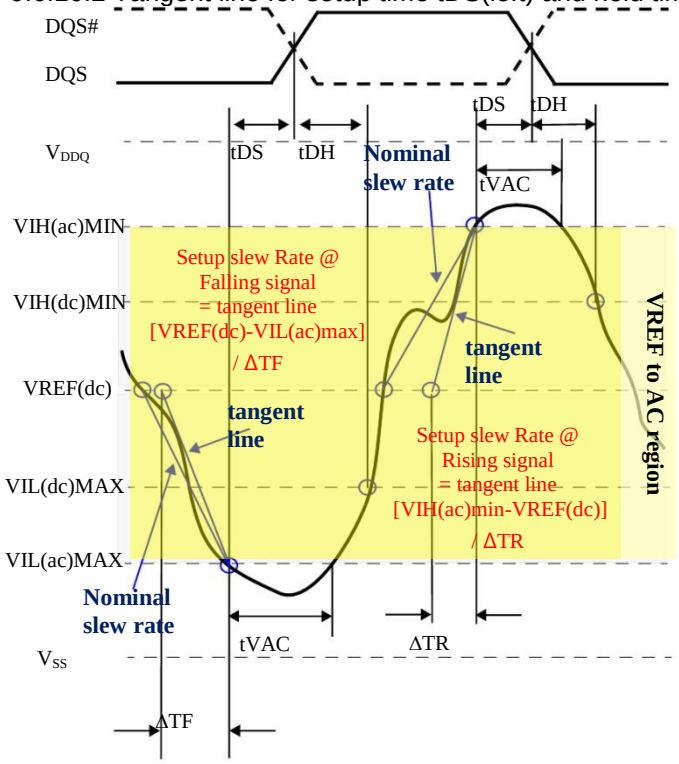
9.6.10 Data Setup, Hold and Slew Rate Derating

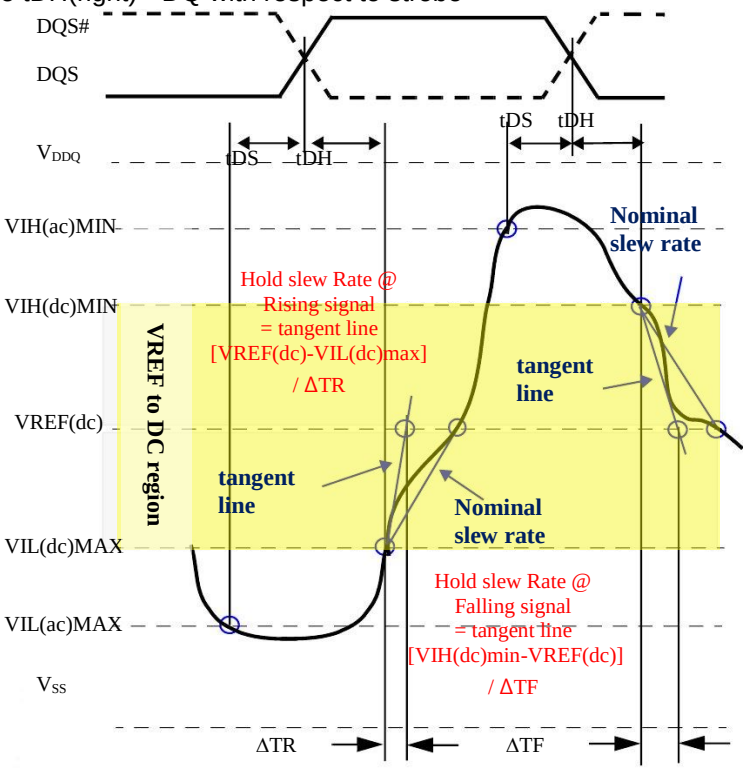
9.6.10.1 Nominal slew rate and tVAC for setup time tDS(left) and hold time tDH(right) - DQ with respect to strobe





9.6.10.2 Tangent line for setup time tDS(left) and hold time tDH(right) - DQ with respect to strobe





ORDERING INFORMATION, 512MX16, 1.5V (DDR3)

512Mx16 - Commercial Range: (0°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1333MT/s	9-9-9	IS43TR16512A-15HBL	96-ball BGA,Lead-free
1600MT/s	11-11-11	IS43TR16512A-125KBL	96-ball BGA,Lead-free
1866MT/s	13-13-13	IS43TR16512A-107MBL	96-ball BGA,Lead-free

512Mx16 - Industrial Range: (–40°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1333MT/s	9-9-9	IS43TR16512A-15HBLI	96-ball BGA,Lead-free
1600MT/s	11-11-11	IS43TR16512A-125KBLI	96-ball BGA,Lead-free
1866MT/s	13-13-13	IS43TR16512A-107MBLI	96-ball BGA,Lead-free

512Mx16 – Automotive, A1 Range: (–40°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1333MT/s	9-9-9	IS46TR16512A-15HBLA1	96-ball BGA,Lead-free
1600MT/s	11-11-11	IS46TR16512A-125KBLA1	96-ball BGA,Lead-free

512Mx16 – Automotive, A2 Range: (–40°C ≤ T_C ≤ 105°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1333MT/s	9-9-9	IS46TR16512A-15HBLA2	96-ball BGA,Lead-free
1600MT/s	11-11-11	IS46TR16512A-125KBLA2	96-ball BGA,Lead-free

Note: Contact ISSI for availability of options.

ORDERING INFORMATION,512MX16,1.35V (DDR3L)

512Mx16 - Commercial Range: (0°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1333MT/s	9-9-9	IS43TR16512AL-15HBL	96-ball BGA,Lead-free
1600MT/s	11-11-11	IS43TR16512AL-125KBL	96-ball BGA,Lead-free
1866MT/s	13-13-13	IS43TR16512AL-107MBL	96-ball BGA,Lead-free

512Mx16 - Industrial Range: (–40°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1333MT/s	9-9-9	IS43TR16512AL-15HBLI	96-ball BGA,Lead-free
1600MT/s	11-11-11	IS43TR16512AL-125KBLI	96-ball BGA,Lead-free

512Mx16 – Automotive, A1 Range: (–40°C ≤ T_C ≤ 95°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1333MT/s	9-9-9	IS46TR16512AL-15HBLA1	96-ball BGA,Lead-free
1600MT/s	11-11-11	IS46TR16512AL-125KBLA1	96-ball BGA,Lead-free

512Mx16 – Automotive, A2 Range: (–40°C ≤ T_C ≤ 105°C)

Data Rate	CL-tRCD-tRP	Order Part No.	Package
1333MT/s	9-9-9	IS46TR16512AL-15HBLA2	96-ball BGA,Lead-free
1600MT/s	11-11-11	IS46TR16512AL-125KBLA2	96-ball BGA,Lead-free

Note: Contact ISSI for availability of options.

PACKAGE OUTLINE DRAWING

96-ball BGA (10mm x 14mm): 0.8mm x 0.8mm Pitch (x16)