

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	$V_{GE} = 0V, I_C = 100\mu A$ ③
$\Delta V_{(BR)CES} / \Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.2	—	V/°C	$V_{GE} = 0V, I_C = 1mA$ (25°C-150°C)
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.9	2.2	V	$I_C = 20A, V_{GE} = 15V, T_J = 25^\circ\text{C}$
		—	2.3	—		$I_C = 20A, V_{GE} = 15V, T_J = 150^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0	V	$V_{CE} = V_{GE}, I_C = 600\mu A$
g_{fe}	Forward Transconductance	—	22	—	S	$V_{CE} = 50V, I_C = 20A, PW = 30\mu s$
I_{CES}	Collector-to-Emitter Leakage Current	—	1.0	100	μA	$V_{GE} = 0V, V_{CE} = 1200V$
		—	120	—		$V_{GE} = 0V, V_{CE} = 1200V, T_J = 150^\circ\text{C}$
V_{FM}	Diode Forward Voltage Drop	—	1.15	1.26	V	$I_F = 20A$
		—	1.08	—		$I_F = 20A, T_J = 150^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 30V$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	85	130	nC	$I_C = 20A$
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	15	20		$V_{GE} = 15V$
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	35	50		$V_{CC} = 600V$
E_{off}	Turn-Off Switching Loss	—	620	850	μJ	$I_C = 20A, V_{CC} = 600V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu H, L_S = 150nH, T_J = 25^\circ\text{C}$ Energy losses include tail
$t_{d(off)}$	Turn-Off delay time	—	160	180	ns	$I_C = 20A, V_{CC} = 600V, V_{GE} = 15V$
t_f	Fall time	—	80	105		$R_G = 10\Omega, L = 200\mu H, L_S = 150nH, T_J = 25^\circ\text{C}$
E_{off}	Turn-Off Switching Loss	—	1120	—	μJ	$I_C = 20A, V_{CC} = 600V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu H, L_S = 150nH, T_J = 150^\circ\text{C}$ Energy losses include tail
$t_{d(off)}$	Turn-Off delay time	—	190	—	ns	$I_C = 20A, V_{CC} = 600V, V_{GE} = 15V$
t_f	Fall time	—	210	—		$R_G = 10\Omega, L = 200\mu H, L_S = 150nH, T_J = 150^\circ\text{C}$
C_{ies}	Input Capacitance	—	1940	—	pF	$V_{GE} = 0V$
C_{oes}	Output Capacitance	—	120	—		$V_{CC} = 30V$
C_{res}	Reverse Transfer Capacitance	—	40	—		$f = 1.0MHz$
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 150^\circ\text{C}, I_C = 80A$ $V_{CC} = 960V, V_p = 1200V$ $R_g = 10\Omega, V_{GE} = +20V \text{ to } 0V$

Notes:

- ① $V_{CC} = 80\% (V_{CES}), V_{GE} = 20V, R_G = 10\Omega$.
- ② Pulse width limited by max. junction temperature.
- ③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.
- ④ R_θ is measured at T_J approximately 90°C .
- ⑤ FBSOA operating conditions only.
- ⑥ $V_{GE} = 0V, T_J = 75^\circ\text{C}, PW \leq 10\mu s$.

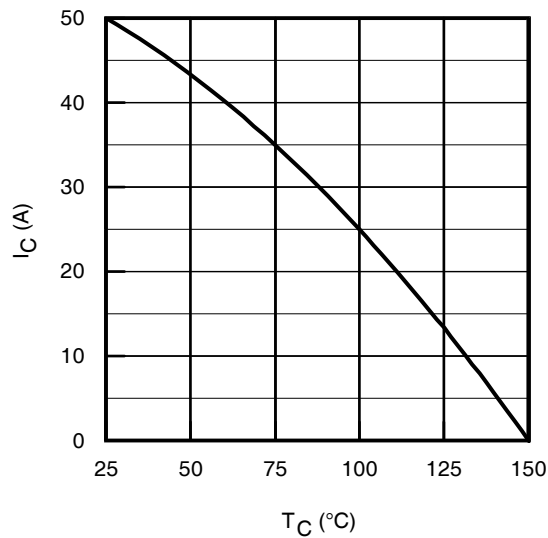


Fig. 1 - Maximum DC Collector Current vs. Case Temperature

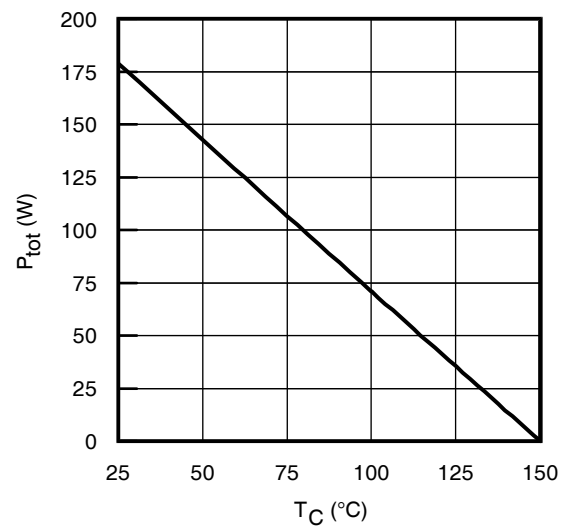


Fig. 2 - Power Dissipation vs. Case Temperature

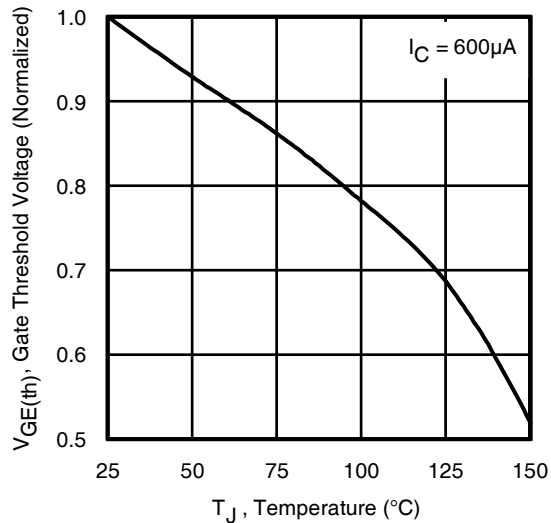


Fig. 3 - Typical Gate Threshold Voltage (Normalized) vs. Junction Temperature

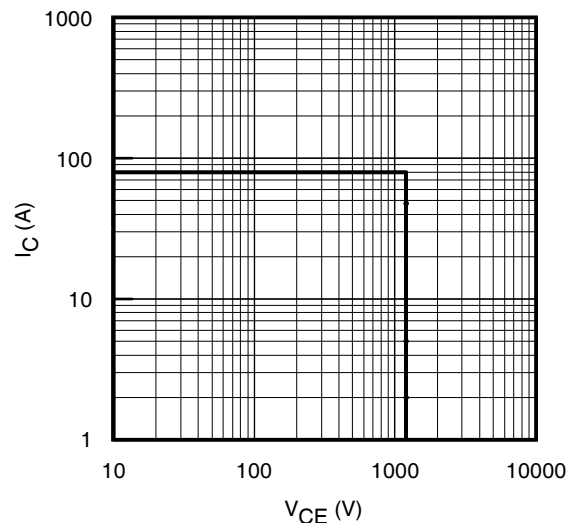


Fig. 4 - Reverse Bias SOA
 $T_J = 150^\circ\text{C}$; $V_{GE} = 20\text{V}$

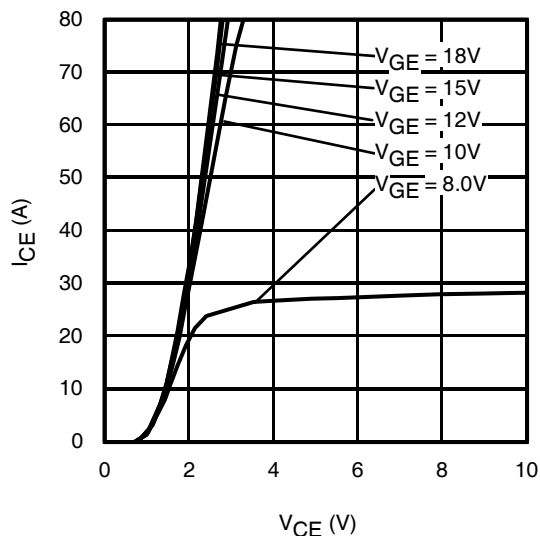


Fig. 5 - Typ. IGBT Output Characteristics
 $T_J = -40^\circ\text{C}$; $t_p = 30\mu\text{s}$

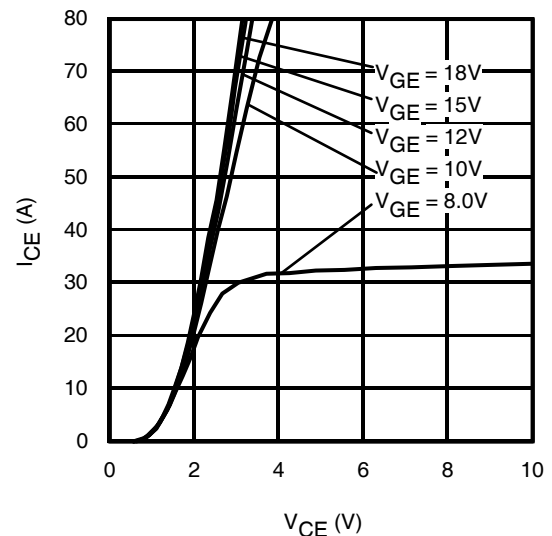


Fig. 6 - Typ. IGBT Output Characteristics
 $T_J = 25^\circ\text{C}$; $t_p = 30\mu\text{s}$

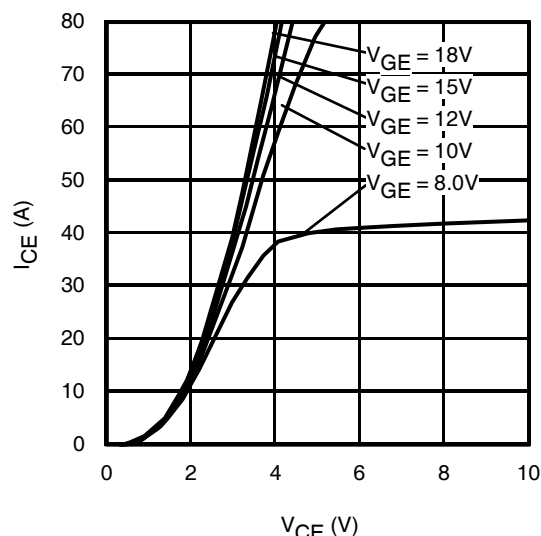


Fig. 7 - Typ. IGBT Output Characteristics
 $T_J = 150^\circ\text{C}$; $t_p = 30\mu\text{s}$

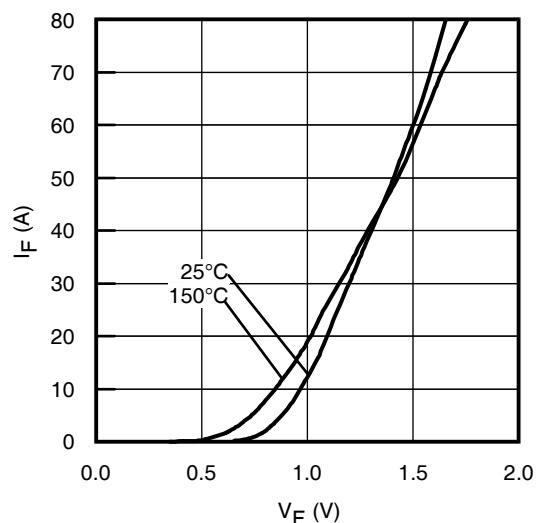


Fig. 8 - Typ. Diode Forward Voltage Drop Characteristics

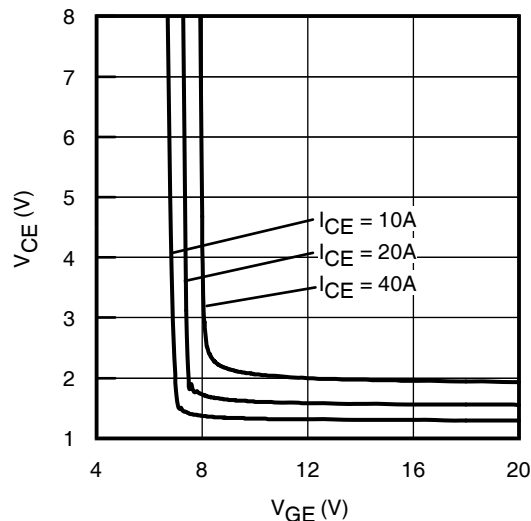


Fig. 9 - Typical V_{CE} vs. V_{GE}
 $T_J = -40^\circ\text{C}$

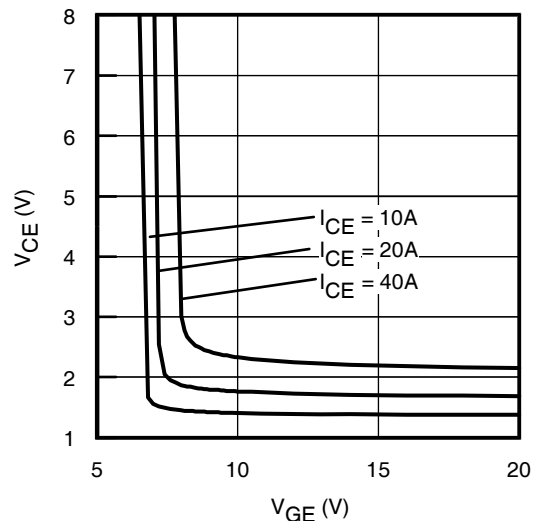


Fig. 10 - Typical V_{CE} vs. V_{GE}
 $T_J = 25^\circ\text{C}$

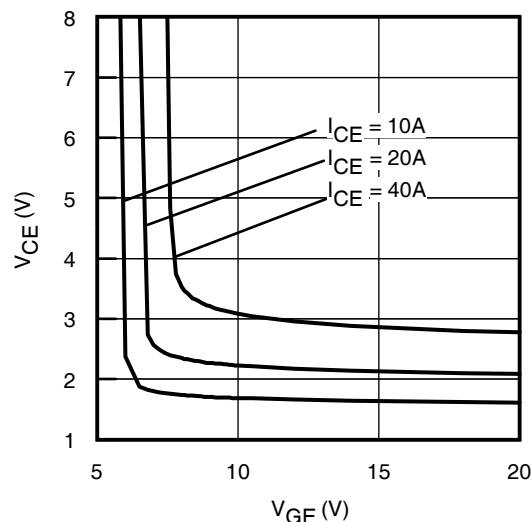


Fig. 11 - Typical V_{CE} vs. V_{GE}
 $T_J = 150^\circ\text{C}$

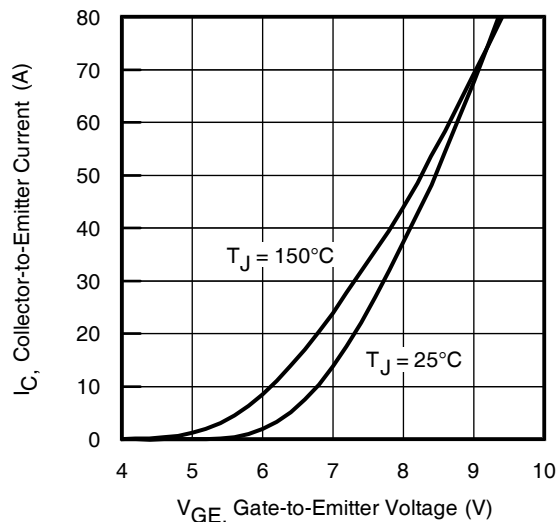


Fig. 12 - Typ. Transfer Characteristics
 $V_{CE} = 50\text{V}$; $t_p = 30\mu\text{s}$

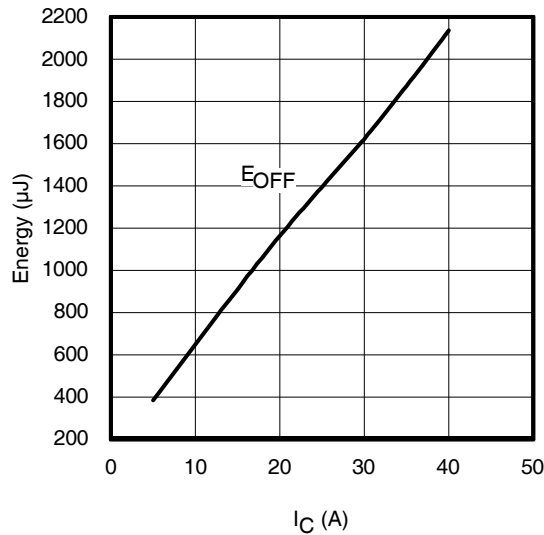


Fig. 13 - Typ. Energy Loss vs. I_C
 $T_J = 150^\circ\text{C}$; $L = 680\mu\text{H}$; $V_{CE} = 600\text{V}$; $R_G = 10\Omega$; $V_{GE} = 15\text{V}$

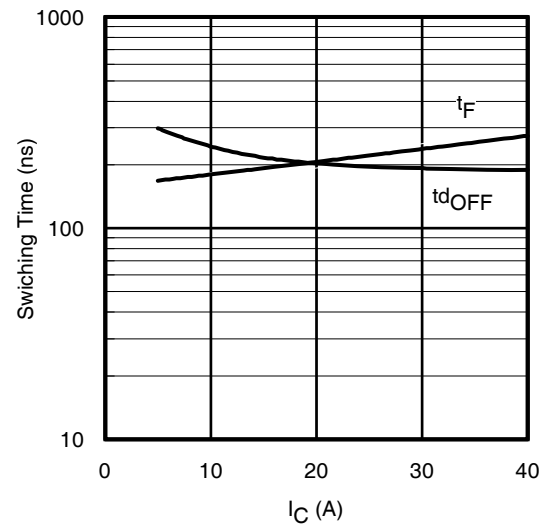


Fig. 14 - Typ. Switching Time vs. I_C
 $T_J = 150^\circ\text{C}$; $L = 680\mu\text{H}$; $V_{CE} = 600\text{V}$; $R_G = 10\Omega$; $V_{GE} = 15\text{V}$

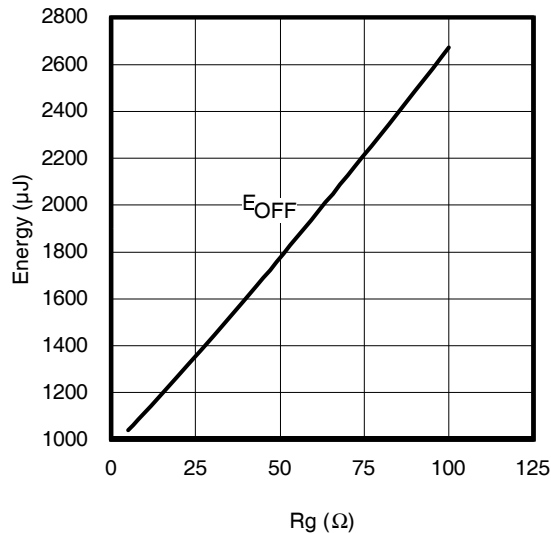


Fig. 15 - Typ. Energy Loss vs. R_G
 $T_J = 150^\circ\text{C}$; $L = 680\mu\text{H}$; $V_{CE} = 600\text{V}$; $I_{CE} = 20\text{A}$; $V_{GE} = 15\text{V}$

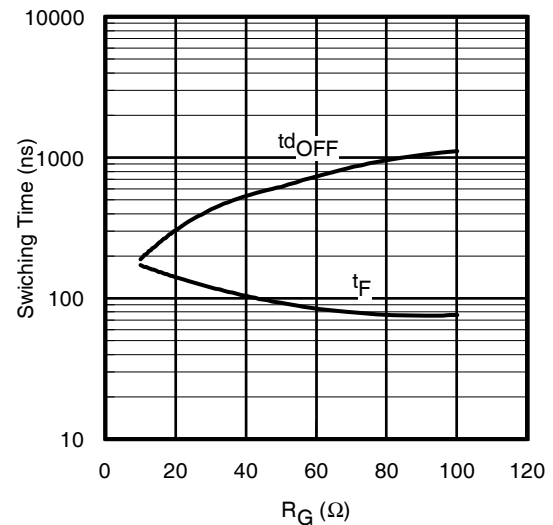


Fig. 16 - Typ. Switching Time vs. R_G
 $T_J = 150^\circ\text{C}$; $L = 680\mu\text{H}$; $V_{CE} = 600\text{V}$; $I_{CE} = 20\text{A}$; $V_{GE} = 15\text{V}$

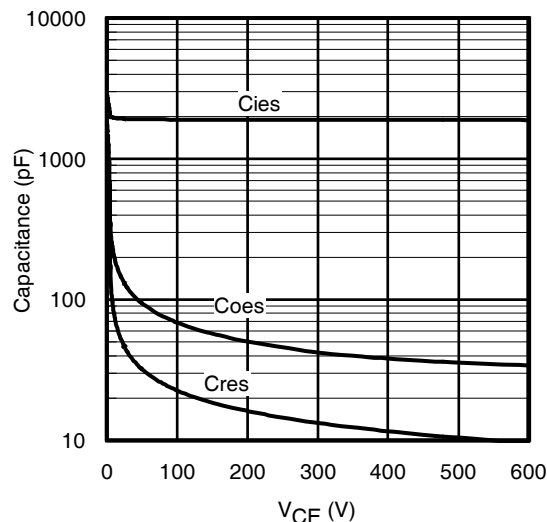


Fig. 17 - Typ. Capacitance vs. V_{CE}
 $V_{GE} = 0\text{V}$; $f = 1\text{MHz}$

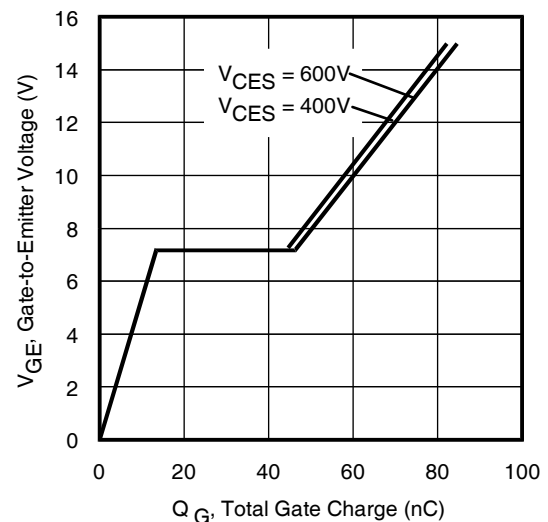


Fig. 18 - Typical Gate Charge vs. V_{GE}
 $I_{CE} = 20\text{A}$; $L = 2.4\text{mH}$

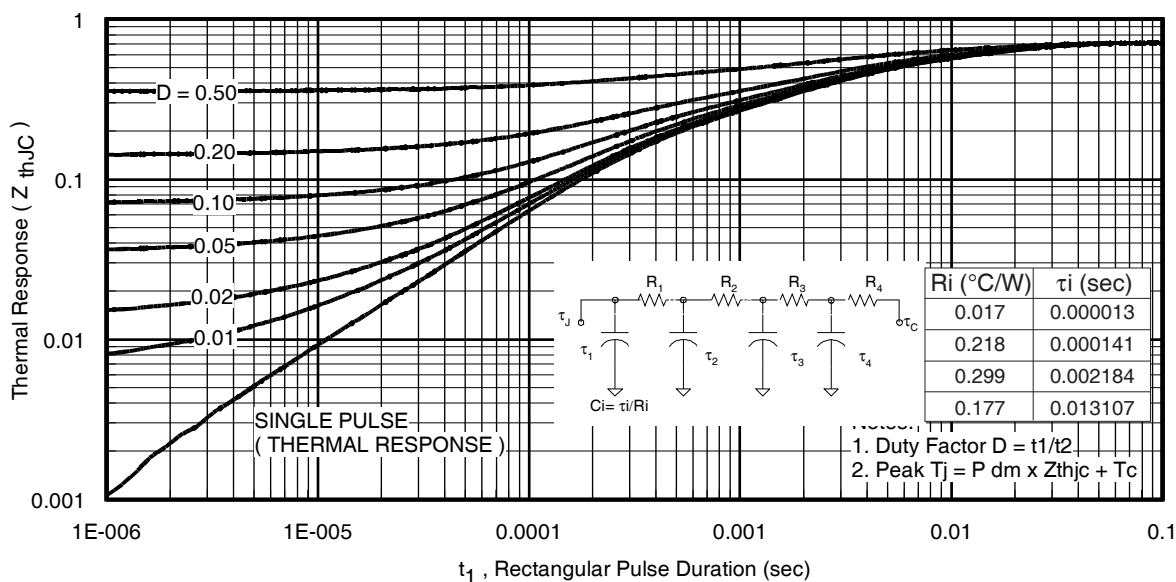


Fig 19. Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)

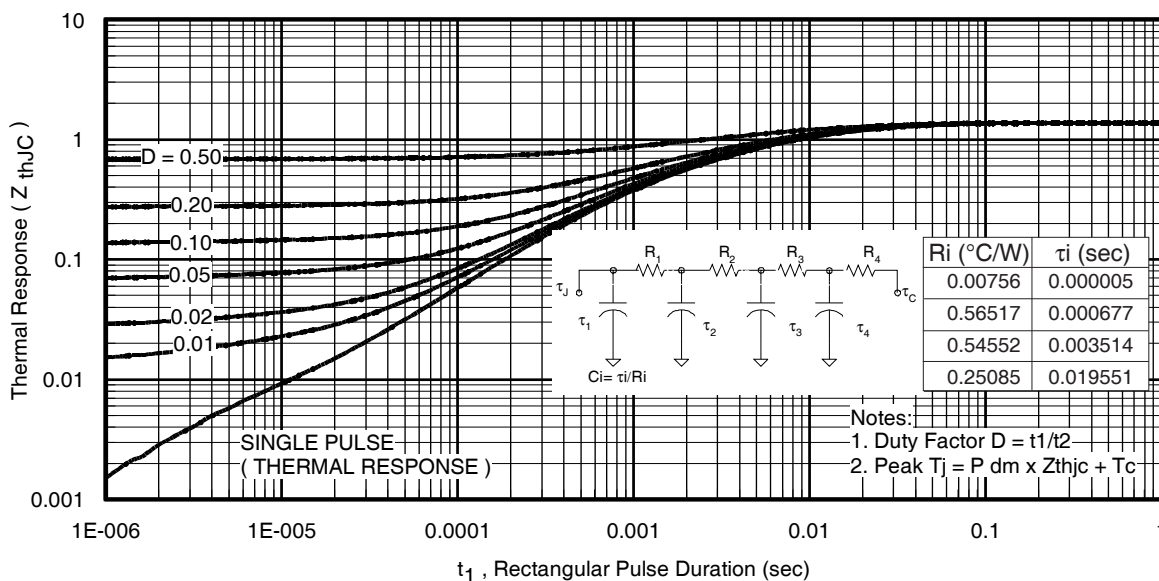


Fig. 20. Maximum Transient Thermal Impedance, Junction-to-Case (DIODE)

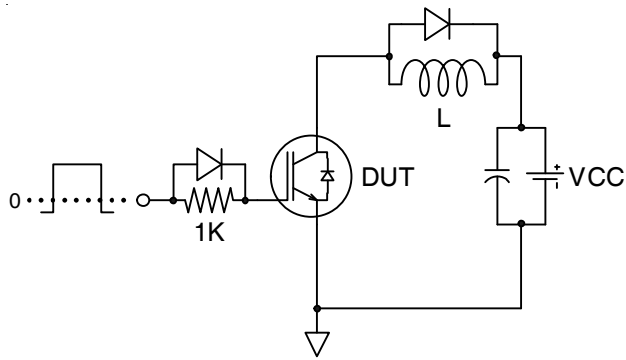


Fig.C.T.1 - Gate Charge Circuit (turn-off)

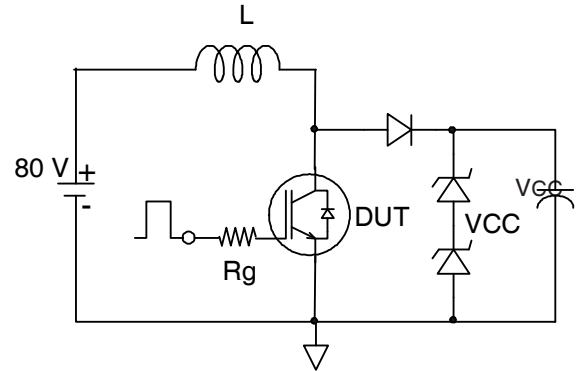


Fig.C.T.2 - RBSOA Circuit

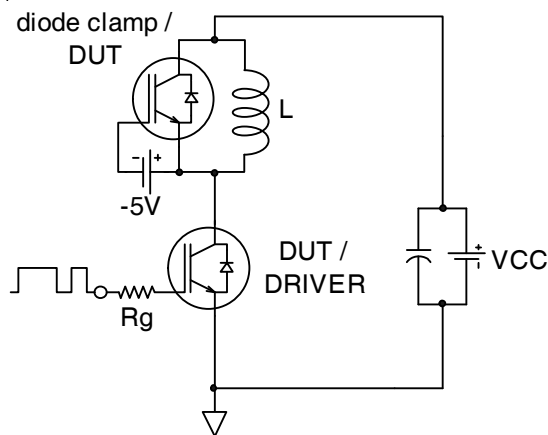


Fig.C.T.3 - Switching Loss Circuit

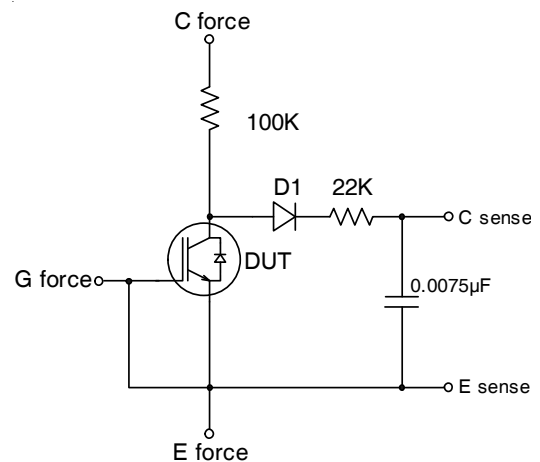


Fig.C.T.4 - BVCES Filter Circuit

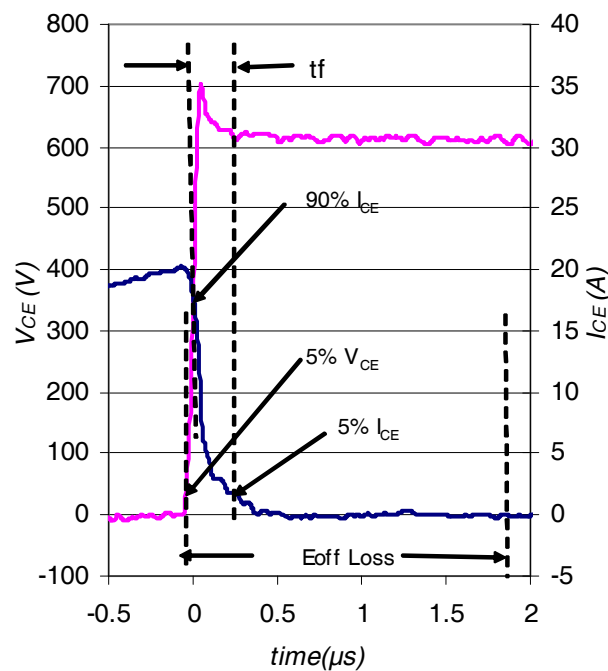
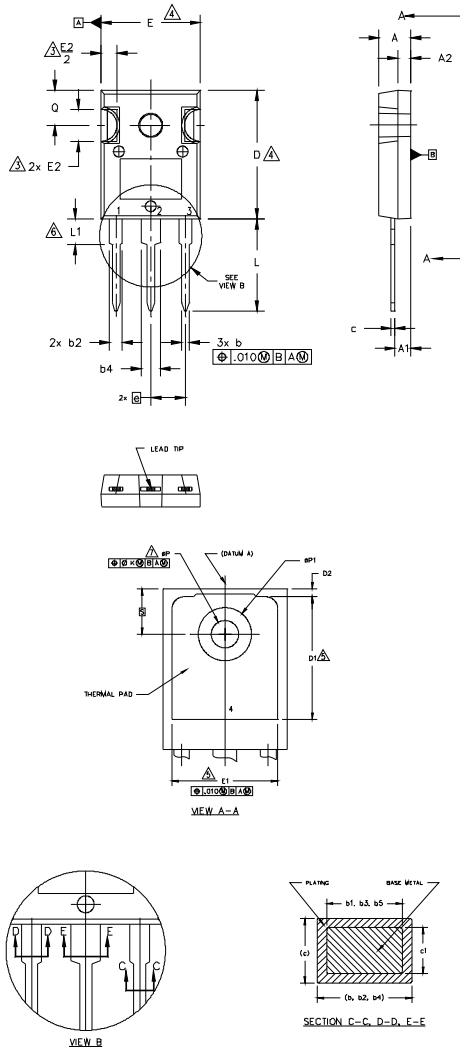


Fig. WF1 - Typ. Turn-off Loss Waveform
@ T_J = 150°C using Fig. CT.3

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	—	13.08	—	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
øP	.140	.144	3.56	3.66	
øP1	—	.291	—	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

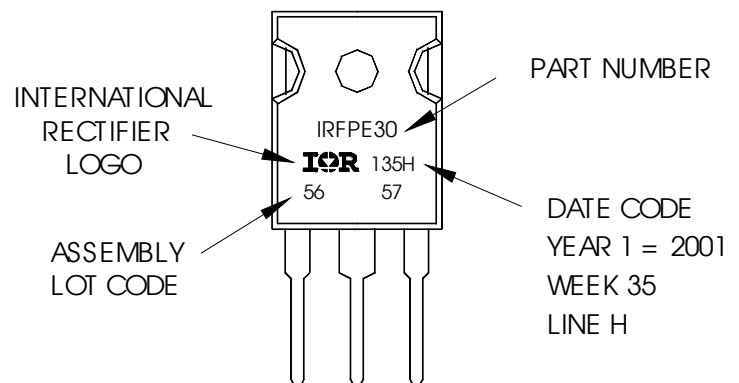
DIODES

1. ANODE/OPEN
2. CATHODE
3. ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"

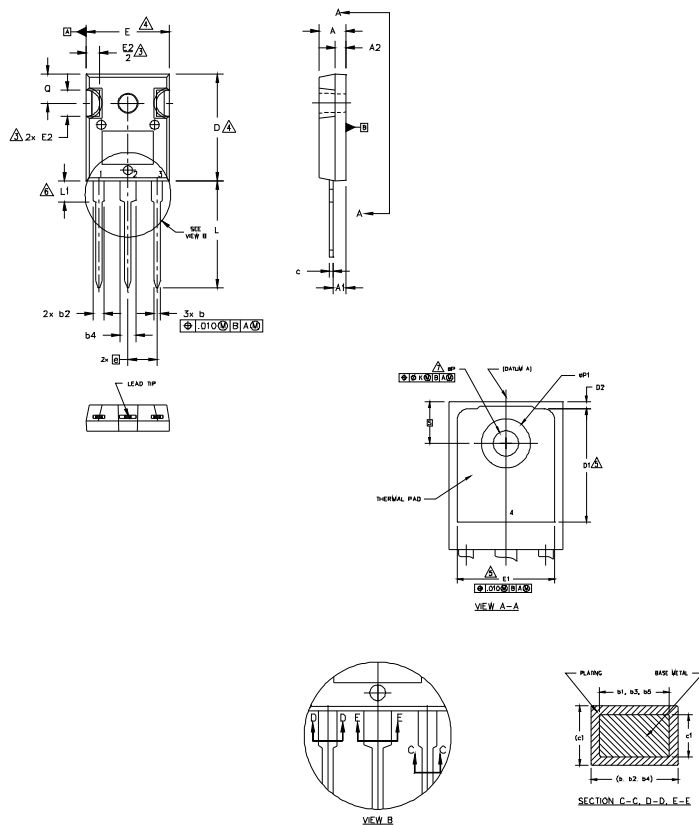


TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ϕP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	—	13.08	—	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
ϕk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
ϕP	.140	.144	3.56	3.66	
$\phi P1$	—	.291	—	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

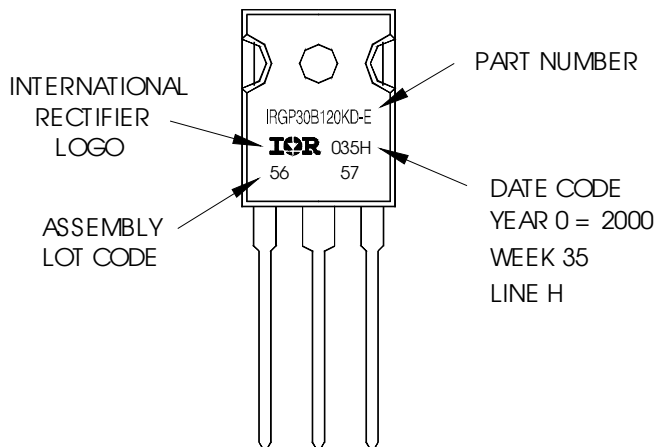
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial [†] (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	TO-247AC	N/A
	TO-247AD	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
4/19/2013	Document updated to new IR corporate template