Ordering Information

Device	Package
	16-Lead SOIC *9.90x3.90mm body* *1.75mm height (max)* *1.27mm pitch*
HV9963	HV9963NG-G

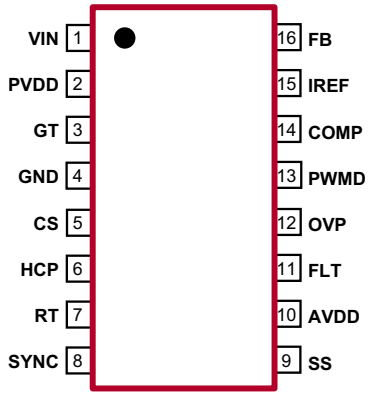
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
VIN to GND	-0.5V to +45V
PVDD to GND	-0.3V to +13V
GATE, FT to GND	-0.3V to (PV_{DD} +0.3V)
AVDD to GND	-0.3V to 6.0V
IREF to GND	-0.3V to 3.5V
All other pins to GND	-0.3V to (AV_{DD} +0.3V)
Junction temperature	+150°C
Storage ambient temperature range	-65°C to +150°C
Continuous power dissipation *(T_A = +25°C)*	1000mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

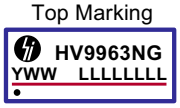
Pin Description



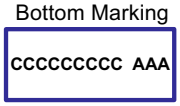
16-Lead SOIC (NG)

Product Marking

Top Marking



Bottom Marking



Y = Last Digit of Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
____ = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

16-Lead SOIC (NG)

Typical Thermal Impedance

Package	θ_{JA}
16-Lead SOIC	82°C/W

Electrical Characteristics

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{IN} = 24V, C_{PVDD} = 1.0µF, C_{AVDD} = 1.0µF, C_{GATE} = 2.0nF, C_{FLT} = 330pF unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage range	-	8.0	-	40	V	DC input voltage
I_{INSD}	Shut-down mode supply current	-	-	-	2.0	mA	PWMD to GND
Internal Regulator for GATE Drivers							
PV_{DD}	Internally regulated voltage	-	9.5	10	10.5	V	V_{IN} = 12 - 40V, R_T = 44.2kΩ, PWMD = AV_{DD}
$UVLO_{RISE}$	V_{DD} under voltage lockout threshold	*	6.55	-	7.20	V	PV_{DD} rising
$UVLO_{HYST}$	V_{DD} under voltage hysteresis	-	-	500	-	mV	PV_{DD} falling
$PV_{DD,MIN}$	Minimum V_{DD} voltage	*	8.0	-	-	V	V_{IN} = 9.0V, R_T = 44.2kΩ, PWMD = AV_{DD}

Note:

* *Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.*

Electrical Characteristics *(cont.)*

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{IN} = 24V, C_{PVDD} = 1.0µF, C_{AVDD} = 1.0µF, C_{GATE} = 2.0nF, C_{FLT} = 330pF unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Units	Conditions
Internal Low Voltage Regulator							
AV_{DD}	Internally regulated voltage	-	4.90	5.00	5.10	V	V_{IN} = 8.0 - 40V
		-	4.85	-	5.10	V	V_{IN} = 8.0 - 40V, 0°C < T_A < +85°C
		-	4.82	-	5.10	V	V_{IN} = 8.0 - 40V, -40°C < T_A < +125°C
$UVLO_{RISE}$	AV_{DD} under voltage lockout threshold	#	4.6	-	4.7	V	AV_{DD} rising
$UVLO_{HYST}$	AV_{DD} under voltage hysteresis	#	-	600	-	mV	AV_{DD} falling
I_{AVDD_ext}	External current draw	-	0	-	500	µA	---
PWM Dimming							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	0.8	V	---
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	---
R_{PWMD}	PWMD pull down resistor	-	50	100	150	kΩ	V_{PWMD} = 3.3V
GATE							
I_{SOURCE}	Short circuit current, sourcing	-	0.2	-	-	A	V_{GATE} = 0V
I_{SINK}	Sinking current	-	0.4	-	-	A	V_{GATE} = 10V
T_{RISE}	Output rise time	-	-	-	60	ns	---
T_{FALL}	Output fall time	-	-	-	60	ns	---
Over Voltage Protection							
$V_{OVP,rising}$	Over voltage rising trip point	*	1.20	1.25	1.40	V	OVP rising
$V_{OVP,HYST}$	Over voltage hysteresis	-	-	0.125	-	V	OVP falling
Hiccup Timer							
I_{HCP+}	Charging current	-	8.8	11	20	µA	HCP = GND
ΔV	Voltage swing for hiccup timer	-	-	2.0	-	V	---
I_{HCP-}	Discharging current	-	10	-	-	mA	V_{HCP} = 5.0V
Soft Start							
I_{SS+}	Charging current	-	8.8	11	20	µA	SS = GND
I_{SS-}	Discharging current	-	1.0	-	-	mA	V_{SS} = 5.0V
Slope Compensation							
R_{SLOPE}	ON resistance of FET at CS pin	*	100	300	600	Ω	---
I_{SLOPE}	Current sourced out of CS pin	-	1.8	2.0	4.0	µA	R_T = 237kΩ

Notes:

\# *Denotes specifications guaranteed by design*

* *Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.*

Electrical Characteristics *(cont.)*

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{IN} = 24V, C_{PVDD} = 1.0µF, C_{AVDD} = 1.0µF, C_{GATE} = 2.0nF, C_{FLT} = 330pF unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Units	Conditions
Current Sense							
T_{BLANK}	Leading edge blanking	*	100	-	300	ns	---
T_{DELAY1}	Delay to output of output comparator	-	-	-	200	ns	COMP = AV_{DD}, 50mV overdrive at CS
R_{div}	Internal resistor divider ratio – COMP to CS	#	-	0.0833	-	-	---
V_{OFFSET}	Comparator offset voltage	-	-20	-	+20	mV	---
Internal Transconductance Opamp							
GB	Gain-bandwidth product	#	-	1.0	-	MHz	150pF capacitance at COMP pin
A_V	Open loop DC gain	-	65	-	-	dB	Output open
Internal Transconductance Opamp							
V_{CM}	Input common-mode range	#	-0.3	-	3.0	V	---
V_O	Output voltage range	#	0.7	-	AV_{DD}-0.7	V	---
G_m	Transconductance	-	1600	2000	2400	µA/V	---
V_{OFFSET}	Input offset voltage	*	-3.0	-	+3.0	mV	I_{REF} = 200mV
I_{COMP_SINK}	COMP sink current	#	-0.2	-	-	mA	V_{FB} = AV_{DD}, V_{IREF} = 0, V_{COMP} = 0
I_{COMP_SOURCE}	COMP source current	#	0.2	-	-	mA	V_{FB} = 0V, V_{IREF} = 3.0V, V_{COMP} = A_{VDD} - 0.7V
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
$I_{COMP,DIS}$	Discharging current	-	1.0	-	-	mA	V_{COMP} = 5.0V
Oscillator							
f_{OSC1}	Oscillator frequency	*	88	100	112	kHz	R_T = 237kΩ
f_{OSC2}	Oscillator frequency	*	460	520	580	kHz	R_T = 44.2kΩ
F_{OSC}	Output frequency range	#	-	-	600	kHz	---
D_{MAX}	Maximum duty cycle	*	87	-	94	%	---
V_{SYNCH}	SYNC input high	-	2.0	-	-	V	---
V_{SYNCL}	SYNC input low	-	-	-	0.8	V	---
$I_{OUTSYNC}$	SYNC output current	-	-	25	-	µA	---
I_{INSYNC}	SYNC input current	-	0	-	200	µA	---

Notes:

 # Denotes specifications guaranteed by design

** Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.*

Electrical Characteristics *(cont.)*

*(The * denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, otherwise the specifications are at T_A = 25°C. V_{IN} = 24V, C_{PVDD} = 1.0µF, C_{AVDD} = 1.0µF, C_{GATE} = 2.0nF, C_{FLT} = 330pF unless otherwise noted.)*

Sym	Description		Min	Typ	Max	Units	Conditions
Output Short Circuit							
G_{SC}	Gain for short circuit comparator	-	1.8	2.0	2.4	-	---
$V_{DISABLE}$	Voltage at IREF pin to disable the short circuit comparator	-	1.19	1.25	1.31	V	PWMD = V_{DD}; F_B = 3.2V; FLT is HIGH
V_{OMIN}	Minimum output voltage of the gain stage	*	0.14	0.20	0.30	V	I_{REF} = GND
T_{OFF}	Propagation time for short circuit detection	-	-	-	250	ns	PWMD = V_{DD}, I_{REF} = 400mV; FB step from 0 to 900mV; FLT goes from high to low; no capacitance at FLT pin
$T_{RISE,FAULT}$	Fault output rise time	-	-	-	500	ns	---
$T_{FALL,FAULT}$	Fault output fall time	-	-	-	300	ns	---
$T_{BLANK,SC}$	Blanking time	*	400	-	800	ns	---

Note:

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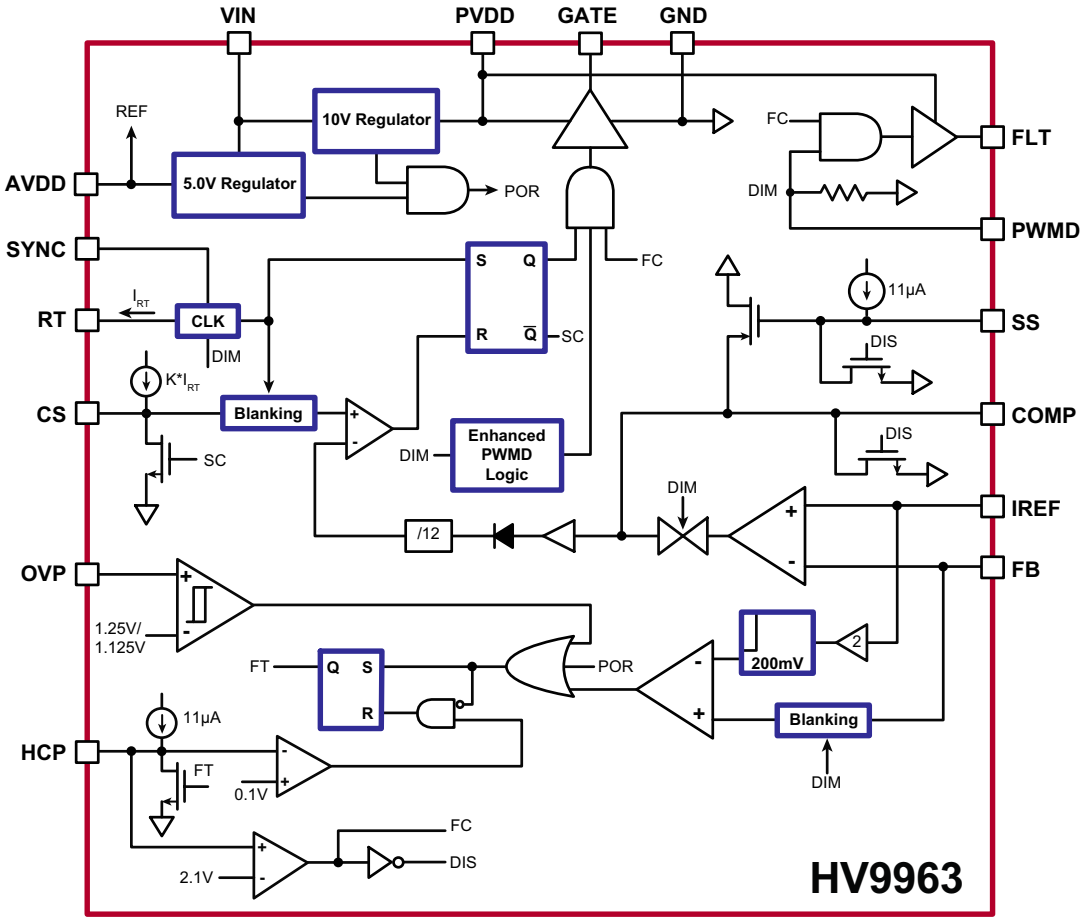
Functional Block Diagram



Power Topology

The HV9963 is a switch-mode LED driver designed to control a buck, boost or SEPIC converter in a constant frequency mode. The IC includes internal linear regulators, which enables it to operate at input voltages from 9 to 40V. The IC includes features typically required in LED drivers like open LED protection, output short circuit protection, linear and PWM dimming and accurate control of the LED current. It also includes logic to enable enhanced PWM dimming which allows dimming ratios in excess of 5000:1.

Power Supply to the IC (VIN, PVDD and AVDD)

The HV9963 can be powered directly from its VIN pin that takes a voltage up to 40V. There are two linear regulators within the HV9963 – a 10V linear regulator (PVDD), which is used for the two FET drivers, and a 5.0V linear regulator (AVDD) which supplies power to the rest of the control logic. The IC also has a built in under-voltage lockout which shuts off the IC if the voltage at either VDD pin falls below its UVLO threshold.

Both VDD pins must by bypassed by a low ESR capacitor (≥ 0.1µF) for proper operation.

The input current drawn from the external power supply (or VIN pin) is a sum of the 1.5mA (max) current drawn by the all the internal circuitry and the current drawn by the gate driver (which in turn depends on the switching frequency and the gate charge of the external FET).

$$I_{IN} = 1.5mA + Q_{g1} \bullet f_S + Q_{g2} \bullet f_{PWMD}$$

In the above equation, fs is the switching frequency of the converter, f_{PWMD} is the frequency of the applied PWM dimming signal, Q_{g1} is the gate charge of the external boost FET and Q_{g2} is the gate charge of the disconnect FET (both of which can be obtained from the FET datasheets).

The AVDD pin can also be used as a reference voltage to set the LED current using a resistor divider to the IREF pin.

Timing Resistor (RT)

The switching frequency of the converter is set by connecting a resistor between RT and GND. The resistor value can be determined as:

$$R_T \approx \frac{1}{43pF \bullet f_S} - 322\Omega$$

The oscillator is also timed to the PWM dimming signal to improve the PWM dimming performance. The oscillator is turned off when PWMD is low and is enabled when PWMD goes high.

Current Sense (CS)

The current sense input is used to sense the source current of the switching FET. The CS input of the HV9963 includes a built in 100ns (minimum) blanking time to prevent spurious turn off due to the initial current spike when the FET turns on.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pins by a factor of 12 (11R:1R). This voltage is used as the reference for the current sense comparators. Since the maximum voltage of the COMP pin is AVDD - 0.7V, this voltage determines the maximum reference current for the current sense comparator and thus the maximum inductor current.

The current sense resistor R_{CS} should be chosen so that the input inductor current is limited to below the saturation current level of the input inductor. For discontinuous conduction mode of operation, no slope compensation is necessary. In this case, the current sense resistor is chosen as:

$$R_{CS} = \frac{AV_{DD} - 0.7V}{12 \bullet I_{SAT}}$$

where I_{SAT} is the maximum desired peak inductor current.

For continuous conduction mode converters operating in the constant frequency mode, slope compensation becomes necessary to ensure stability of the peak current mode controller, if the operating duty cycle is greater than 0.5. This factor must also be accounted for when determining R_{CS} (see Slope Compensation section).

Slope Compensation

Choosing a slope compensation that is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

Slope compensation in the HV9963 can be programmed by one external capacitor in series with the CS pin (see Figure 1). A current, proportional to the switching frequency, is sourced out of the CS pin.

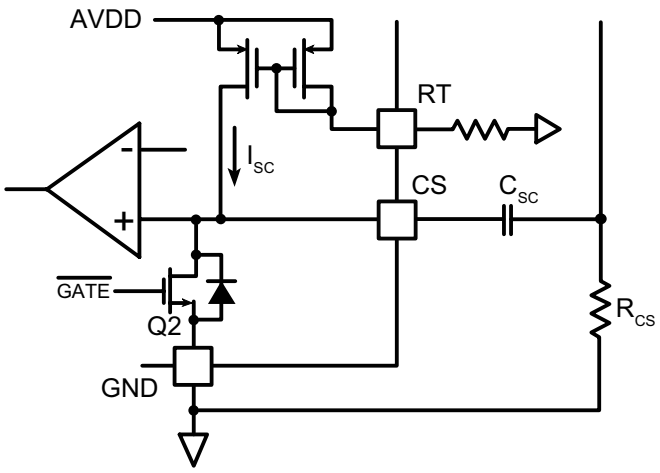


Figure 1: Slope Compensation circuit

$$I_{SC} = 2\mu A \bullet \frac{f_S}{100kHz}$$

This current flows into the capacitor and produces a ramp voltage across the capacitor. The voltage at the CS pin is then the sum of the voltage across the capacitor and the voltage across the current sense resistor, with the voltage across the capacitor providing the required slope compensation. When the GATE turns off, an internal pull down FET discharges the capacitor.

Assuming a down slope of DS (A/µs) for the inductor current, the current sense resistor can be computed as:

$$R_{CS} = \frac{AV_{DD} - 0.9V}{12} \bullet \frac{1}{\frac{D_S \bullet 10^6 \bullet 0.93}{2 \bullet f_S} + I_{SAT}}$$

The slope compensation capacitor is chosen to provide the required amount of slope compensation required to maintain stability.

$$C_{SC} = \frac{I_{SC}}{DS/2 \bullet R_{CS}}$$

Note: *Sometimes, excessive stray inductance in the current sense path might cause the slope compensation circuit to mis-trigger. The following section describes the cause of the problem and the solution.*

Figure 2 shows the detailed slope compensation circuit with a parasitic inductance L_P between the ground of the boost converter and the ground of the HV9963. Also shown is the drain capacitance of the boost FET Q1 (which is the total capacitance at the drain node).

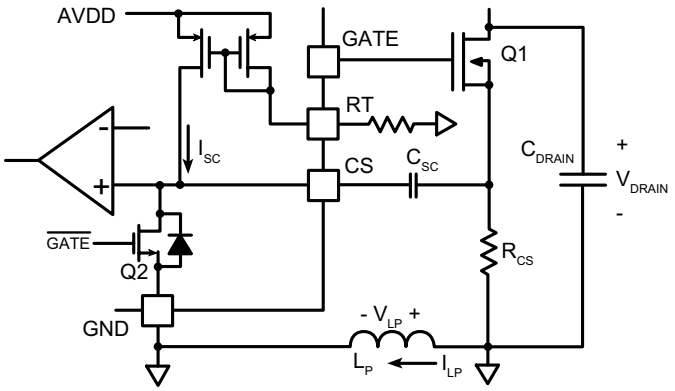


Figure 2: Slope Compensation circuit with parasitics

When the FET Q1 is off, the internal discharge to FET Q2 is turned on and capacitor C_{SC} is discharged. Also, C_{DRAIN} is charged to the output voltage V_O. When the FET Q1 is turned on, the drain node of the FET is pulled to ground (Q2 is turned off just prior to Q1 being turned on). This causes the drain capacitance to discharge through the FET Q1, causing a current spike as shown in Figure 3. This current spike causes a voltage to develop across the parasitic inductance. As long as the current is increasing through the inductance, the voltage developed across the inductor is successfully blocked by the body diode of Q2. However, during the falling edge of the current spike, the voltage across the inductor causes the body diode to become forward biased. This conduction path through the body diode of Q2 causes pre-charge of C_{SC}. The pre-charge voltage can be fairly high since the current's rate of fall is very large.

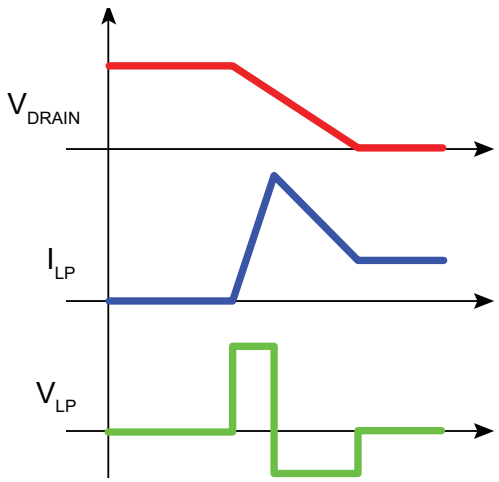


Figure 3: Waveforms during turn-on

For example, a typical current spike usually lasts about 100ns. Assuming a 3A peak current (this value is usually the saturation current of the FET which can be much higher) and

equal distribution between the rise and fall times, a 10nH parasitic inductance causes a pre-charge voltage of:

$$V_{PRE\text{-}CHARGE} = 10nH \bullet \frac{3A}{50ns} = 600mV$$

As can be seen, a very conservative estimate of the pre-charge voltage is already larger than the steady state peak current sense voltage and will cause the converter to falsely trip.

To prevent this behavior, a resistor (typically 500 – 800Ω) can be added in series with the capacitor as shown in Figure 4. This resistor limits the charging current into the capacitor. However, the resistor will also slow down the discharge of the capacitor during the FET off time, so the maximum external resistance will be limited by the switching frequency and the slope compensation capacitor.

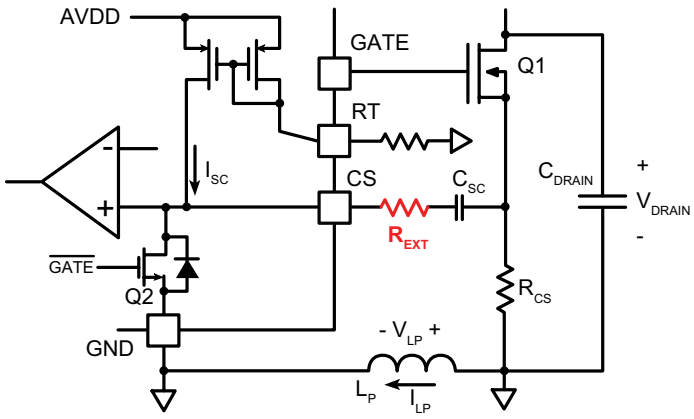


Figure 4: Modified Slope compensation circuit

$$R_{ext,max} = \frac{1}{3} \bullet \frac{0.07}{f_S} \bullet \frac{1}{C_{SC}} - 600\Omega$$

FLT Output

The FLT pin is used to drive a disconnect FET when driving boost and SEPIC converters. In the case of boost converters, when there is a short circuit fault at the output, there is a direct path from the input source to ground which can cause high currents to flow. The disconnect switch is used to interrupt this path and prevent damage to the converter.

The disconnect switch also helps to disconnect the output filter capacitors for the boost and SEPIC converters from the LED load during PWM dimming and enables a very high PWM dimming ratio.

Control of the LED Current (IREF, FDBK and COMP)

The LED current in the HV9963 is controlled in a closed-loop manner. The current reference which sets the three LED currents at the IREF pin is set by using a resistor divider from the AVDD pin (or can be set externally with a low voltage source). This reference voltage is compared to the voltage at the FDBK pin which senses the LED current by using current sense resistors. HV9963 includes a 1.0MHz transconductance amplifier with tri-state output, which is used to close the feedback loops and provide accurate current control. The compensation network is connected at the COMP pin.

The output of the op-amp is buffered and connected to the current sense comparator using a 11R:1R resistor divider.

The output of the op-amp is also controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the op-amp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal has turned off the gate drive. When the IC is enabled, the voltage on the integrating capacitor will force the converter into a steady state almost instantaneously.

Note: *The absolute maximum voltage rating of the IREF pin is 3.5V and the voltage applied at this pin should not exceed this rating.*

Soft Start (SS)

Soft start of the LED current can be achieved by connecting a capacitor at the SS pin. The rate of rise of SS pin limits the LED current's rate of rise.

Upon start-up, the capacitance at the COMP network is being charged by the 200µA sourcing current of the transconductance amplifier. Without the soft-start function, this larger current would cause the COMP voltage to increase faster than the boost converter's response time, causing overshoots in the LED current during start-up.

The SS pin is used to prevent these LED current overshoots by limiting the COMP pin's rate of rise . A capacitor at the soft start pin programs the voltage's rate of rise at the pin. The SS pin holds the COMP pin to 1.0V above the SS pin and thereby controls the COMP pin's rate of rise. The COMP pin is released once the voltage reaches its steady state voltage.

If the steady state voltage at the COMP pin ($V_{COMP(SS)}$) and the desired rate of rise of the LED current (T_{RISE}) is known, the capacitance required at the SS pin can be computed as:

$$C_{SS} = \frac{11\mu A \bullet T_{RISE}}{V_{COMP(SS)} - 1V}$$

Linear Dimming

Linear Dimming can be accomplished in the HV9963 by varying the voltages at the IREF pin. Note that since the HV9963 is a peak current mode controller, it has a minimum on-time for the GATE output. This minimum on-time will prevent the converter from completely turning off even when the IREF pin is pulled to GND. Thus, linear dimming cannot accomplish true zero LED current. To get zero LED current, PWM dimming has to be used.

Due to the offset voltage of the short circuit comparator as well as the non-linearity of the X2 gain stage, pulling the IREF pin very close to GND might trigger the internal short circuit comparator and shut down the IC. To overcome this, the output of the gain stage is limited to 140mV (minimum), allowing the IREF pin to be pulled all the way to 0V without triggering the short circuit comparator.

PWM Dimming (PWMD)

PWM dimming in the HV9963 can be accomplished using a TTL compatible square wave source at the PWMD pin.

The HV9963 has an enhanced PWM dimming capability, which allows PWM dimming to widths less than one switching cycle with no drop in the LED current.

The enhanced PWM dimming performance of the HV9963 can be best explained by considering typical boost converter circuits without this functionality. When the PWM dimming pulse becomes very small (less than one switching cycle for a DCM design or less than five switching cycles for a CCM design), the boost converter is turned off before the input current can reach its steady state value. This causes the input power to droop, which is manifested in the output as a droop in the LED current (Figure. 5; for a CCM design).

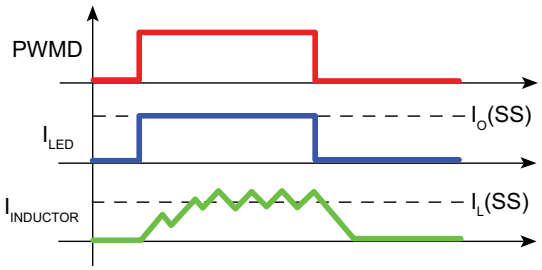


Figure 5a: PWM Dimming with dimming on-time far greater than one switching time period

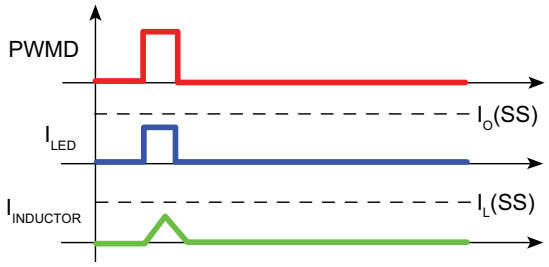


Figure 5b: PWM Dimming with dimming on-time equal to one switching time

In the above figures, I_O(SS) and I_L(SS) refer to the steady state values (PWMD = 100%) for the output current and inductor current respectively. As can be seen, the inductor current does not rise enough to trip the CS comparator. This causes the closed loop amplifier to lose control of the LED current and COMP rails to VDD.

In the HV9963, however, this problem is overcome by keeping the boost converter ON, even though PWMD has gone to zero to ensure enough power is delivered to the output. Thus, the amplifier still has control over the LED current and the LED current will be in regulation as shown in Figure. 6.

When the PWM signal is high, the GATE and FLT pins are enabled and the output of the transconductance op-amp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The FLT pin goes low, turning off the disconnect switch. However, the boost FET is kept running.

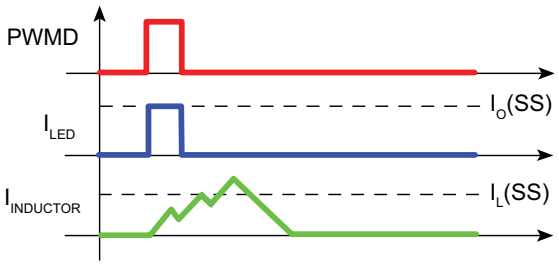


Figure 6: PWM Dimming with dimming on-time equal to one switching time period with the HV9963

Note that disconnecting the LED load during PWM dimming causes the energy stored in the inductor to be dumped into the output capacitor. The chosen filter capacitor should be large enough so that it can absorb the inductor energy without significant change of the voltage across it. If the capacitor voltage change is significant, it would cause a turn-on spike in the inductor current when PWMD goes high.

Fault Conditions and Hiccup Timer (OVP, HCP)

The HV9963 is a robust controller which can protect the LEDs and the LED driver in case of fault conditions. The HV9963 includes both open LED protection and output short circuit protection. In both cases, the HV9963 shuts down and attempts a restart. The hiccup time is programmed by the capacitor at the HCP pin.

When a fault condition is detected, both GATE and FLT outputs are disabled and the COMP, SS and HCP pins are pulled to GND. Once the voltage at the HCP pin falls below 0.1V and the fault condition(s) have disappeared, the capacitor at the HCP pin is released and is charged slowly by a 11µA current source. Once the capacitor is charged to 2.1V, the COMP and SS pins are released and GATE and FLT pins are allowed to turn on. Then, the converter will go into a soft-start mode ensuring a smooth recovery for the LED current.

Hiccup Timer (HCP)

The value of the capacitor required for a given hiccup time is given by:

$$C_{HCP} = \frac{11\mu A \bullet T_{HCP}}{2V}$$

Short Circuit Protection

When a short circuit condition is detected (output current becomes higher than twice the steady state current), the GATE and FLT outputs are pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and the short circuit condition disappears. At this time, the hiccup timer is started. Once the timing is complete, the converter attempts to restart. If the fault condition still persists, the converter shuts down and goes through the cycle again. If the fault condition is cleared (due to a momentary output short) the converter will start regulating the output current normally. This allows the LED driver to recover from accidental shorts without having to reset the IC.

Note that the power rating of the LED sense resistor has to be chosen properly if it has to survive a persistent fault condition. The power rating can be determined using:

$$P_{RS} \geq \frac{I_{SAT}^2 \bullet R_S \bullet (T_{FAULT} + T_{OFF})}{t_{HICCUP}}$$

Where I_{SAT} is the saturation current of the disconnect FET. In the case of the HV9963, (T_{FAULT} + T_{OFF}) is 550ns (max).

False Triggering of the Short Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string might cause a spike in the output current when the disconnect FET is turned on. If this spike is detected by the short circuit comparator, it will cause the IC to falsely detect an over current condition and shut down.

In the HV9963, to prevent these false triggers, there is a built in 500ns blanking network for the short circuit comparator. This blanking network is activated when the PWMD input goes high. Thus, the short circuit comparator will not see the spike in the LED current during the PWM dimming turn-on transition. Once the blanking timer is completed, the short circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short circuit will depend on the condition of the PWMD input.

If the output short circuit exists before the PWM dimming signal goes high, the total detection time will be:

$$t_{DETECT1} = t_{BLANK} + t_{DELAY} \approx 1050ns(max)$$

If the short circuit occurs when the PWM dimming signal is already high, the time to detect will be:

$$t_{DETECT1} = t_{DELAY} \approx 250ns(max)$$

Over Voltage Protection

The HV9963 provides hysteretic over voltage protection allowing the IC to recover in case the LED load is disconnected momentarily.

When the load is disconnected in a boost converter, the output voltage rises as the output capacitor starts charging. When the output voltage reaches the OVP rising threshold, the HV9963 detects an over voltage condition and turns off the converter. The converter is turned back on only when the output voltage falls below the falling OVP threshold (which is 10% lower than the rising threshold). This time is mostly dictated by the R-C time constant of the output capacitor C_O and the resistor network used to sense over voltage (R_{OVP1} + R_{OVP2}). In case of a persistent open circuit condition, this cycle keeps repeating; maintaining the output voltage within a 10% band.

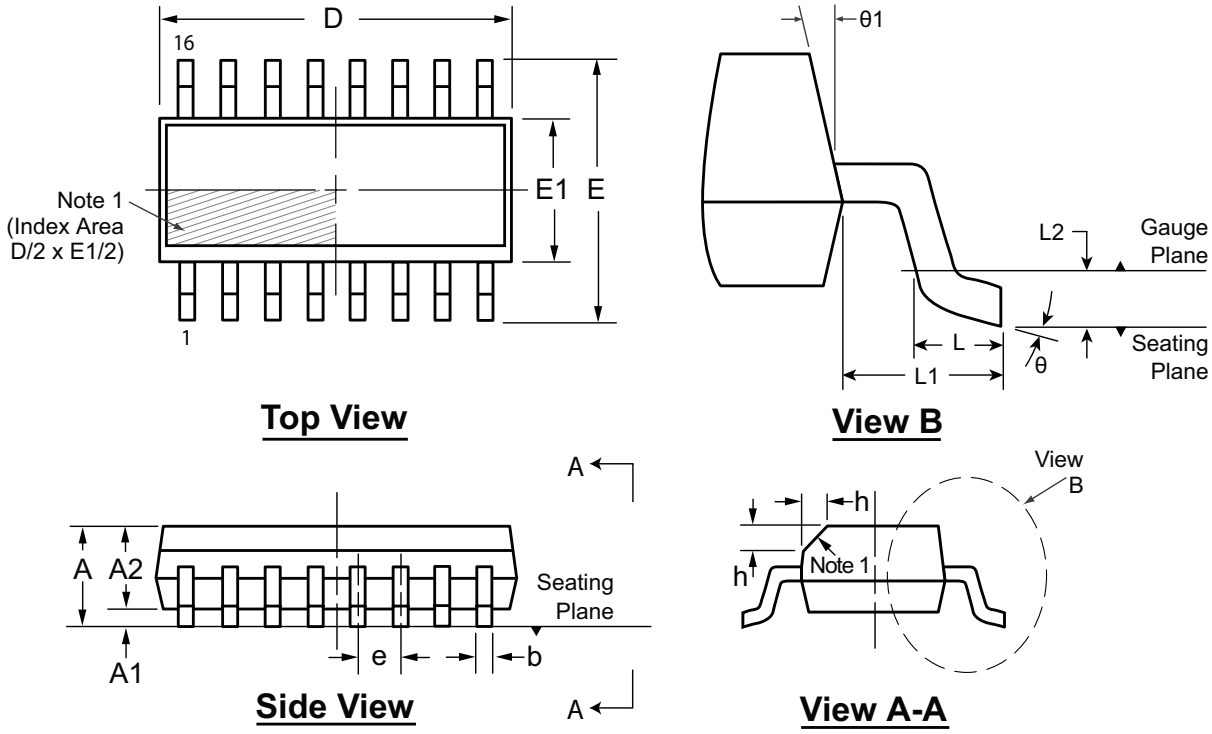
In most designs, the lower threshold voltage of the over voltage protection (V_{OVP} – 10%) -- the point at which the HV9963 attempts to restart-- will be more than the LED string voltage. Thus, when the LED load is reconnected to the output of the converter, the voltage differential between the actual output voltage and the LED string voltage will cause a spike in the output current. This causes a short circuit to be detected and the HV9963 will trigger short circuit protection. This behavior continues until the output voltage becomes lower than the LED string voltage at which point, no fault will be detected and normal operation of the circuit will commence.

Pin Description

Pin #	Name	Description
1	VIN	This pin is the input of a 40V high voltage regulator, and should not be left unconnected. If a voltage at PVDD is being applied from an external power supply, the VIN and PVDD pins should be shorted.
2	PVDD	This pin is a regulated 10V supply for the two gate drivers (FLT and GATE). It must be bypassed with a low ESR capacitor to GND (at least 1.0µF).
3	GATE	This is the GATE driver output for the switching FET.
4	GND	Ground return for all the low power analog internal circuitry as well as the gate drivers. This pin must be connected to the return path from the input.
5	CS	This pin is used to sense the source current of the external power FET. It includes a built-in 100ns (min) blanking time.
6	HCP	This pin provides the hiccup timer in case of a fault. A capacitor at this pin programs the hiccup time.
7	RT	This pin sets the frequency of the power circuit. A resistor between RT and GND will program the circuit in constant frequency mode. The switching frequency is synchronized to the PWMD input and oscillator will turn on once PWMD goes high.
8	SYNC	This I/O pin may be connected to the SYNC pin of other HV9963 circuits and will cause the oscillators to lock to the highest frequency oscillator.
9	SS	This pin is used to provide soft start upon turn-on of the IC. A capacitor at this pin programs the soft start time.
10	AVDD	This is a power supply pin for all internal control circuits. This voltage is also used as the reference voltage both internally and externally. It must be bypassed with a low ESR capacitor to GND (at least 0.1µF).
11	FLT	This pin is used to drive an external disconnect FET which disconnects the load from the circuit during a fault condition or during PWM dimming to achieve a very high dimming ratio.
12	OVP	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 1.25V, the gate output of the HV9963 is turned off and FLT goes low. The IC will turn on when the voltage at the pin goes below 1.125V.
13	PWMD	When this pin is pulled to GND (or left open), switching of the HV9963 is disabled. When an external TTL high level is applied to it, switching will resume.
14	COMP	Stable Closed loop control can be accomplished by connecting a compensation network between COMP and GND.
15	IREF	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the AVDD pin. Connecting a voltage greater than 1.25V at this pin will disable the short circuit comparator.
16	FB	This pin provides output current feedback to the HV9963 by using a current sense resistor.

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0^O	5^O
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8^O	15^O

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-16SONG, Version G041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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