Table of Content

1 FEATURES

- Industry-standard Microwire Interface
- Wide-voltage Operation
  - Vcc = 1.8V to 5.5V
- Speed
  - 1 MHz (1.8V), 2 MHz (2.5V), 3 MHz (5.5V)
- Standby current
  - 1uA (max.) 1.8V
- Operating current
  - 1mA (max.) 1.8V
- User Configured Memory Organization
  - 256x16-bit (ORG = Vcc or Floating) or 512x8-bit (ORG = 0V)
- Self timed write cycle: 5 ms (max.)
- Hardware and software write protection
  - Defaults to write-disabled state at power-up
  - Software instructions for write-enable/disable
- CMOS technology
- Versatile, easy-to-use interface
  - Automatic erase-before-write
  - Programming status indicator
  - Byte, Word and chip single erasable
  - Chip select enables power savings
- Noise immunity on inputs, besides Schmitt trigger
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 100 years
- Packages: SOIC/SOP, TSSOP, and UDFN
- Lead-free, RoHS, Halogen free, Green

2 DESCRIPTION

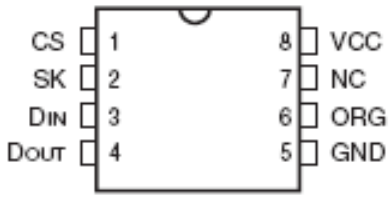
The GT93C66A is 4kb non-volatile serial EEPROM with memory array of 4,096 bits. The array can be organized as either 512 bytes of 8 bits or 256 words of 16 bits via the ORG control. Utilizing the CMOS design and process, these products provide low standby current and low power operations. The devices can operate in a wide supply voltage range from 1.8V to 5.5V, with frequency up to 3MHz.

When the ORG pin is connected to Vcc or floating, x16 is selected. Conversely, when it is connected to ground, x8 is chosen.

An instruction Op-code defines the various operations of the devices, including read, write, and mode-enable functions. To protect against inadvertent data modification, all write and erase instructions are merely accepted while the device is in write enable mode. A selected x8 byte or x16 word can be modified with a single WRITE or ERASE instruction. Additionally, the WRITE ALL or ERASE ALL instruction can program or erase the entire array, respectively. Once a device begins its self-timed program procedure, the data out pin (Dout) can indicate the READY/**BUSY** status by raising chip select (CS). The devices can output any number of consecutive bytes/words using a single READ instruction.

3 PIN CONFIGURATION

8-Pin SOIC/SOP, TSSOP



8-pad UDFN

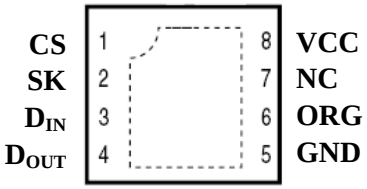
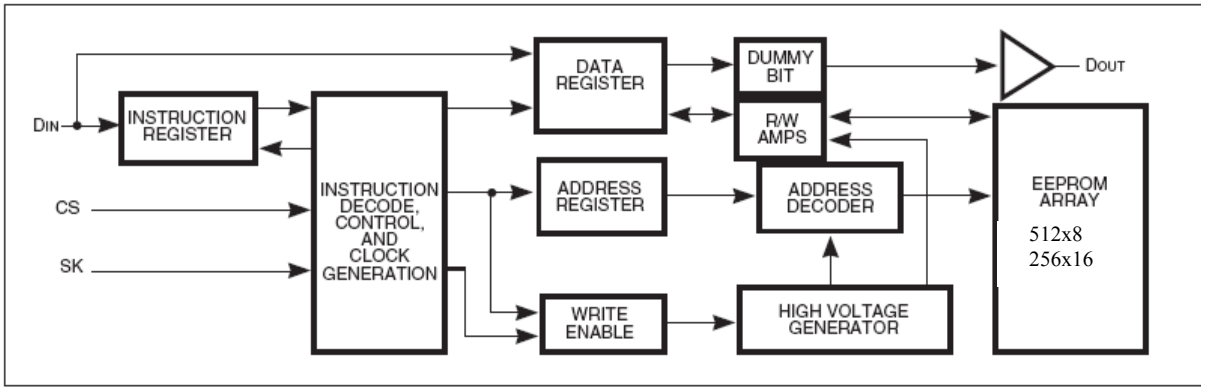


Table 3.1: Pin Descriptions

Pin Name	Descriptions
CS	Chip Select
SK	Serial Data Clock
D_{IN}	Serial Data Input
D_{OUT}	Serial Data Output
GND	Ground
ORG	Organization Select
NC	Not Connect
V_{CC}	Supply Voltage

4 BLOCK DIAGRAM



5 DEVICE OPERATION

Device Operations

The GT93C66A is controlled by a set of instructions which are clocked-in serially on the Din pin. Before each low-to-high transition of the clock (SK), the CS pin must have already been raised to HIGH, and the Din value must be stable at either LOW or HIGH. Each instruction begins with a start bit of the logical "1" or HIGH. Following this are the Op-code, address field, and data, if appropriate. The clock signal may be held stable at any moment to suspend the device at its last state, allowing clock speed flexibility. Upon completion of bus communication, CS would be pulled LOW. The device then would enter Standby mode if no internal programming is underway.

Read (READ)

The READ instruction is the only instruction that outputs serial data on the DOUT pin. After the read instruction and address have been decoded, data is transferred from the selected memory array into a serial shift register. (Please note that one logical "0" bit precedes the actual 8 or 16-bit output data string.) The output on DOUT changes during the low-to-high transitions of SK (see Figure 3).
The GT93C66A is designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 8 or 16 bits of the addressed register have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the chip select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done. When Vcc is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter, the device remains enabled until a WDS instruction is executed or until Vcc is removed. (See Figure 4.) (Note: Chip select must remain LOW until Vcc reaches its operational value.)

Write Disable (WDS)

The write disable (WDS) instruction disables all programming capabilities. This protects the entire device against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation.

Write (WRITE)

The WRITE instruction writes 8 or 16 bits of data into the specified memory location. After the last data bit has been applied to DIN, and before the next rising edge of SK, CS must be brought LOW. If the device is write-enabled, then the falling edge of CS initiates the self-timed programming cycle (see WEN). If CS is brought HIGH, after a minimum wait of 200 ns after the falling edge of CS (t_{CS}) DOUT will indicate the READY/**BUSY** status of the chip. Logical "0" means programming is still in progress; logical "1" means the selected memory array has been written, and the part is ready for another instruction (see Figure 5). The READY/**BUSY** status will not be available if the CS input goes HIGH after the end of the self-timed programming cycle (t_{WP}).

Write All Memory (WRAL)

The write all (WRALL) instruction programs entire memory with the data pattern specified in the instruction. As with the WRITE instruction, the falling edge of CS must occur to initiate the self-timed programming cycle. If CS is then brought HIGH after a minimum wait of 200 ns (t_{CS}), the DOUT pin indicates the READY/**BUSY** status of the chip (see Figure 6).

Erase (ERASE)

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DOUT to indicate the READ/**BUSY** status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction (see Figure 8).

Erase All Memory (ERAL)

Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1" (see Figure 9).

Power-On Reset (POR)

The device incorporates a Power-On Reset (POR) circuitry which protects the internal logic against powering up into a wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This POR feature protects the device being 'brown-out' due to a sudden power loss or power cycling.

In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset (POR) circuit is embedded. During power-up, the device does not respond to any instruction until V_{CC} has reached a minimum stable level above the reset threshold voltage. Once V_{CC} passes the POR threshold, the device is reset and enters in Standby mode. This can also avoid any inadvertent Write operations during power-up stage. During power-down process, the device must enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will enter standby mode after current operation completes, provided that no internal write operation is in progress.

INSTRUCTION SET - GT93C66A (4Kb)

Instruction [2]	Start Bit	OP Code	8-bit Organization (ORG = GND)			16-bit Organization (ORG = Vcc or Floating)		
			Address[1]	Data[1]	Required Clock Cycles	Address[1]	Data[1]	Required Clock Cycles
WDS (Write Disable)	1	00	0 0xxx xxxx	—	12	00xx xxxx	—	11
WEN (Write Enable)	1	00	1 1xxx xxxx	—	12	11xx xxxx	—	11
ERAL (Erase All Memory)	1	00	1 0xxx xxxx	—	12	10xx xxxx	—	11
WRAL (Write All Memory)	1	00	0 1xxx xxxx	(D_7-D_0)	20	01xx xxxx	(D_{15}-D_0)	27
WRITE	1	01	(A_8-A_0)	(D_7-D_0)	20	(A_7-A_0)	(D_{15}-D_0)	27
READ	1	10	(A_8-A_0)	—		(A_7-A_0)	—	
ERASE	1	11	(A_8-A_0)	—	12	(A_7-A_0)	—	11

Notes:
1. x = Don't care bit.
2. Exact number of clock cycles is required for each Op-code instruction.

6 TIMING DIAGRAMS

Fig. 2: Synchronous Data Timing

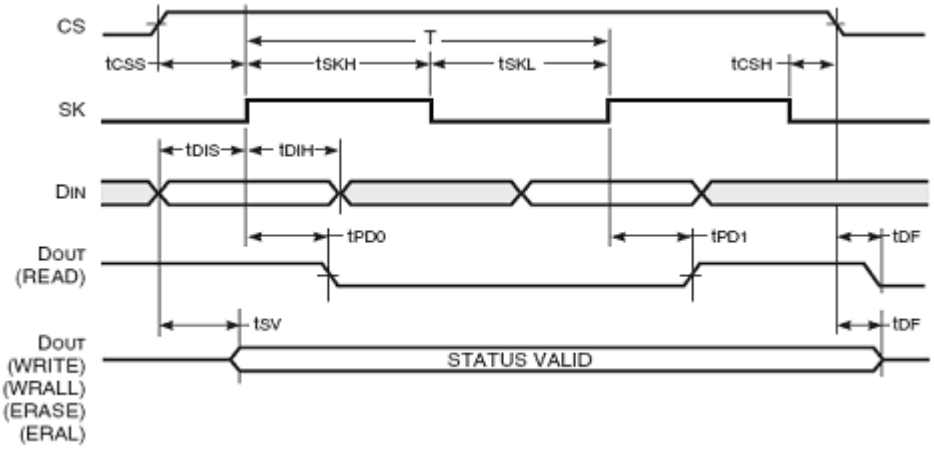


Fig. 3: Read Cycle Timing

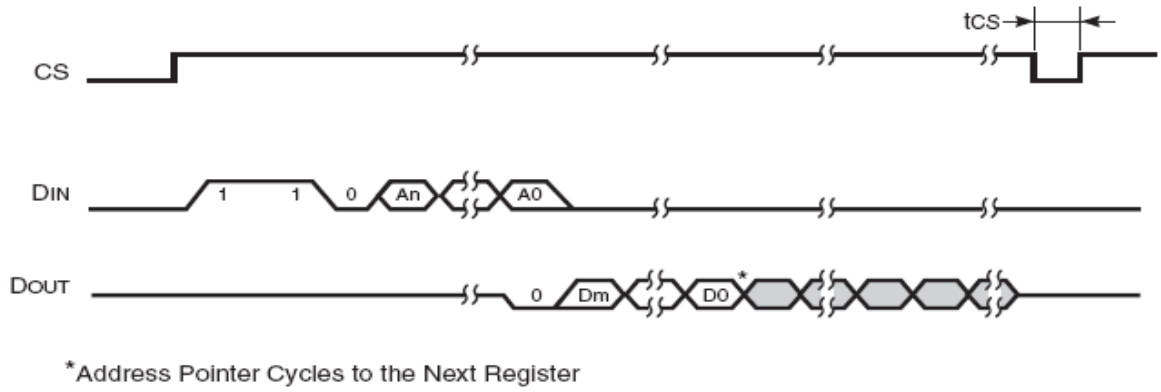


Fig. 4: Write Enable (WEN) Cycle Timing

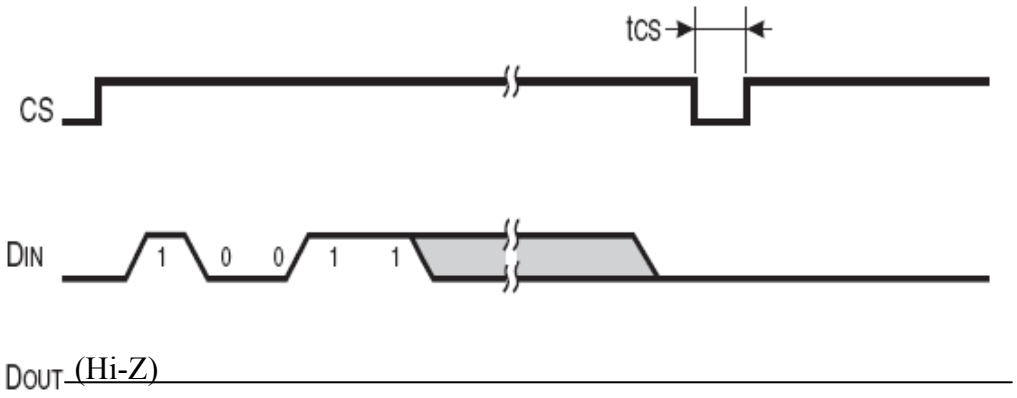
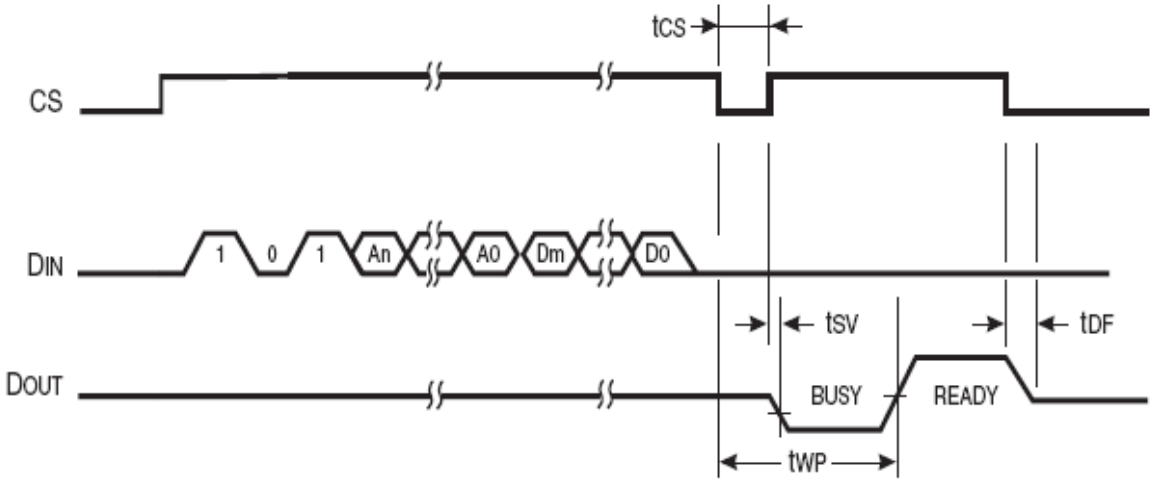
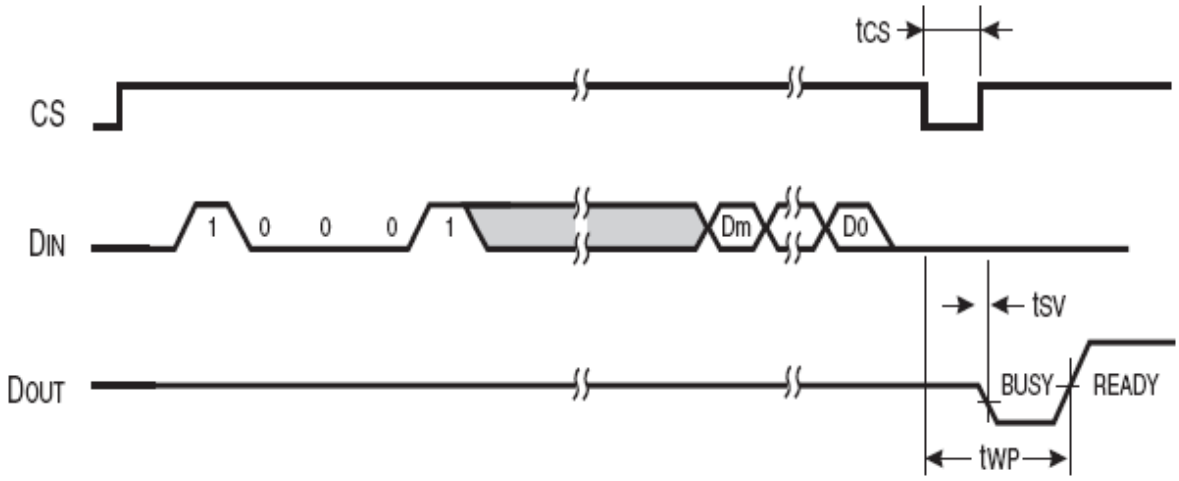


Fig. 5: Write (Write) Cycle Timing



Notes:
1. After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in **BUSY** status (DOUT indicates **BUSY** status) then attempting to perform another instruction could cause device malfunction.
2. To determine address bits An-A0 and data bits Dm-D0, see Instruction Set for the specific device.

Fig. 6: Write All (WRALL) Cycle Timing



Notes:
1. After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in **BUSY** status (DOUT indicates **BUSY** status) then attempting to perform another instruction could cause device malfunction.
2. To determine data bits Dm-D0, see Instruction Set for the appropriate device.

Fig. 7: Write Disable (WDS) Timing

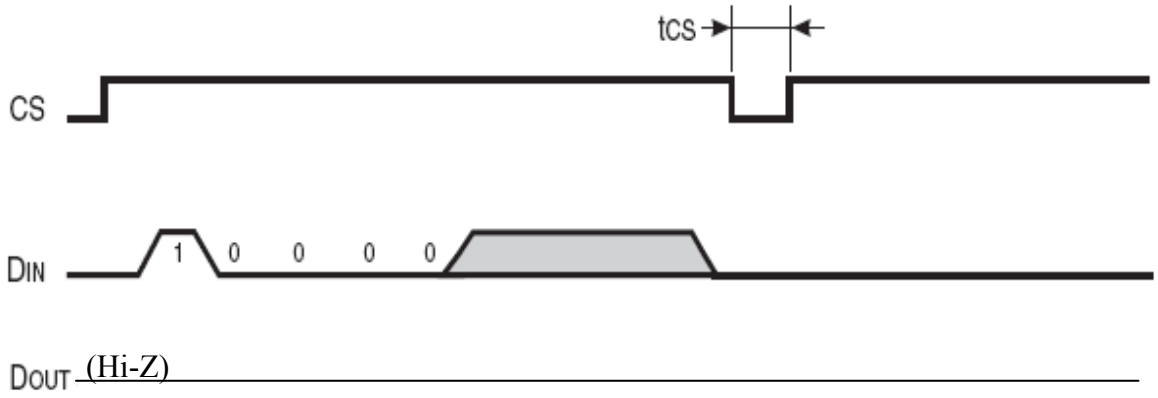


Fig. 8: Erase (Erase) Cycle Timing

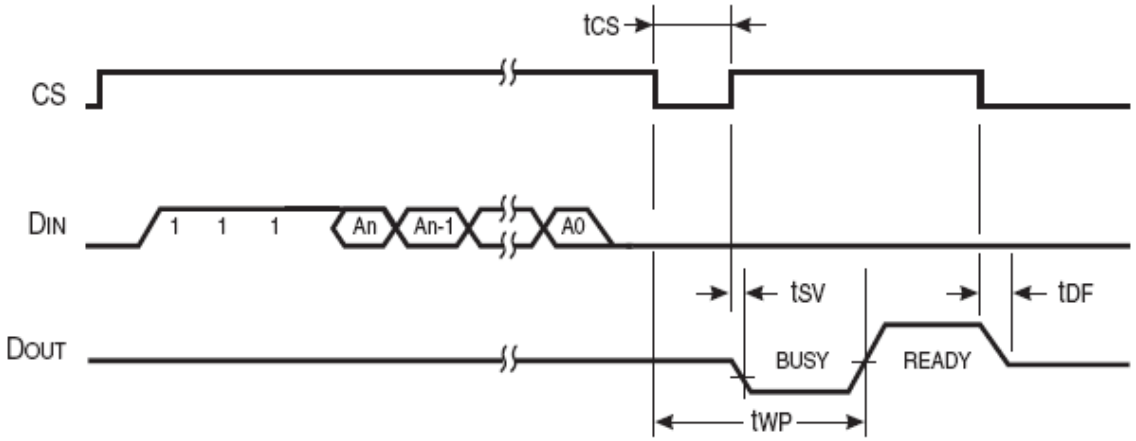
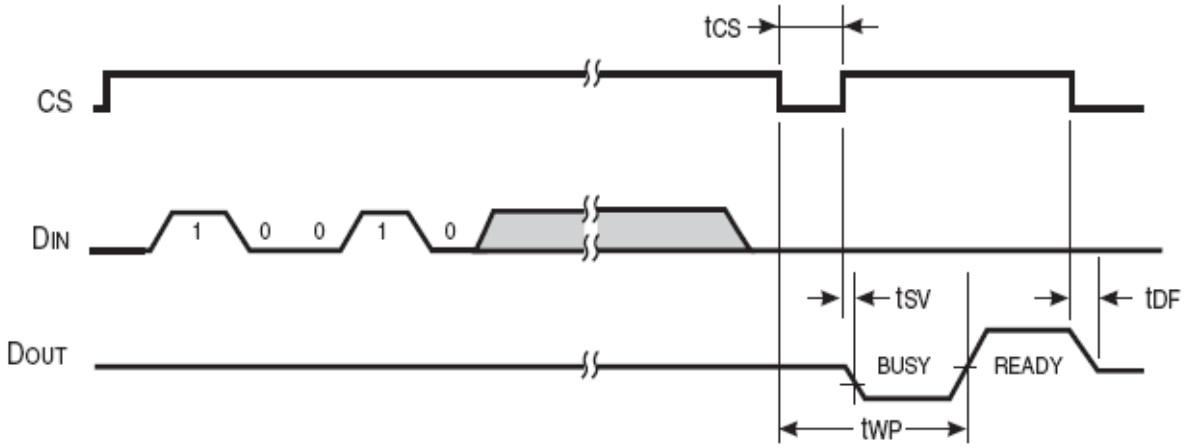


Fig. 9: Erase All (ERAL) Cycle Timing



Note for Figures 8 and 9:
1. After the completion of the instruction (DOUT is in READY status) then it may perform another instruction. If device is in **BUSY** status (DOUT indicates **BUSY** status) then attempting to perform another instruction could cause device malfunction.
2. To determine data bits An - A0, see Instruction Set for the appropriate device.

7 ABSOLUTE MAXIMUM RATINGS

Table 7.1. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +6.5	V
V_P	Voltage on Any Pin	-0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

[1] Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Table 7.2. Industrial Operation

V_{CC}	Ambient Temperature (T_A)	Grade
1.8V to 5.5V	-40°C to +85°C	Industrial (I)

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input /Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

8 DC ELECTRICAL CHARACTERISTICS

Table 8.1. DC Characteristics

T_A = –40°C to +85°C for Industrial

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OL1}	Output LOW Voltage	V_{CC} = 1.8V~5.5V, I_{OL} = 100 uA	—	0.2	V
V_{OL2}	Output LOW Voltage	V_{CC} = 2.5V~5.5V, I_{OL} = 2.1 mA	—	0.4	V
V_{OH1}	Output HIGH Voltage	V_{CC} = 1.8V~5.5V, I_{OH} = -0.1mA	VCC – 0.2	—	V
V_{OH2}	Output HIGH Voltage	V_{CC} = 2.5V~5.5V, I_{OH} = -0.4mA	2.4	—	V
V_{IH1}	Input HIGH Voltage	1.8V to 5.5V	0.7*V_{CC}	V_{CC} +1	V
V_{IH2}	Input HIGH Voltage	2.5V to 5.5V	2	V_{CC} +1	V
V_{IL1}	Input LOW Voltage	1.8V to 5.5V	-0.3	0.3*V_{CC}	V
V_{IL2}	Input LOW Voltage	2.5V to 5.5V	-0.3	0.8	V
I_{LI}	Input Leakage Current	VIN = 0V to VCC (CS, SK,DIN,ORG)	0	2.5	µA
I_{LO}	Output Leakage Current	VOUT = 0V to VCC, CS = 0V	0	2.5	µA

POWER SUPPLY CHARACTERISTICS

Table 8.2. Power Supply Characteristics

(**T_A** = –40°C to +85°C for Industrial)

Symbol	Parameter	Vcc	Test Conditions	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage			1.8		5.5	V
I_{SB1}	Standby current	1.8	CS = GND, SK = GND, ORG = Vcc or Floating (x16), DIN = Vcc or GND	—	0.1	1	µA
		2.5		—	0.3	1	µA
		5.5		—	0.5	1	µA
I_{SB2}	Standby current	1.8	CS = GND, SK = GND, ORG = GND (x8), DIN = Vcc or GND	—	0.4	1	µA
		2.5		—	6	10	µA
		5.5		—	10	15	µA
$I_{CC\text{-}Read}$	Read current	1.8	CS = V_{IH}, SK = 1 MHz	—		0.5	mA
		2.5	CS = V_{IH}, SK = 2 MHz	—		0.5	mA
		5.5	CS = V_{IH}, SK = 3 MHz	—		1	mA
$I_{CC\text{-}Write}$	Write current	1.8	CS = V_{IH}, SK = 1 MHz	—		1	mA
		2.5	CS = V_{IH}, SK = 2 MHz	—		1	mA
		5.5	CS = V_{IH}, SK = 3 MHz	—		2	mA

9 AC ELECTRICAL CHARACTERISTICS

AC Characteristics - Industrial

Table 9.1: AC Characteristics - Industrial

(T_A = –40°C to +85°C, Supply voltage = 1.8V to 5.5V)

Symbol	Parameter [1]	1.8V≤ Vcc < 2.5V		2.5V≤ Vcc < 4.5V		4.5V≤ Vcc < 5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCK}	SCK Clock Frequency	0	1	0	2	0	3	MHz
t_R	Input Rise Time	—	10	—	10	—	10	ns
t_F	Input Fall Time	—	10	—	10	—	10	ns
t_{SKH}	SK High Time	250	—	200	—	200	—	ns
t_{SKL}	SK Low Time	250	—	200	—	100	—	ns
t_{CS}	Minimum CS LOW Time	250	—	200	—	200	—	ns
t_{CSS}	CS Setup Time	200	—	100	—	50	—	ns
t_{CSH}	CS Hold Time	0	—	0	—	0	—	ns
t_{DIS}	D_{IN} Setup Time	100	—	50	—	50	—	ns
t_{DIH}	D_{IN} Hold Time	50	—	50	—	50	—	ns
t_{PD1}	Output Delay to “1”	—	400	—	200	—	100	ns
t_{PD0}	Output Delay to “0”	—	400	—	200	—	100	ns
t_{SV}	CS to Status Valid	—	400	—	200	—	200	ns
t_{DF}	CS to Dout in 3-state	—	200	—	100	—	100	ns
t_{WP}	Write Cycle Time	—	10	—	5	—	5	ms

Notes: 1. The parameters are characterized but not 100% tested.

2. AC measurement conditions:

C_L = 100 pF

Input pulse voltages: per V_{IL} and V_{IH} spec

Input rise and fall times: ≤ 10 ns

Timing reference voltages: half V_{CC} level

10 ORDERING INFORMATION

Industrial Grade: 1.8V to 5.5V, -40°C to +85°C, Lead-free

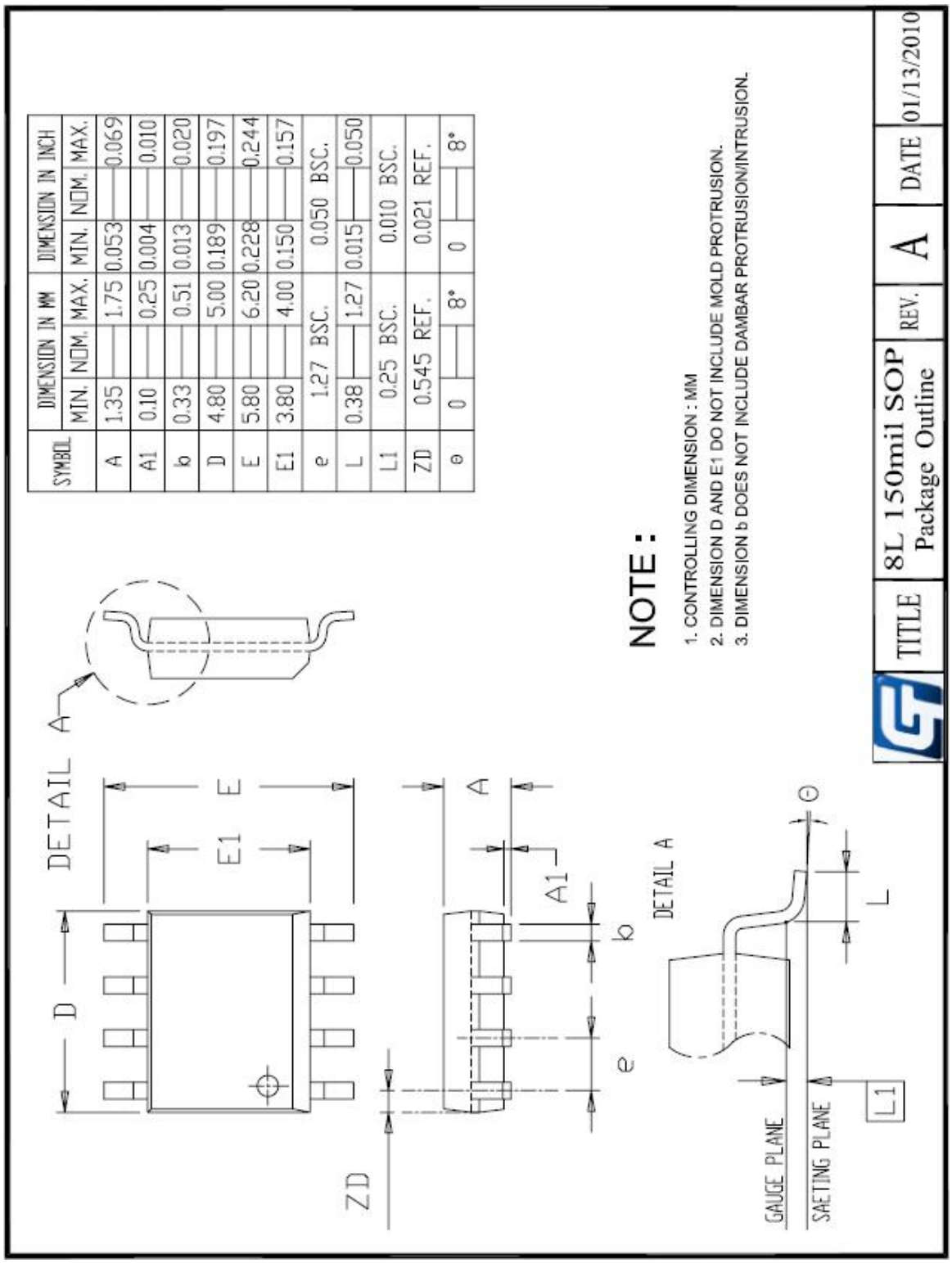
Product	Voltage Range	Part Number*	Package (8-pin)*
GT93C66A	1.8V to 5.5V	GT93C66A-2GLI-TR	150-mil SOIC/SOP JEDEC
		GT93C66A-2ZLI-TR	3 x 4.4 mm TSSOP
		GT93C66A-2UDLI-TR	2 x 3 x0.55 mm UDFN

*

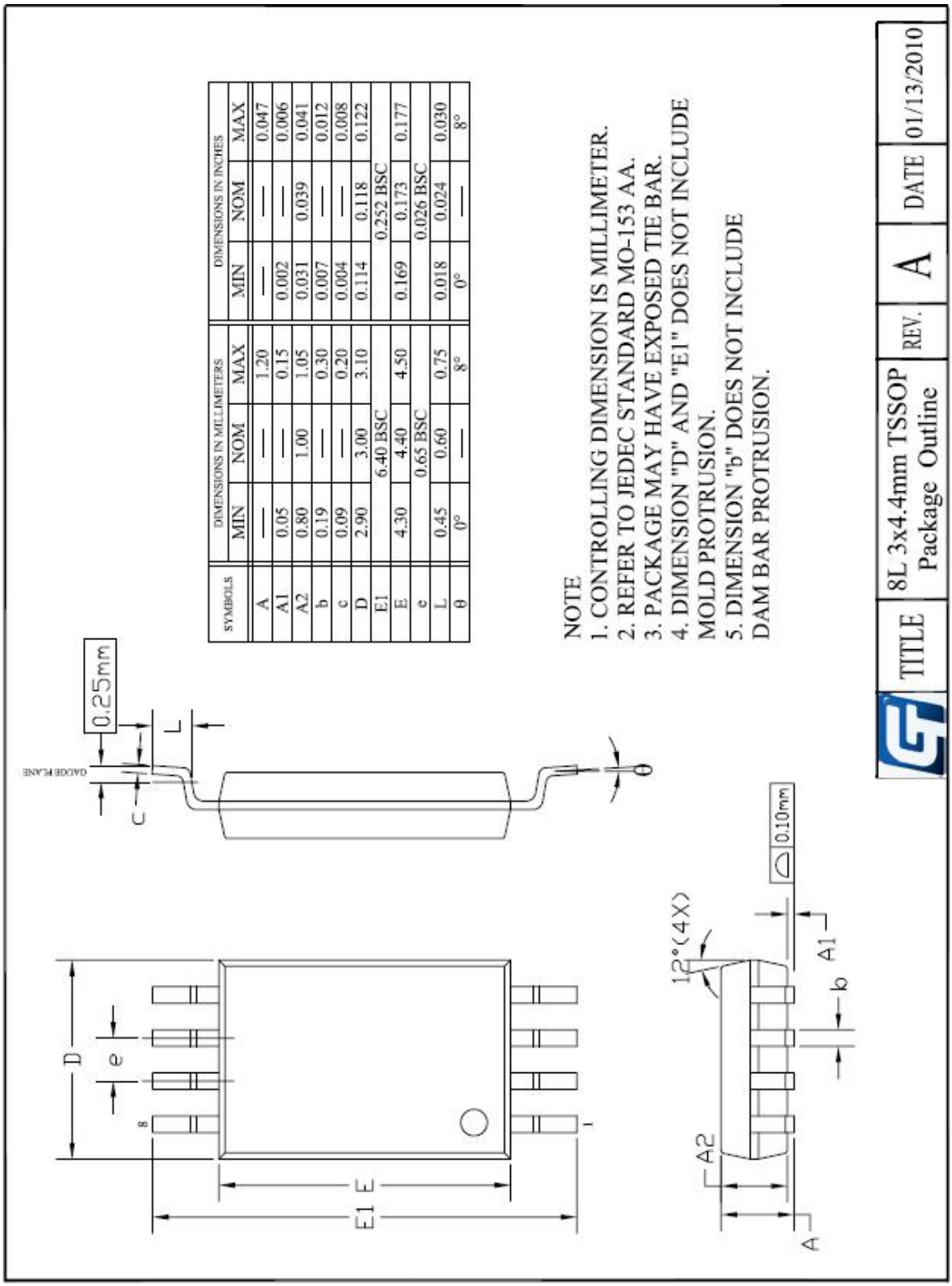
1. Contact Giantec Sales Representatives for availability and other package information.
2. The listed part numbers are packed in tape and reel "-TR" (4K per reel). UDFN is 5K per reel.
3. For tube/bulk packaging, remove "-TR" at the end of the P/N.
4. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free, or Green, whichever is applicable.
5. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

11 PACKAGE INFORMATION

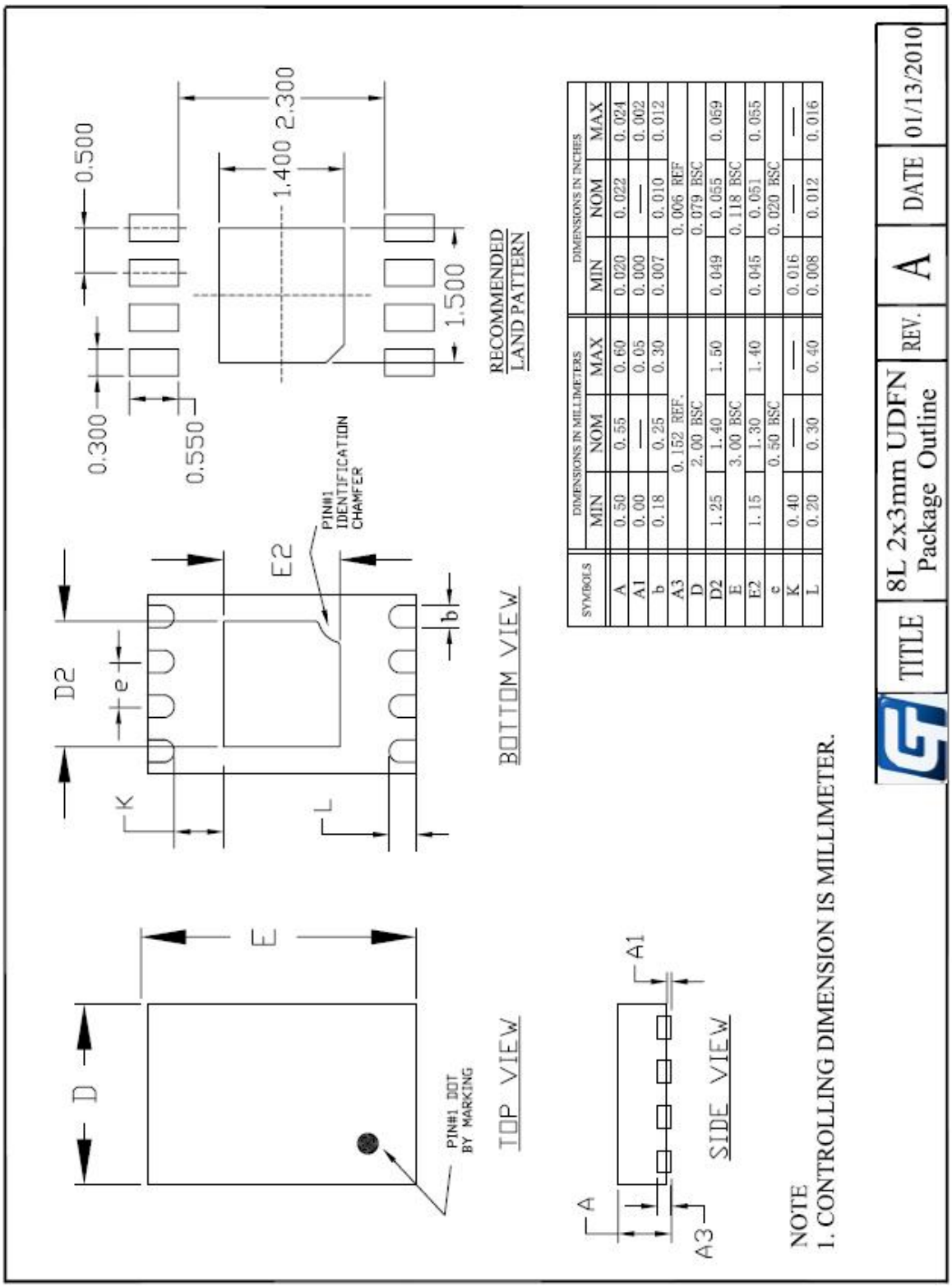
SOIC/SOP (JEDEC)



TSSOP



UDFN: Ultra-thin DFN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	—	0.05	0.000	—	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A3		0.152 REF.			0.006 REF	
D		2.00 BSC			0.079 BSC	
D2	1.25	1.40	1.50	0.049	0.055	0.059
E		3.00 BSC			0.118 BSC	
E2	1.15	1.30	1.40	0.045	0.051	0.055
e		0.50 BSC			0.020 BSC	
K	0.40	—	—	0.016	—	—
L	0.20	0.30	0.40	0.008	0.012	0.016

12 REVISION HISTORY

Revision	Date	Page	Descriptions
a0	3/23/2010	All	Initial version