Symbol	Parameter	Test Conditions		Min	Тур	Max	Units
Off Cha	aracteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		800			V
ΔBV_{DSS} / ΔT_{J}	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced t	to 25°C		0.9		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V				10	μΑ
		V _{DS} = 640 V, T _C = 125°C				100	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
On Cha	racteristics						
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10 V, I _D =1.65 A			1.5	1.95	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 50 V, I _D = 1.65 A	(Note 4)		4.3		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$			1150 125 14	1500 160 18	pF pF pF
Switchi	ing Characteristics						
t _{d(on)}	Turn-On Delay Time				30	70	ns
t _r	Turn-On Rise Time	$V_{DD} = 400 \text{ V}, I_D = 5.8 \text{ A},$		70	150	ns	
t _{d(off)}	Turn-Off Delay Time	R_G = 25 Ω (Note 4, 5)			65	140	ns
t _f	Turn-Off Fall Time				45	100	ns
Q _g	Total Gate Charge	V _{DS} = 640 V, I _D = 5.8 A,			31		nC
Q _{gs}	Gate-Source Charge	$V_{GS} = 0.0 \text{ V}, I_D = 0.0 \text{ A},$			7.1		nC
Q _{qd}	Gate-Drain Charge	(Note 4, 5)			15		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings					
I _S	Maximum Continuous Drain-Source Diode Forward Current					3.3	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current					13.2	Α
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 3.3 \text{ A}$				1.4	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{S} = 5.8 \text{ A},$			650		ns
Q _{rr}	Reverse Recovery Charge	$dI_F / dt = 100 A/\mu s$ (Note 4)			5.7		μC

©2000 Fairchild Semiconductor International Rev. A, September 2000

^{1.} Repetitive Rating : Pulse width limited by maximum junction temper 2. L = 117mH, $I_{AS} = 3.3A$, $V_{DD} = 50V$, $R_G = 25~\Omega$, Starting $T_J = 25^{\circ}C$ 3. $I_{SD} \le 5.8A$, di/dt $\le 2004/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25^{\circ}C$ 4. Pulse Test : Pulse width $\le 300\mu s$, Duty cycle $\le 2\%$ 5. Essentially independent of operating temperature

Typical Characteristics

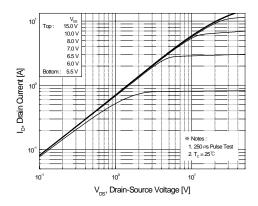


Figure 1. On-Region Characteristics

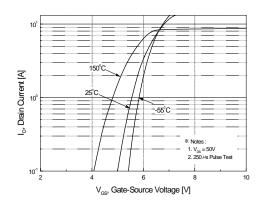


Figure 2. Transfer Characteristics

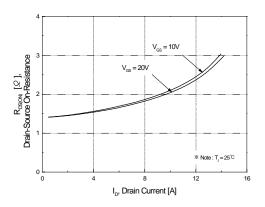


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

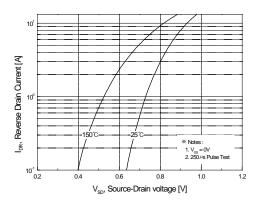


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

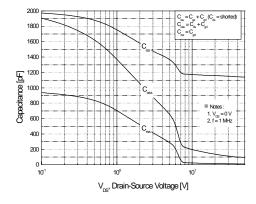


Figure 5. Capacitance Characteristics

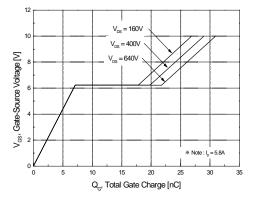
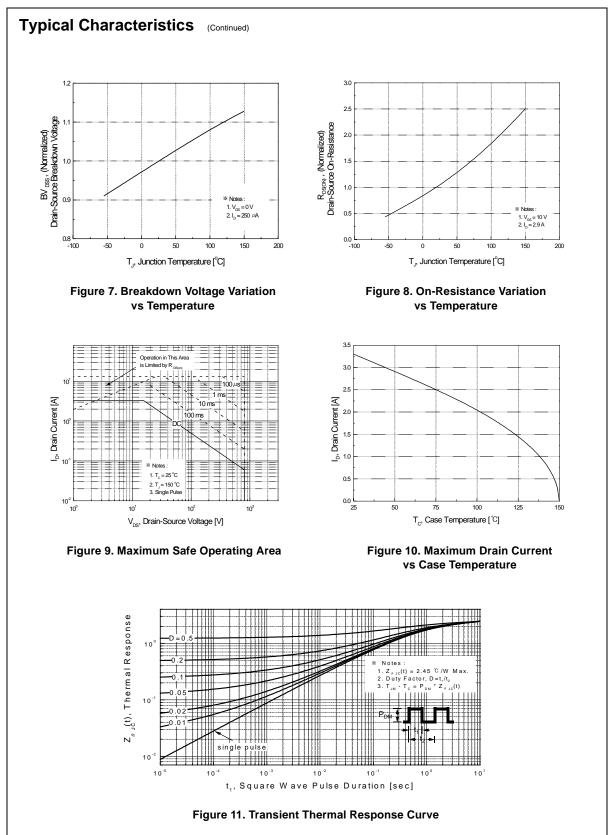
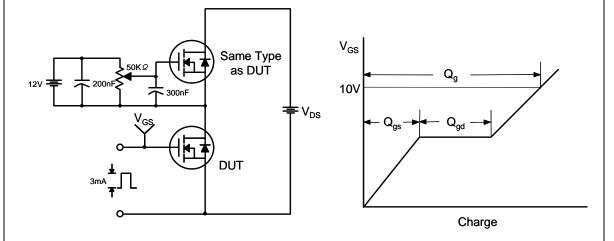


Figure 6. Gate Charge Characteristics

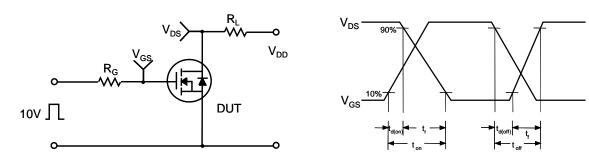


©2000 Fairchild Semiconductor International Rev. A, September 2000

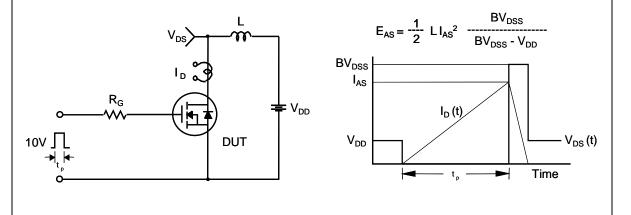
Gate Charge Test Circuit & Waveform



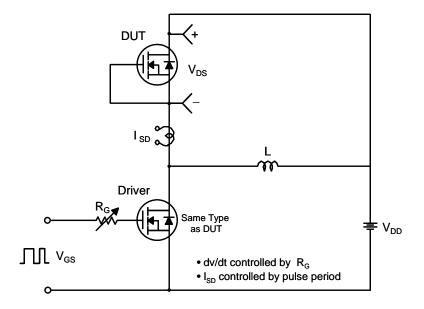
Resistive Switching Test Circuit & Waveforms

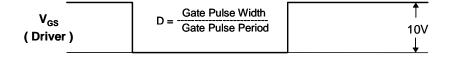


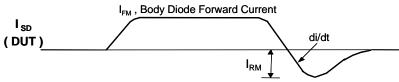
Unclamped Inductive Switching Test Circuit & Waveforms



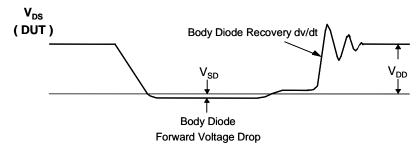
Peak Diode Recovery dv/dt Test Circuit & Waveforms



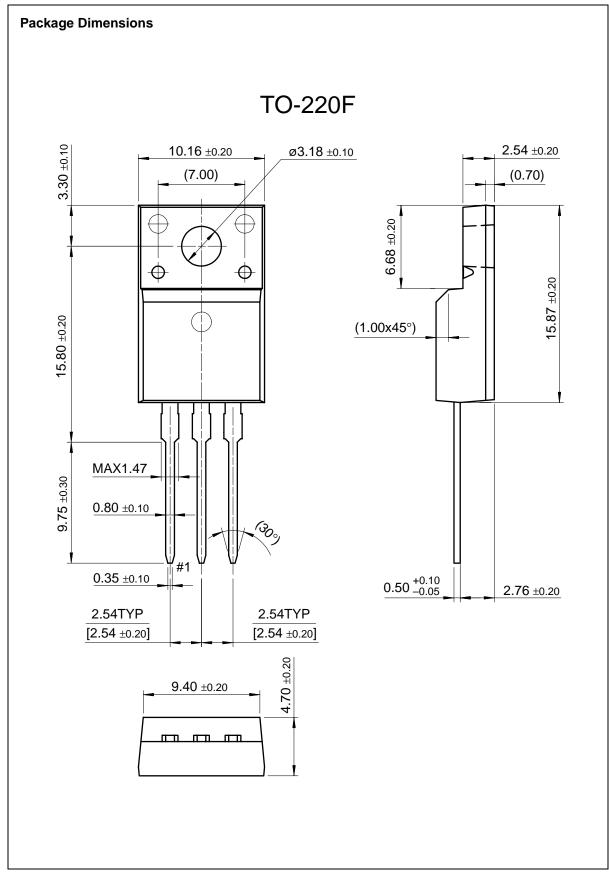




Body Diode Reverse Current



©2000 Fairchild Semiconductor International



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEXTM FASTrTM QFETTM VCXTM

Bottomless[™] GlobalOptoisolator[™] QS[™]

CoolFET™ GTO™ QT Optoelectronics™

CROSSVOLT™ HiSeC™ Quiet Series™ DOME™ ISOPLANAR™ SuperSOT™-3 E²CMOS™ MICROWIRE™ SuperSOT™-6 EnSigna™ OPTOLOGIC™ SuperSOT™-8 FACT™ OPTOPLANAR™ SyncFET™ РОР™ FACT Quiet Series™ TinyLogic™

FAST® PowerTrench® UHC™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR INTERNATIONAL.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

©2000 Fairchild Semiconductor International Rev. F