



ON Semiconductor®

## FDC642P

### Single P-Channel 2.5V Specified PowerTrench® MOSFET -20 V, -4.0 A, 65 mΩ

#### Features

- Max  $r_{DS(on)}$  = 65 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -4.0$  A
- Max  $r_{DS(on)}$  = 100 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -3.2$  A
- Fast switching speed
- Low gate charge (11nC typical)
- High performance trench technology for extremely low  $r_{DS(on)}$
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1 mm thick)
- Termination is Lead-free and RoHS Compliant



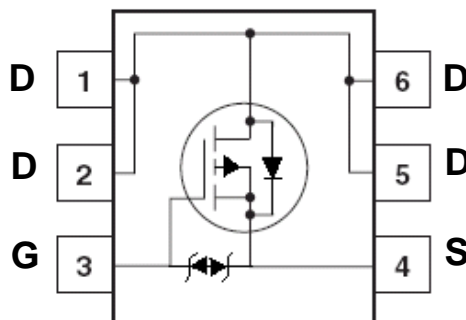
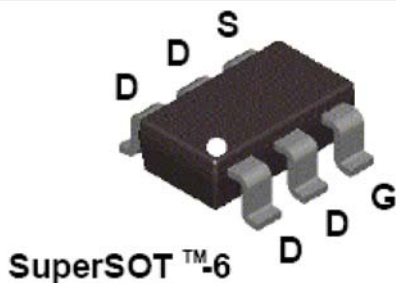
#### General Description

This P-Channel 2.5V specified MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the larger packages are impractical.

#### Applications

- Load switch
- Battery protection
- Power management



#### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	-4.0	A
	-Pulsed	-20	
$P_D$	Power Dissipation (Note 1a)	1.6	W
	Power Dissipation (Note 1b)	0.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to + 150	$^\circ\text{C}$

#### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	$^\circ\text{C/W}$
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#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.642	FDC642P	SSOT-6™	7"	8 mm	3000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-13		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\ \text{V}$ , $V_{GS} = 0\ \text{V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\ \text{V}$ , $V_{DS} = 0\ \text{V}$			$\pm 10$	$\mu\text{A}$

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\ \mu\text{A}$	-0.4	-0.6	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		2.5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\ \text{V}$ , $I_D = -4.0\ \text{A}$		45	65	m $\Omega$
		$V_{GS} = -2.5\ \text{V}$ , $I_D = -3.2\ \text{A}$		55	100	
		$V_{GS} = -4.5\ \text{V}$ , $I_D = -4.0\ \text{A}$ , $T_J = 125^\circ\text{C}$		62	90	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\ \text{V}$ , $I_D = -4.0\ \text{A}$		15		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -10\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$		700	925	pF
$C_{oss}$	Output Capacitance			110	150	pF
$C_{rss}$	Reverse Transfer Capacitance			95	145	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\ \text{V}$ , $I_D = -1\ \text{A}$ , $V_{GS} = -4.5\ \text{V}$ , $R_{GEN} = 6\ \Omega$		6	12	ns
$t_r$	Rise Time			7	14	ns
$t_{d(off)}$	Turn-Off Delay Time			120	190	ns
$t_f$	Fall Time			52	83	ns
$Q_g$	Total Gate Charge	$V_{DD} = -10\ \text{V}$ , $I_D = -4\ \text{A}$ , $V_{GS} = -4.5\ \text{V}$		11	16	nC
$Q_{gs}$	Gate to Source Charge			1.1		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3.0		nC

**Drain-Source Diode Characteristics**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$ , $I_S = -1.3\ \text{A}$ (Note 2)		-0.7	-1.2	V

**Notes:**

1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

- a.  $78^\circ\text{C/W}$  when mounted on a  $1\ \text{in}^2$  pad of 2 oz copper.
- b.  $156^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2: Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%.

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

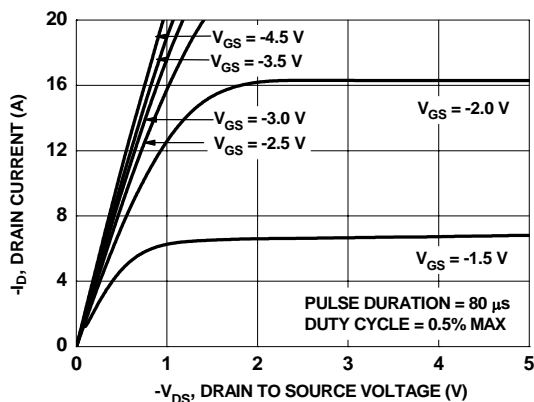


Figure 1. On Region Characteristics

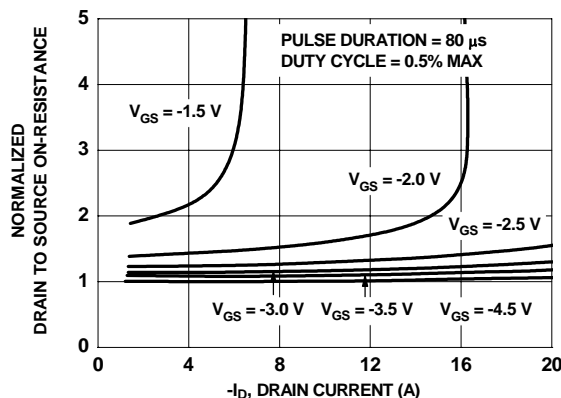


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

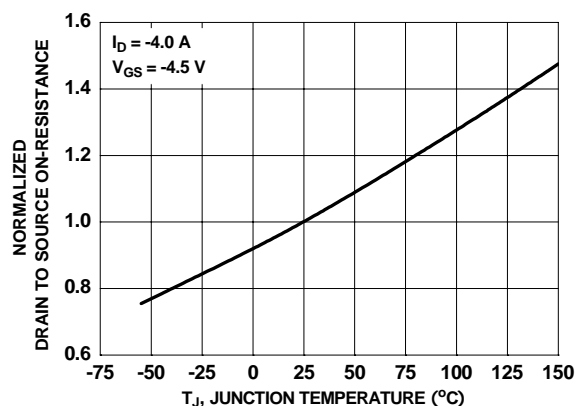


Figure 3. Normalized On Resistance vs Junction Temperature

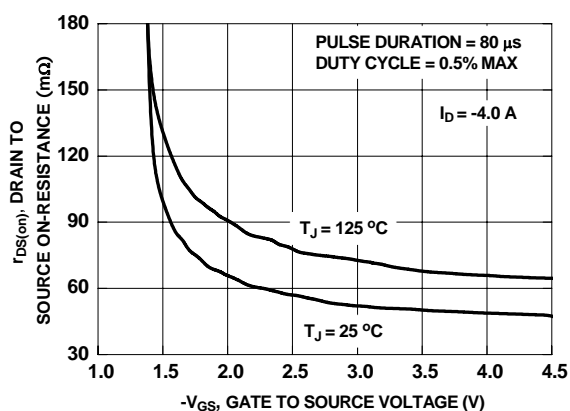


Figure 4. On-Resistance vs Gate to Source Voltage

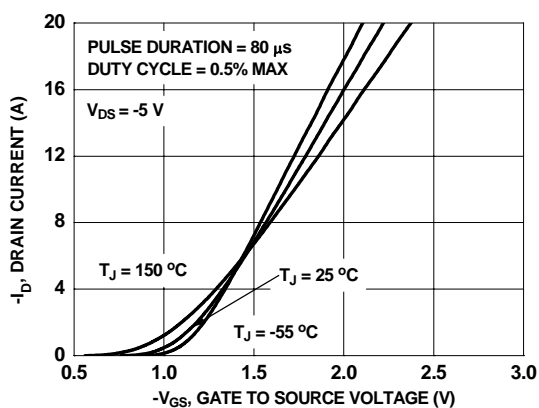


Figure 5. Transfer Characteristics

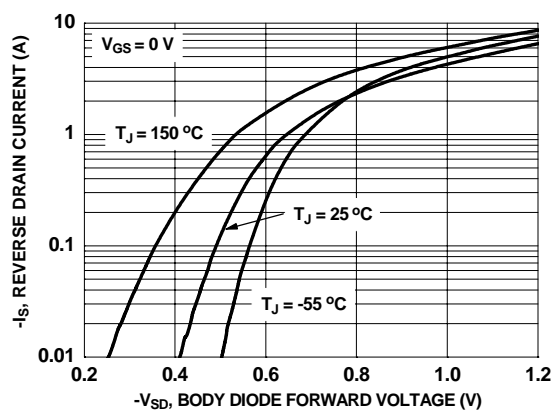


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

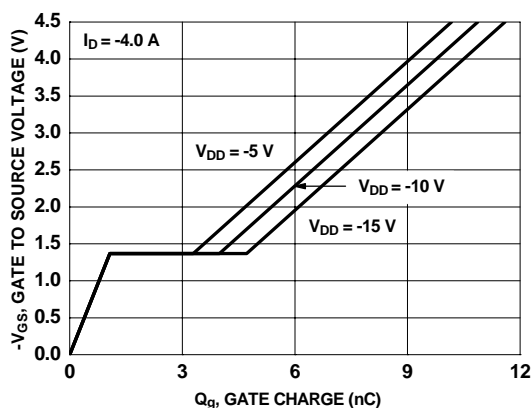


Figure 7. Gate Charge Characteristics

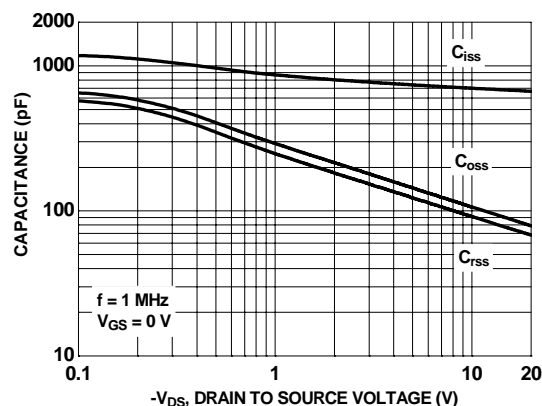


Figure 8. Capacitance vs Drain to Source Voltage

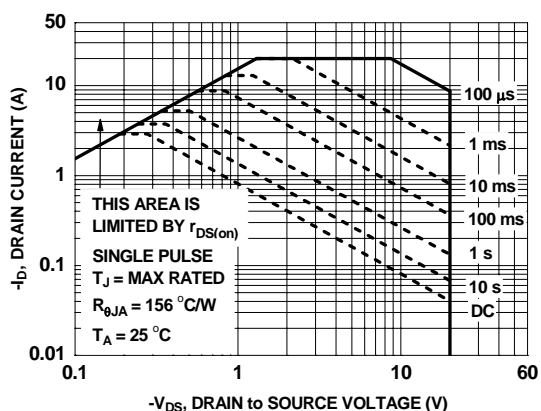


Figure 9. Forward Bias Safe Operating Area

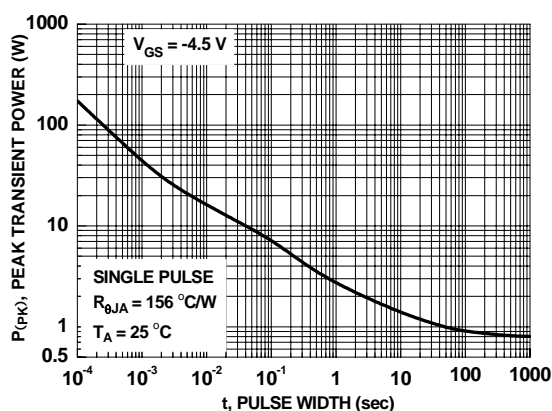


Figure 10. Single Pulse Maximum Power Dissipation

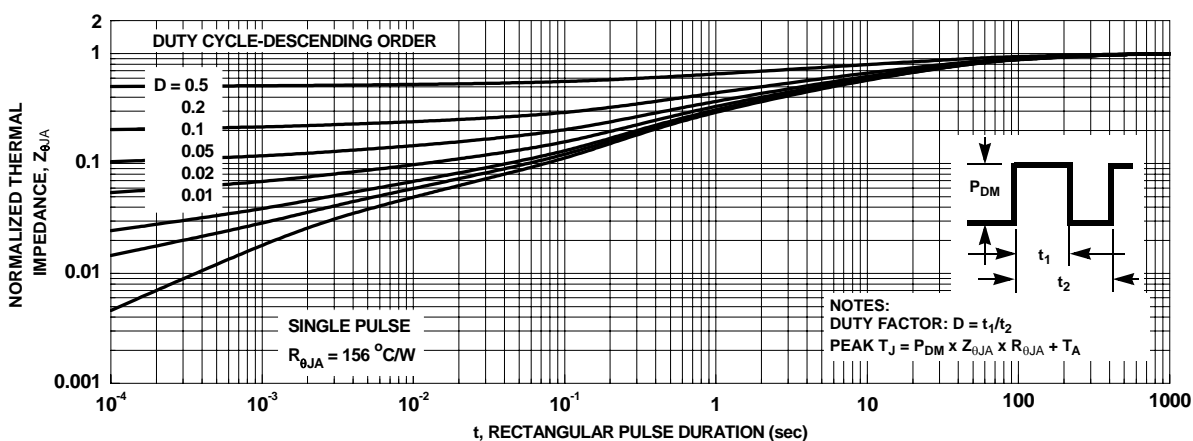



Figure 11. Junction-to-Ambient Transient Thermal Response Curve

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