

## Ordering Information (Note 4)

Part Number	Package	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DGD0506AFN-7	W-DFN3030-10	DGD0506A	7	8	3,000
DGD0506AM10-13	MSOP10	DGD0506A	13	12	2,500

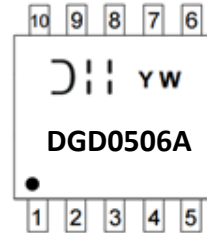
Note: 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information



W-DFN3030-10

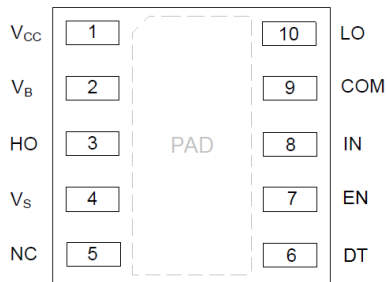
DGD0506A = Product Type Marking Code  
 YY = Year (ex: 19 = 2019)  
 WW = Week (01 to 53)



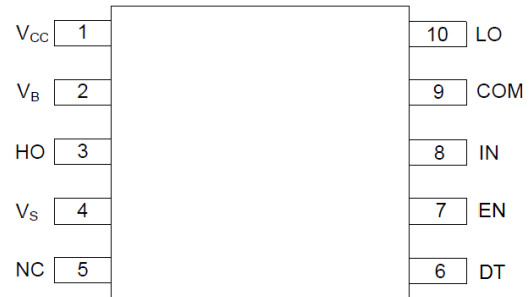
MSOP-10

DII = Manufacturer's Marking  
 DGD0506A = Product Type Marking Code  
 Y = Year: (0 to 9)  
 W = Week: (A – Z : 1 – 26 week)  
 (a – z : 27 – 52 week)

## Pin Diagrams



Top View: W-DFN3030-10

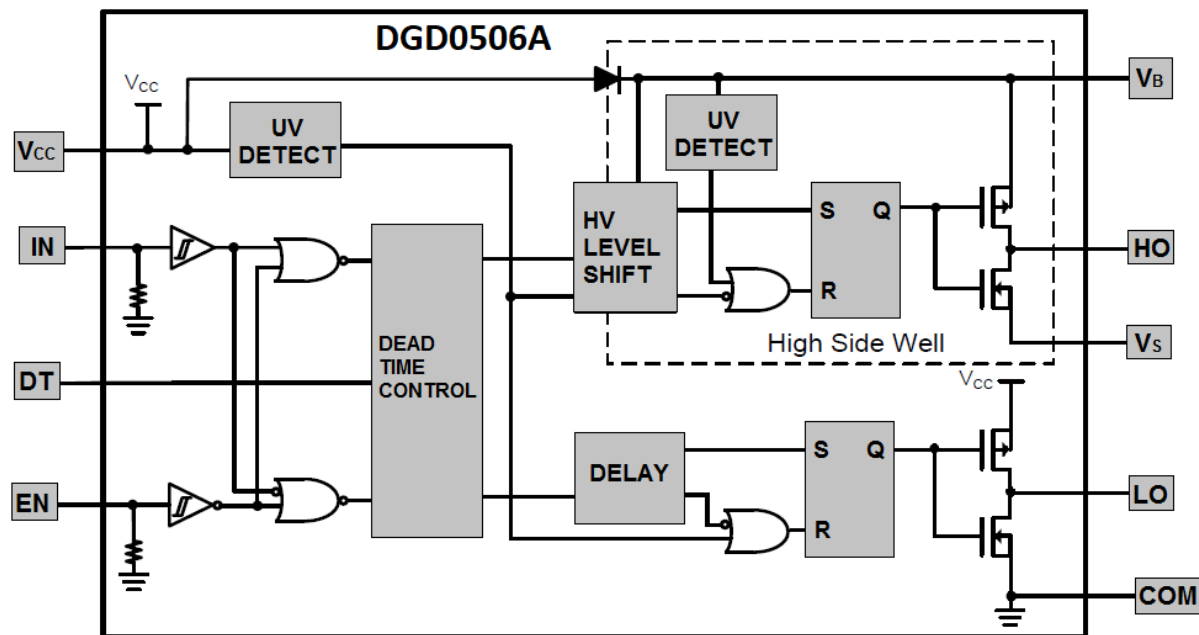


Top View: MSOP-10

## Pin Descriptions

Pin Number	Pin Name	Function
1	V <sub>CC</sub>	Low-Side and Logic Supply
2	V <sub>B</sub>	High-Side Floating Supply
3	H <sub>O</sub>	High-Side Gate Drive Output
4	V <sub>S</sub>	High-Side Floating Supply Return
5	NC	No Connect (No Internal Connection)
6	DT	Deadtime Control
7	EN	Logic Input Enable, a Logic Low turns off Gate Driver
8	IN	Logic Input for High-Side and Low-Side Gate Driver Outputs (H <sub>O</sub> and L <sub>O</sub> ), in Phase with H <sub>O</sub>
9	COM	Low-Side and Logic Return
10	L <sub>O</sub>	Low-Side Gate Drive Output
PAD	Substrate	Connect to COM on PCB

## Functional Block Diagram



## Absolute Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Positive Supply Voltage	V <sub>B</sub>	-0.3 to +60	V
High-Side Floating Negative Supply Voltage	V <sub>S</sub>	V <sub>B</sub> -14 to V <sub>B</sub> +0.3	V
High-Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub> -0.3 to V <sub>B</sub> +0.3	V
Offset Supply Voltage Transient	dV <sub>S</sub> /dt	50	V/ns
Logic and Low-Side Fixed Supply Voltage	V <sub>CC</sub>	-0.3 to +14	V
Low-Side Output Voltage	V <sub>LO</sub>	-0.3 to V <sub>CC</sub> +0.3	V
Logic Input Voltage (IN and EN)	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> +0.3	V

## Thermal Characteristics – W-DFN3030-10 (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	P <sub>D</sub>	0.4	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	64	°C/W
Thermal Resistance, Junction to Case (Note 5)	R <sub>θJC</sub>	42	°C/W
Operating Temperature	T <sub>J</sub>	+150	°C
Lead Temperature (Soldering, 10s)	T <sub>L</sub>	+300	
Storage Temperature Range	T <sub>STG</sub>	-55 to +150	

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

## Thermal Characteristics – MSOP-10 (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 6)	P <sub>D</sub>	0.75	W
Thermal Resistance, Junction to Ambient (Note 6)	R <sub>θJA</sub>	166	°C/W
Thermal Resistance, Junction to Case (Note 6)	R <sub>θJC</sub>	32	°C/W
Operating Temperature	T <sub>J</sub>	+150	°C
Lead Temperature (Soldering, 10s)	T <sub>L</sub>	+300	
Storage Temperature Range	T <sub>STG</sub>	-55 to +150	

Note: 6. When mounted on a standard JEDEC 2-layer FR-4 board with minimum recommended pad layout.

## Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply	V <sub>B</sub>	V <sub>S</sub> + 8	V <sub>S</sub> + 14	V
High-Side Floating Supply Offset Voltage	V <sub>S</sub>	(Note 7)	50 (Note 8)	V
High-Side Floating Output Voltage	V <sub>HO</sub>	V <sub>S</sub>	V <sub>B</sub>	V
Logic and Low Side Fixed Supply Voltage	V <sub>CC</sub>	8	14	V
Low-Side Output Voltage	V <sub>LO</sub>	0	V <sub>CC</sub>	V
Logic Input Voltage (IN and EN)	V <sub>IN</sub>	0	5	V
Ambient Temperature	T <sub>A</sub>	-40	+125	°C

Notes: 7. Logic operation for V<sub>S</sub> of -5V to +50V.

8. Provided V<sub>B</sub> doesn't exceed absolute maximum rating of 60V.

**DC Electrical Characteristics** ( $V_{CC} = V_{BS} = 12V$ ,  $COM = V_S = 0V$ , @  $T_A = +25^\circ C$ , unless otherwise specified.) (Note 9)

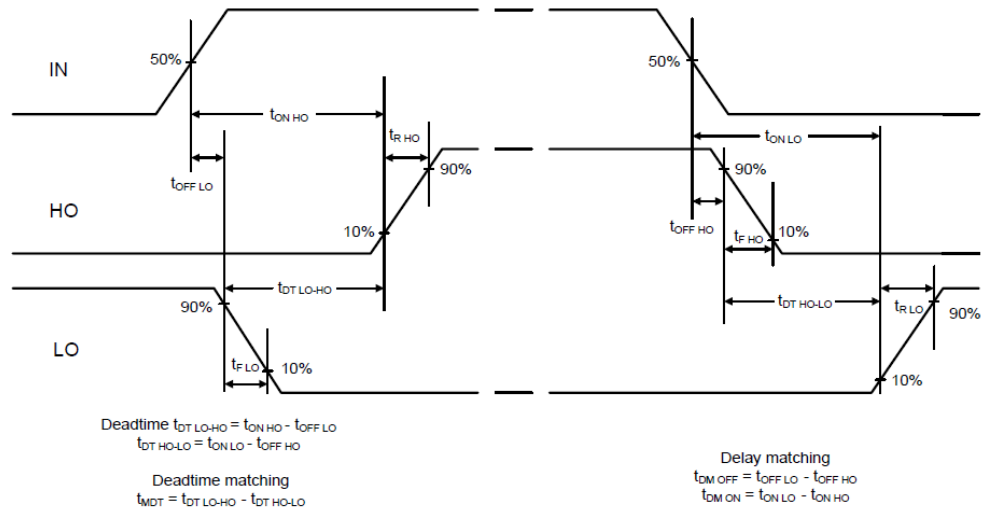
Parameter	Symbol	Min	Typ	Max	Unit	Condition
Logic "1" Input Voltage	$V_{IH}$	2.4	—	—	V	—
Logic "0" Input Voltage	$V_{IL}$	—	—	0.8	V	—
Enable Logic "1" Input Voltage	$V_{ENIH}$	1.5	—	—	V	—
Enable Logic "0" Input Voltage	$V_{ENIL}$	—	—	0.7	V	—
Input Voltage Hysteresis	$V_{INHYS}$	—	0.6	—	V	—
High Level Output Voltage, $V_{BIAS} - V_O$	$V_{OH}$	—	0.45	0.6	V	$I_{O+} = 100mA$
Low Level Output Voltage, $V_O$	$V_{OL}$	—	0.15	0.22	V	$I_{O-} = 100mA$
Offset Supply Leakage Current	$I_{LK}$	—	10	50	$\mu A$	$V_B = V_S = 60V$
$V_{CC}$ Shutdown Supply Current	$I_{CCSD}$	—	0	1	$\mu A$	$V_{IN} = 0V$ or $5V$ , $V_{EN} = 0V$
$V_{CC}$ Quiescent Supply Current	$I_{CCQ}$	—	0.28	0.5	mA	$V_{IN} = 0V$ or $5V$ , $R_{DT} = 100k\Omega$
$V_{CC}$ Operating Supply Current	$I_{CCOP}$	—	7.6	—	mA	$f_s = 500kHz$ , $C_L = 1000pF$
$V_{BS}$ Quiescent Supply Current	$I_{BSQ}$	—	32	100	$\mu A$	$V_{IN} = 0V$ or $5V$
$V_{BS}$ Operating Supply Current	$I_{BSOP}$	—	7.6	—	mA	$f_s = 500kHz$ , $C_L = 1000pF$
Logic "1" Input Bias Current	$I_{IN+}$	—	25	60	$\mu A$	$V_{IN} = 5V$
Logic "0" Input Bias Current	$I_{IN-}$	—	0	1	$\mu A$	$V_{IN} = 0V$
$V_{BS}$ Supply Undervoltage Positive Going Threshold	$V_{BSUV+}$	6.0	7.0	8.0	V	—
$V_{BS}$ Supply Undervoltage Negative Going Threshold	$V_{BSUV-}$	5.6	6.6	7.6	V	—
$V_{CC}$ Supply Undervoltage Positive Going Threshold	$V_{CCUV+}$	6.0	7.0	8.0	V	—
$V_{CC}$ Supply Undervoltage Negative Going Threshold	$V_{CCUV-}$	5.6	6.6	7.6	V	—
Output High Short-Circuit Pulsed Current	$I_{O+}$	0.9	1.5	—	A	$V_O = 0V$ , $PW \leq 10\mu s$
Output Low Short-Circuit Pulsed Current	$I_{O-}$	1.5	2.0	—	A	$V_O = 15V$ , $PW \leq 10\mu s$
Forward Voltage of Bootstrap Diode	$V_{F1}$	—	0.67	—	V	$I_F = 100\mu A$
Forward Voltage of Bootstrap Diode	$V_{F2}$	—	1.7	—	V	$I_F = 100mA$

Note: 9. The  $V_{IN}$  and  $I_{IN}$  parameters are applicable to the two logic pins: IN and EN. The  $V_O$  and  $I_O$  parameters are applicable to the respective output pins: HO and LO.

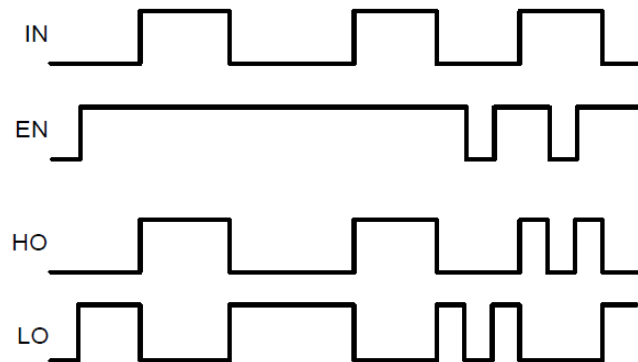
**AC Electrical Characteristics** ( $V_{CC} = V_{BS} = 12V$ ,  $COM = V_S = 0V$ ,  $C_L = 1000pF$ , @  $T_A = +25^\circ C$ , unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Turn-On Propagation Delay, HO & LO	$t_{ON}$	65	96	125	ns	$R_{DT} = 10k\Omega$
		350	463	580	ns	$R_{DT} = 100k\Omega$
Turn-Off Propagation Delay, HO & LO	$t_{OFF}$	—	22	56	ns	—
Turn-On Rise Time	$t_R$	—	17	35	ns	—
Turn-Off Fall Time	$t_F$	—	12	25	ns	—
Delay Matching	$t_{DM}$	—	—	50	ns	—
Deadtime: $t_{DT LO-HO}$ & $t_{DT HO-LO}$	$t_{DT}$	40	70	100	ns	$R_{DT} = 10k\Omega$
		300	430	560	ns	$R_{DT} = 100k\Omega$
Deadtime Matching	$t_{MDT}$	—	—	50	ns	$R_{DT} = 100k\Omega$

## Timing Waveforms



**Figure 1.** Switching Time Waveform Definitions



**Figure 2.** Input / Output Timing Diagram

**Typical Performance Characteristics** ( $V_{CC} = 12V$ , @  $T_A = +25^\circ C$ , unless otherwise specified.)

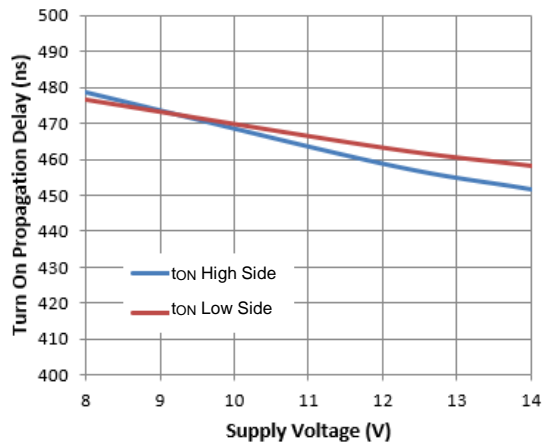


Figure 3. Turn-on Propagation Delay vs. Supply Voltage

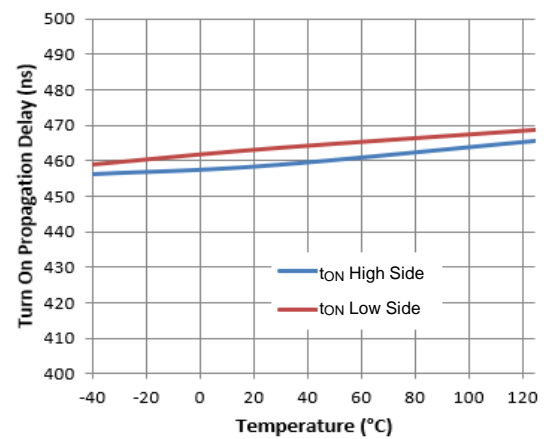


Figure 4. Turn-on Propagation Delay vs. Temperature

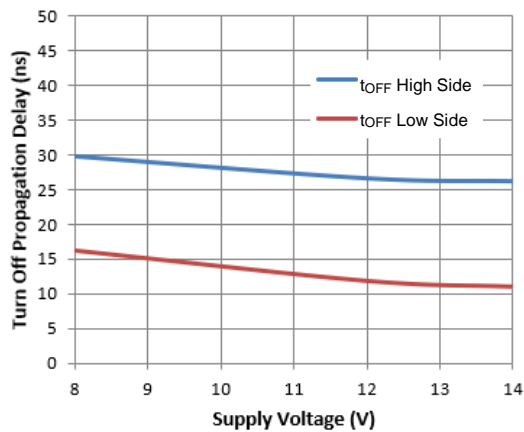


Figure 5. Turn-off Propagation Delay vs. Supply Voltage

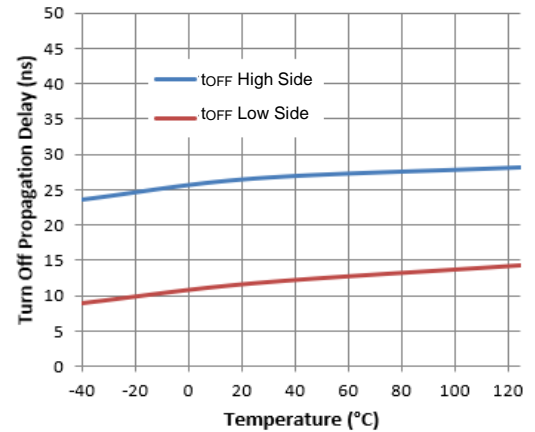


Figure 6. Turn-off Propagation Delay vs. Temperature

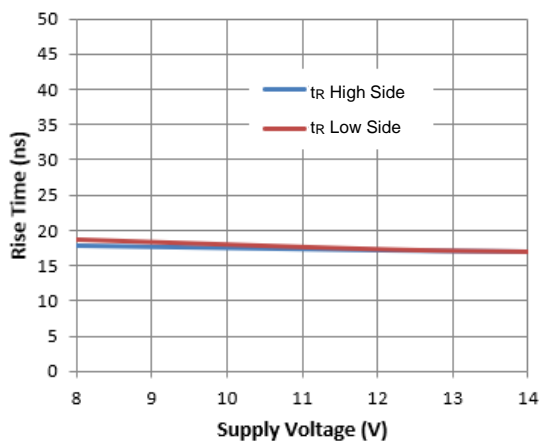


Figure 7. Rise Time vs. Supply Voltage

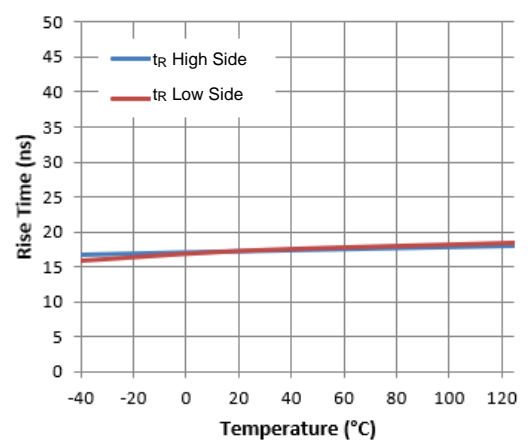


Figure 8. Rise Time vs. Temperature

# Typical Performance Characteristics (continued)

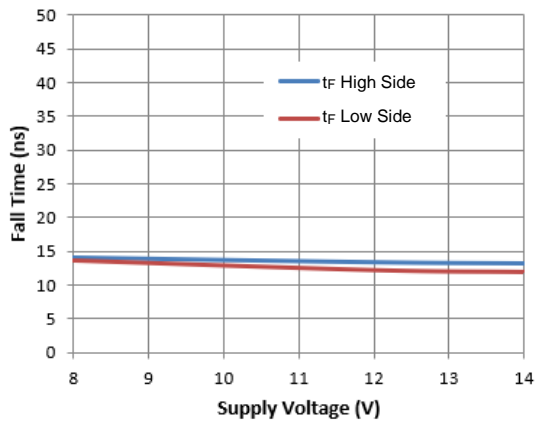


Figure 9. Fall Time vs. Supply Voltage

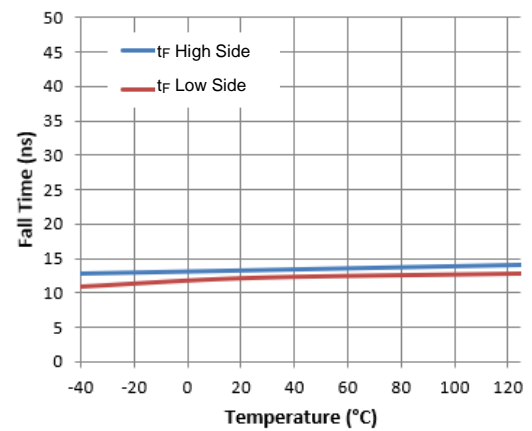


Figure 10. Fall Time vs. Temperature

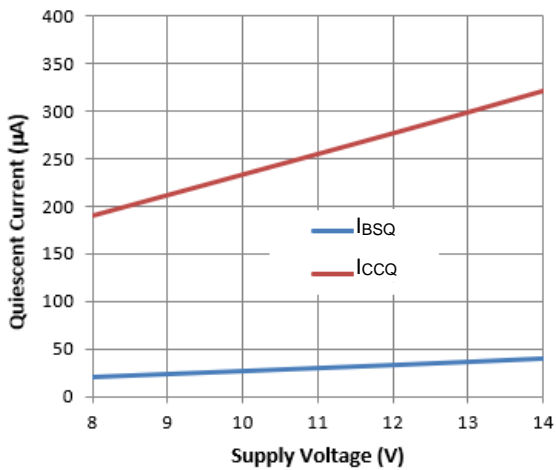


Figure 11. Quiescent Current vs. Supply Voltage

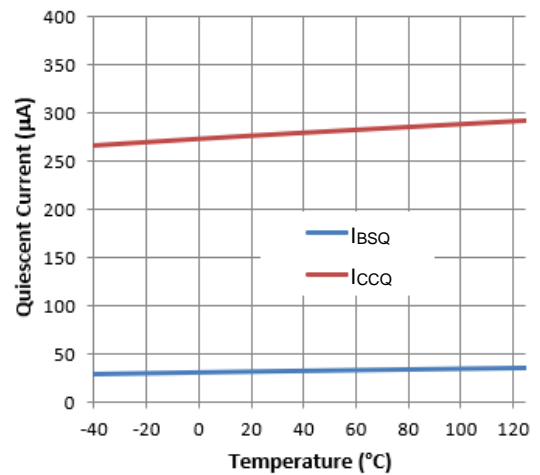


Figure 12. Quiescent Current vs. Temperature

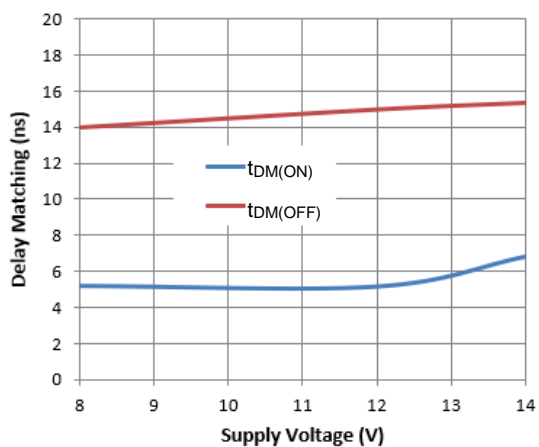


Figure 13. Delay Matching vs. Supply Voltage

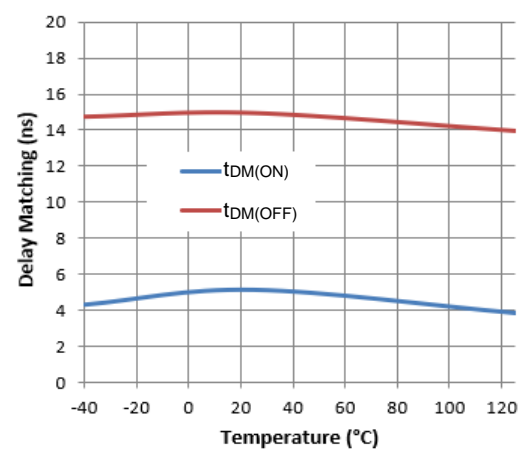


Figure 14. Delay Matching vs. Temperature

## Typical Performance Characteristics (continued)

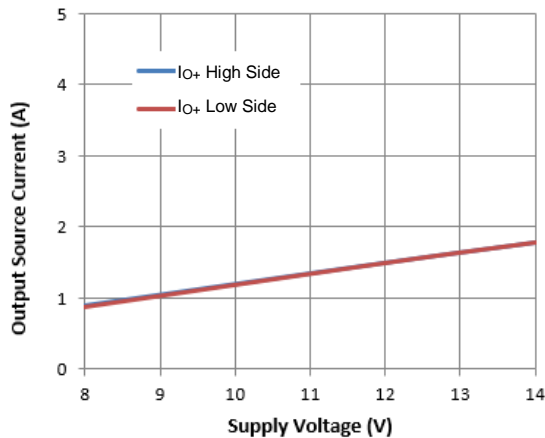


Figure 15. Output Source Current vs. Supply Voltage

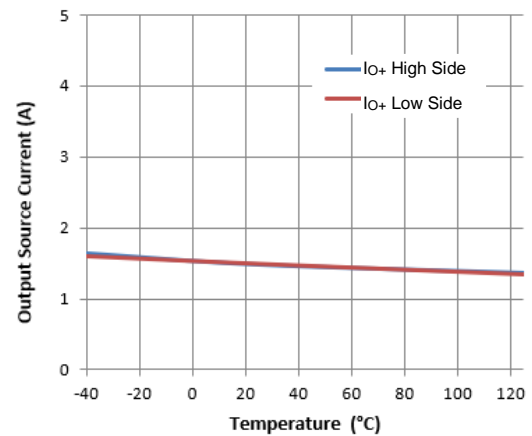


Figure 16. Output Source Current vs. Temperature

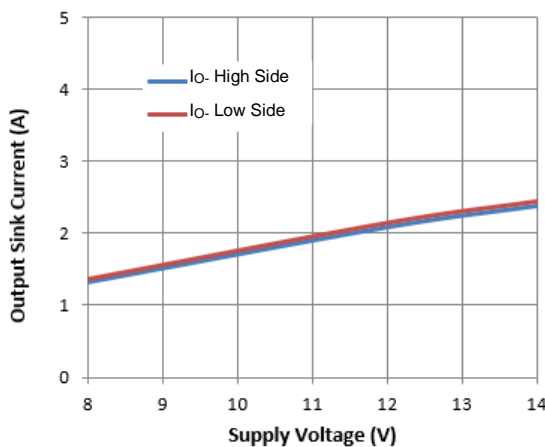


Figure 17. Output Sink Current vs. Supply Voltage

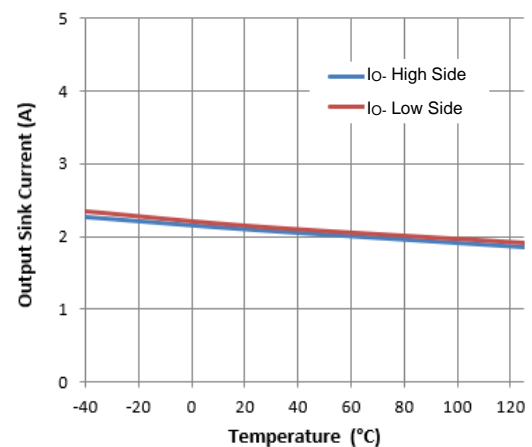


Figure 18. Output Sink Current vs. Temperature

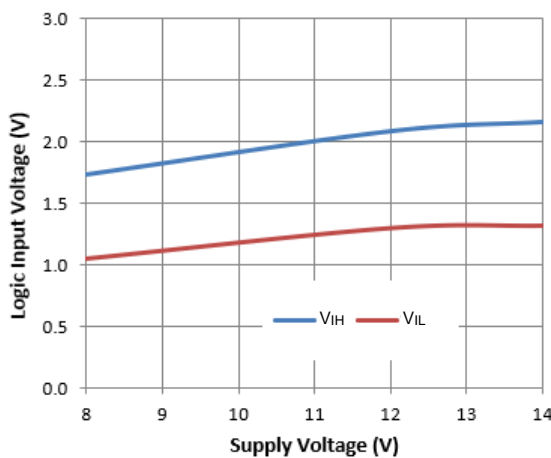


Figure 19. Logic Input Voltage vs. Supply Voltage

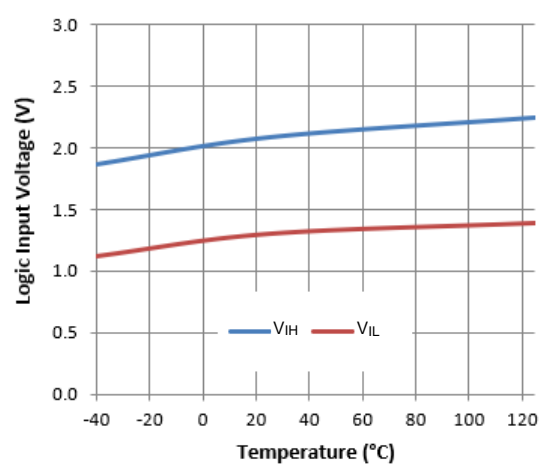


Figure 20. Logic Input Voltage vs. Temperature



## Typical Performance Characteristics (continued)

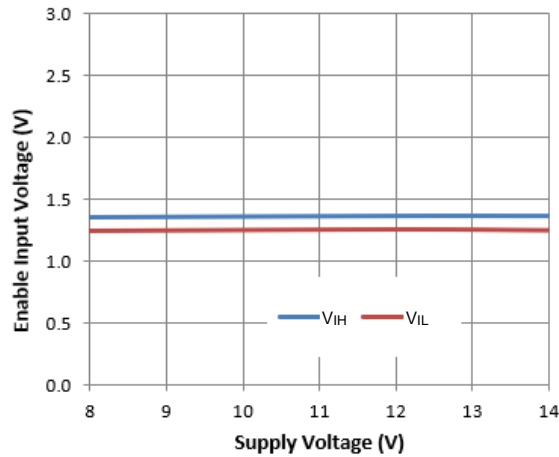


Figure 21. Enable Input Voltage vs. Supply Voltage

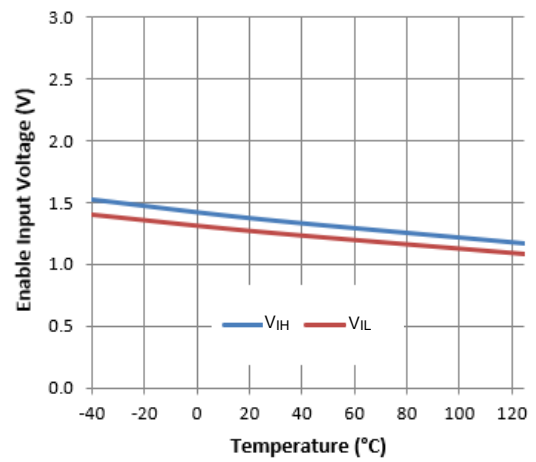


Figure 22. Enable Input Voltage vs. Temperature

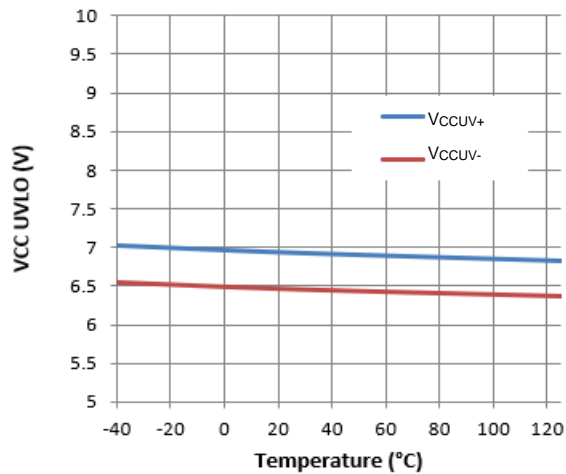


Figure 23. VCC UVLO vs. Temperature

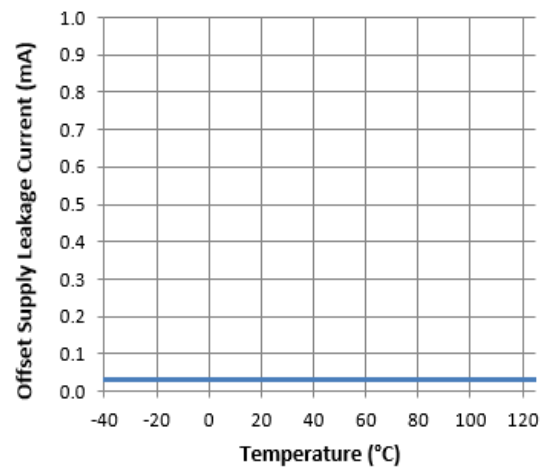
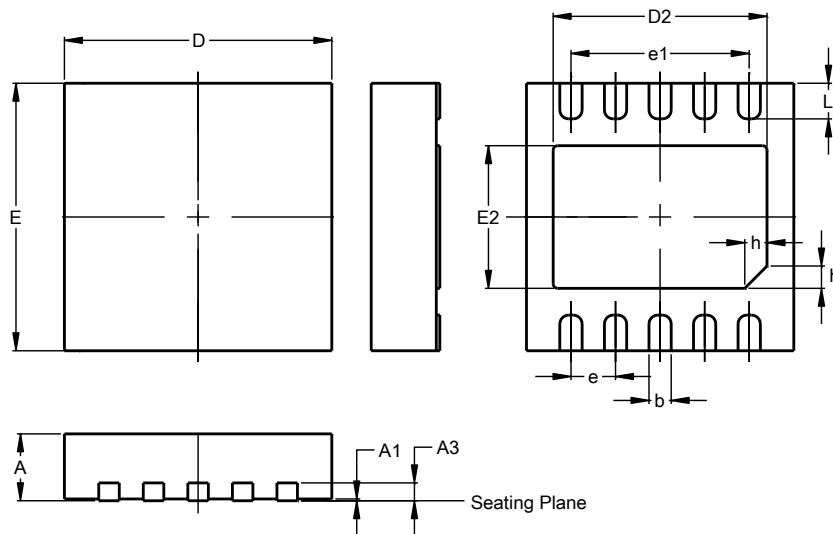


Figure 24. Offset Supply Leakage Current vs. Temperature

## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-10 (Type TH)

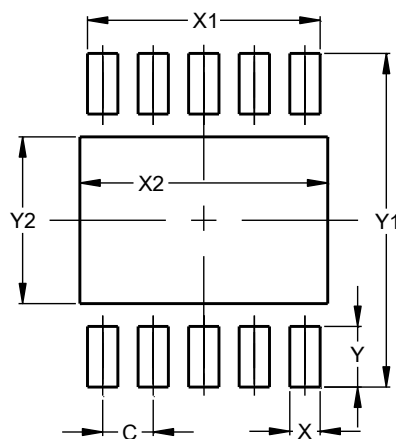


W-DFN3030-10 (Type TH)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	--	0.05	0.02
A3	0.18	0.25	0.20
b	0.18	0.30	0.25
D	2.90	3.10	3.00
D2	2.40	2.60	2.50
e	0.50BSC		
e1	2.00BSC		
E	2.90	3.10	3.00
E2	1.45	1.65	1.55
h	0.20	0.30	0.25
L	0.30	0.50	0.40
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-DFN3030-10 (Type TH)



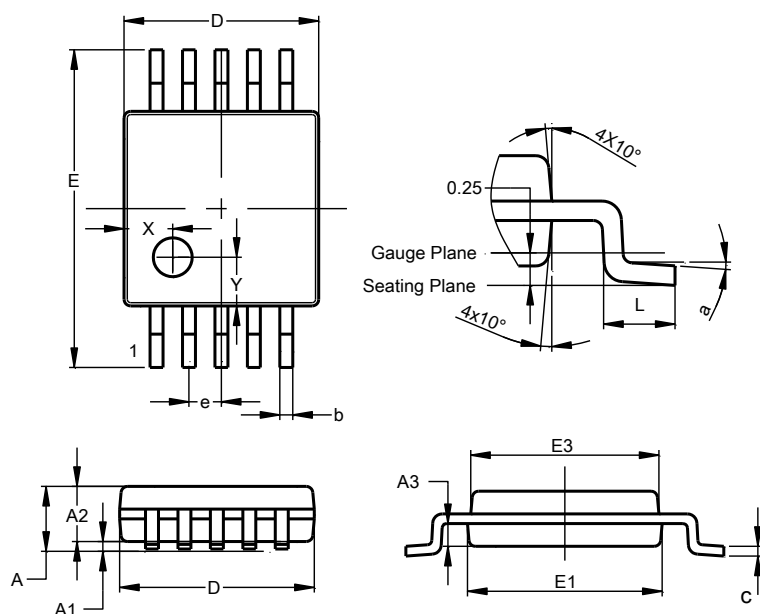
Dimensions	Value (in mm)
C	0.500
X	0.300
X1	2.300
X2	2.600
Y	0.600
Y1	3.300
Y2	1.650

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

## Package Outline Dimensions (continued)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

### MSOP-10

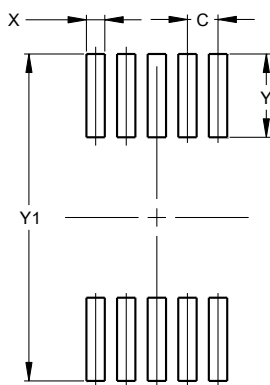


MSOP-10			
Dim	Min	Max	Typ
<b>A</b>	-	1.10	-
<b>A1</b>	0.05	0.15	0.10
<b>A2</b>	0.75	0.95	0.86
<b>A3</b>	0.29	0.49	0.39
<b>b</b>	0.17	0.27	0.20
<b>c</b>	0.08	0.23	0.15
<b>D</b>	2.95	3.05	3.00
<b>e</b>	-	-	0.50
<b>E</b>	4.80	5.00	4.90
<b>E1</b>	2.95	3.05	3.00
<b>E3</b>	2.85	3.05	2.95
<b>L</b>	0.40	0.80	0.60
<b>X</b>	--	--	0.750
<b>Y</b>	--	--	0.750
<b>a</b>	0°	8°	4°
All Dimensions in mm			

## Suggested Pad Layout (continued)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

### MSOP-10



Dimensions	Value (in mm)
<b>C</b>	0.50
<b>X</b>	0.30
<b>Y</b>	1.35
<b>Y1</b>	5.30

Note: For high-voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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