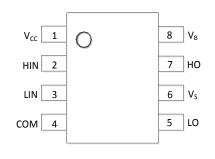


Pin Diagrams

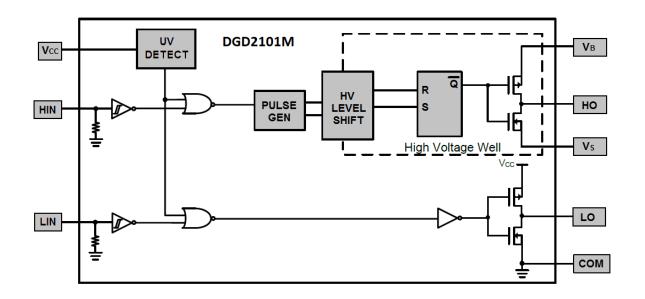


Top View: SO-8

Pin Descriptions

Pin Number	Pin Name	Function	
1	Vcc	Low-side and logic fixed supply	
2	HIN	Logic input for high-side gate driver output (HO), in phase	
3	LIN	ngic input for low-side gate driver output (LO), in phase	
4	COM	Low-side return	
5	LO	Low-side gate drive output	
6	Vs	High-side floating supply return	
7	HO	High-side gate drive output	
8	VB	High-side floating supply	

Functional Block Diagram





Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
High-Side Floating Supply Voltage	VB	-0.3 to +624	V
High-Side Floating Supply Offset Voltage	Vs	V _B -24 to V _B +0.3	V
High-Side Floating Output Voltage	V _{HO}	V _S -0.3 to V _B +0.3	V
Offset Supply Voltage Transient	dV _S / dt	50	V/ns
Low-Side and Logic Fixed Supply Voltage	Vcc	-0.3 to +24	V
Low-Side Output Voltage	V _{LO}	-0.3 to V _{CC} +0.3	V
Logic Input Voltage (HIN and LIN)	V _{IN}	-0.3 to V _{CC} +0.3	V

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation Linear Derating Factor (Note 5)	PD	0.625	W
Thermal Resistance, Junction to Ambient (Note 5)	R _{0JA}	200	°C/W
Thermal Resistance, Junction to Case (Note 5)	Rejc	45	°C/W
Operating Temperature	TJ	+150	°C
Storage Temperature Range	T _{STG}	-55 to +150	-C

Note: 5. When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High-Side Floating Supply Absolute Voltage	VB	V _S + 10	V _S + 20	V
High-Side Floating Supply Offset Voltage	Vs	(Note 6)	600	V
High-Side Floating Output Voltage	V _{HO}	Vs	VB	V
Low-Side and Logic Fixed Supply Voltage	V _{CC}	10	20	V
Low-Side Output Voltage	VLO	0	Vcc	V
Logic Input Voltage (HIN and LIN)	V _{IN}	0	5	V
Ambient Temperature	T _A	-40	+125	°C

Note: 6. Logic operation for $V_S = -5V$ to +600V.



DC Electrical Characteristics (V_{BIAS} (V_{CC} , V_{BS}) = 15V, @T_A = +25°C, unless otherwise specified.) (Note 7)

Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Logic "1" Input Voltage (Note 8)	VIH	2.5	_	_	V	V _{CC} = 10V to 20V
Logic "0" Input Voltage (Note 8)	VIL	—	_	0.8	V	$V_{CC} = 10V$ to 20V
High Level Output Voltage, V _{BIAS} - V _O	Vон	—	0.05	0.2	V	$I_0 = 2mA$
Low Level Output Voltage, V _O	V _{OL}	—	0.02	0.1	V	$I_0 = 2mA$
Offset Supply Leakage Current	I _{LK}	—	_	50	μA	$V_{B} = V_{S} = 600V$
Quiescent V _{BS} Supply Current	I _{BSQ}	—	30	55	μA	$V_{IN} = 0V \text{ or } 5V$
Quiescent V _{CC} Supply Current	Iccq	—	150	270	μA	$V_{IN} = 0V \text{ or } 5V$
Logic "1" Input Bias Current	I _{IN+}	—	3.0	10	μA	$V_{IN} = 5V$
Logic "0" Input Bias Current	I _{IN-}	—	_	5.0	μA	$V_{IN} = 0V$
V _{CC} Supply Undervoltage Positive Going Threshold	V _{CCUV+}	8.0	8.9	9.8	V	—
V _{CC} Supply Undervoltage Negative Going Threshold	V _{CCUV} -	7.4	8.2	9.0	V	—
Output High Short Circuit Pulsed Current	I _{O+}	130	290	—	mA	$V_O = 0V$, $V_{IN} = Logic$ "1", PW ≤ 10µs
Output Low Short Circuit Pulsed Current	I _{O-}	270	600	_	mA	$V_O = 15V$, $V_{IN} = Logic"0"$, PW $\leq 10\mu s$

Notes:

7. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO.

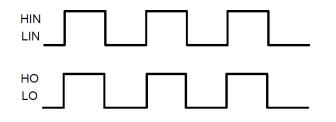
8. For optimal operation, it is recommended that the input pulses (HIN and LIN) should have a minimum amplitude of 2.5V with a minimum pulse width of 300ns.

AC Electrical Characteristics (V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, @T_A = +25°C, unless otherwise specified.)

Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Turn-On Propagation Delay	t _{ON}	—	160	220	ns	$V_{\rm S} = 0V$
Turn-Off Propagation Delay	tOFF	—	150	220	ns	Vs = 600V
Turn-On Rise Time	t _R	—	70	170	ns	—
Turn-Off Fall Time	t _F	—	35	90	ns	—
Delay Matching	t _{DM}	—	_	50	ns	—



Timing Waveforms





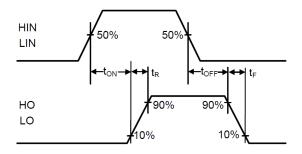
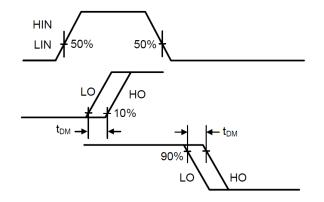


Figure 2. Switching Time Waveform Definitions







Typical Performance Characteristics (V_{CC} = 15V, @T_A = +25°C, unless otherwise specified.)

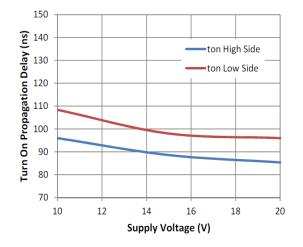


Figure 4. Turn-on Propogation Delay vs. Supply Voltage

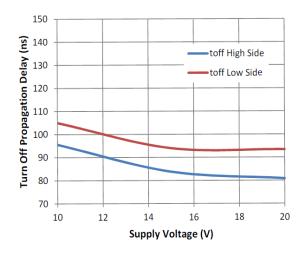


Figure 6. Turn-off Propogation Delay vs. Supply Voltage

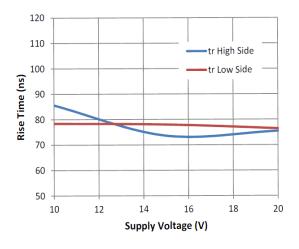


Figure 8. Rise Time vs. Supply Voltage

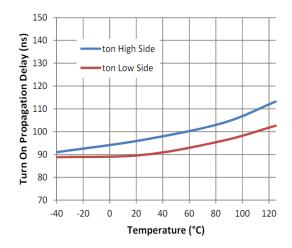


Figure 5. Turn-on Propogation Delay vs. Temperature

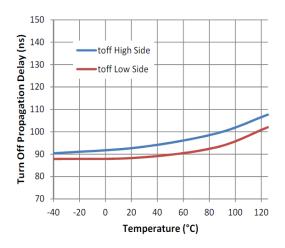


Figure 7. Turn-off Propogation Delay vs. Temperature

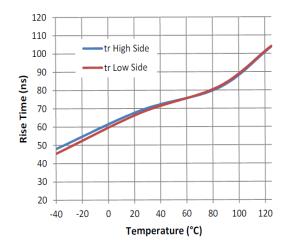


Figure 9. Rise Time vs. Temperature



Typical Performance Characteristics (continued)

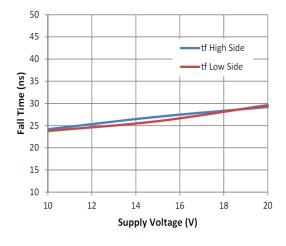


Figure 10. Fall Time vs. Supply Voltage

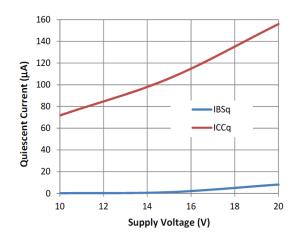


Figure 12. Quiescent Current vs. Supply Voltage

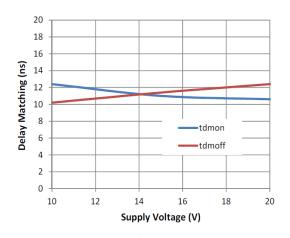


Figure 14. Delay Matching vs. Supply Voltage

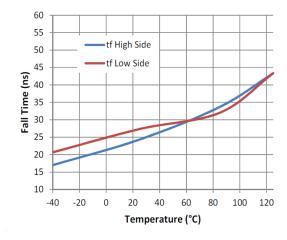


Figure 11. Fall Time vs. Temperature

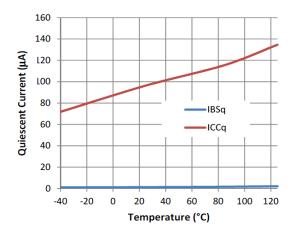


Figure 13. Quiescent Current vs. Temperature

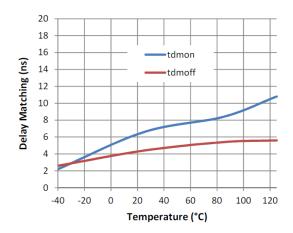


Figure 15. Delay Matching vs. Temperature



Typical Performance Characteristics (continued)

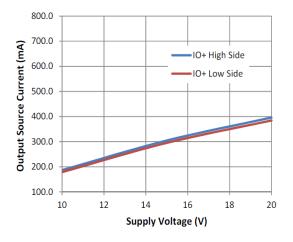


Figure 16. Output Source Current vs. Supply Voltage

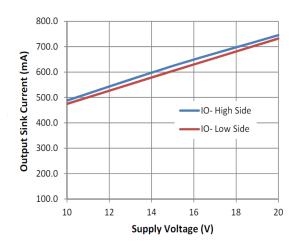


Figure 18. Output Sink Current vs. Supply Voltage

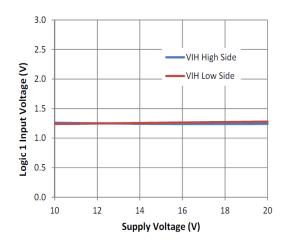


Figure 20. Logic 1 Input Voltage vs. Supply Voltage

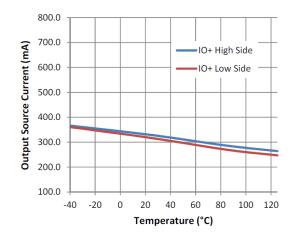


Figure 17. Output Source Current vs. Temperature

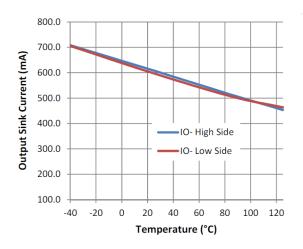


Figure 19. Output Sink Current vs. Temperature

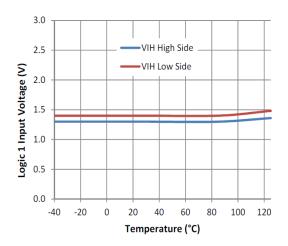


Figure 21. Logic 1 Input Voltage vs. Temperature



Typical Performance Characteristics (continued)

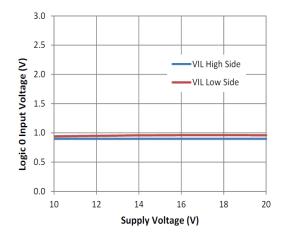


Figure 22. Logic 0 Input Voltage vs. Supply Voltage

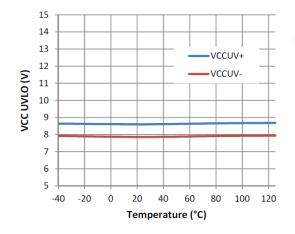


Figure 24. V_{cc} UVLO vs. Temperature

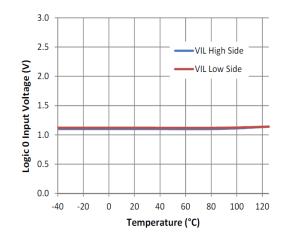


Figure 23. Logic 0 Input Voltage vs. Temperature

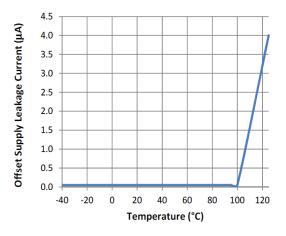


Figure 25. Offset Supply Leakage Current Temperature



Max

1.75

0.25

0.51

5.00

6.20

4.00

0.50

1.27

8°

Тур

--

--

1.45

--

---4.90

6.00

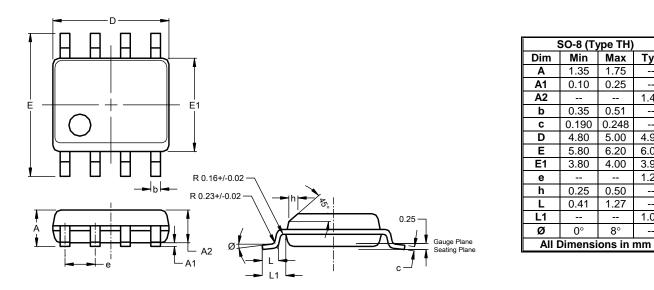
3.90 1.27

--1.04

Package Outline Dimensions

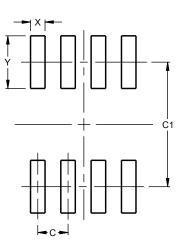
Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8 (Type TH)



Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value (in mm)			
С	1.27			
C1	5.20			
Х	0.60			
Y	2.20			

For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking. Note:



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