TRUTH TABLES AND ORDERING INFORMATION

TRUTH TABLE—DUAL-IN-LINE PACKAGE

$\overline{RS}$	CLK*	D_{IN}	D_1	D_n
1	↑	0	0	D_{n-1}
1	↑	1	1	D_{n-1}
1	↓	X	D_1	D_n (No Change)
0	X	X	0	0

*CLK Input Edge Triggered

TRUTH TABLE—PLCC & LCC PACKAGES

LD*	D_n	L_n	SW_n
↑	0	0	OFF
↑	1	1	ON
↓	D_n	L_n	(No Change)

*LD Input Level Triggered

ORDERING INFORMATION

Temp Range	Package	Part Number
–40 to 85°C	18-Pin Plastic DIP	DG485DJ
	20-Pin PLCC	DG485DN
–55 to 125°C	LCC-20	DG485AZ/883

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–
V+ . . . . . 44 V
GND . . . . . 25 V
Digital Inputs[a] V_S, V_D . . . . . (V–) –2 V to (V+) + 2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) . . . . . 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) . . . . . 100 mA
Storage Temperature (AZ Suffix) . . . . . –65 to 150°C
(DJ, DN Suffix) . . . . . –65 to 125°C

Power Dissipation (Package)[b]
18-Pin Plastic DIP[c] . . . . . 470 mW
20-Pin PLCC, LCC[d] . . . . . 800 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6 mW/°C above 75°C.
d. Derate 10 mW/°C above 75°C.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		–15	15	–15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 13.5 V, V– = –13.5 V I_S = –5 mA, V_D = ±10 V	Room Full	55		85 125		85 125	Ω
Delta Drain-Source On-Resistance[g]	$\Delta r_{DS(on)}$		Room	6					%
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V– = –16.5 V V_D = ∓15.5 V, V_S = ±15.5 V	Room Full	0.01	–1 –20	1 20	–1 –10	1 10	nA
	$I_{D(off)}$		Room Full	0.1	–10 –200	10 200	–10 –50	10 50	
Channel On Leakage Current	$I_{D(on)}$	V± = ±16.5 V V_S = V_D = ±15.5 V One Switch At A Time	Room Full	0.11	–20 –500	20 500	–20 –50	20 50	
		V± = ±16.5 V, V_S = V_D = ±15.5 V All Switches On	Room	0.2					
Input									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V All Other = 2.4 V	Room Full	–0.0001	–1 –5	1 5	–1 –5	1 5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V All Other = 0.8 V	Room Full	0.0001	–1 –5	1 5	–1 –5	1 5	
Serial Data Output									
Output Voltage with V_{IN} Low – D_{OUT}	V_{OL}	I_O = 1.6 mA, V+ = 4.5 V	Full	0.25		0.4		0.4	V
Output Voltage with V_{IN} High – D_{OUT}	V_{OH}	I_O = –80 µA, V+ = 16.5 V V_L = 4.75 V	Full	4.4	2.7		2.7		
Dynamic Characteristics									
Turn-On Time	t_{ON}	V_S = ±10 V See Figures 1, 8	Room Full	170		200 275		200 275	ns
Turn-Off Time	t_{OFF}	V_S = ±10 V See Figures 2, 3, 8	Room Full	150		200 275		200 276	
Data Setup Time	t_{DS}	See Figures 4, 8	Room Full		40 60		40 60		
Data Hold Time	t_{DH}		Room Full		40 60		40 60		
LOAD Hold Time	t_{LH}	See Figures 5, 8	Room Full		100 150		100 150		
$\overline{RESET}$ Hold Time	t_{RH}		Room Full		100 150		100 150		
$\overline{RESET}$ ↑ to $\overline{CLOCK}$ ↑ Delay	t_{DRC}		Room Full		40 60		40 60		
Charge Injection	Q	V_S = 0 V, C_L = 1,000 pF Any One Channel	Room	17					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz See Figure 9	Room	–75					dB
Maximum Clock Frequency	f_{CLK}		Room	10					MHz

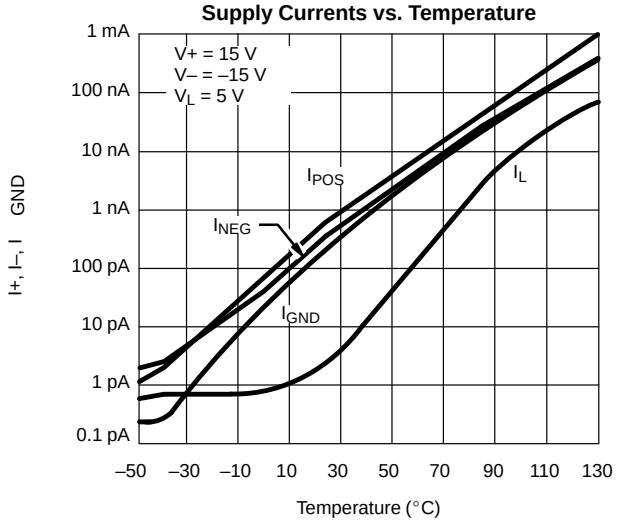
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)									
Source Off Capacitance[e]	$C_{S(off)}$	V_{gen} = 0 V, R_{gen} = 0 Ω, f = 1 MHz	Room	7					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	43					
On-State Capacitance[e]	$C_{D(on)}$	V_{gen} = 0 V, R_{gen} = 0 Ω, f = 1 MHz One Channel On	Room	53					
		V_{gen} = 0 V, R_{gen} = 0 Ω, f = 1 MHz All Channels On	Room	122					
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V– = –16.5 V V_{IN} = 0 or 5 V, V_L = 5.25 V D_{OUT} Open	Room Full	0.001		3 10		3 10	µA
Negative Supply Current	I–		Room Full	–0.001	–3 –10		–3 –10		
Logic Supply Current	I_L		Room Full	0.001		3 10		3 10	
Ground Current	I_{GND}		Room Full	–0.001	–3 –10		–3 –10		

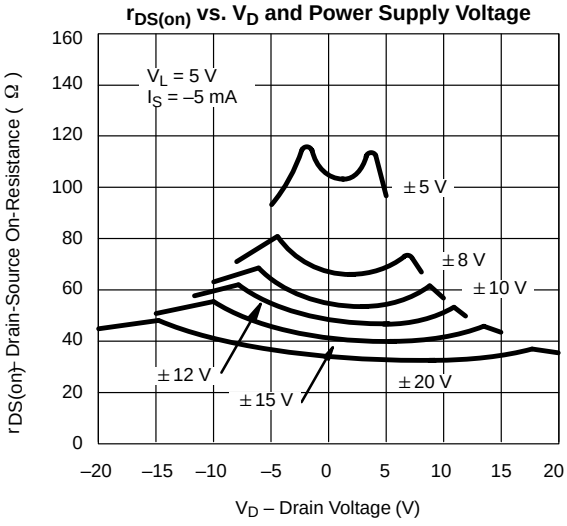
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. For each V_D: $\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ \text{MAX} - r_{DS(on)}\ \text{MIN}}{r_{DS(on)}\ \text{AVE}} \right)$

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Supply Currents vs. Temperature

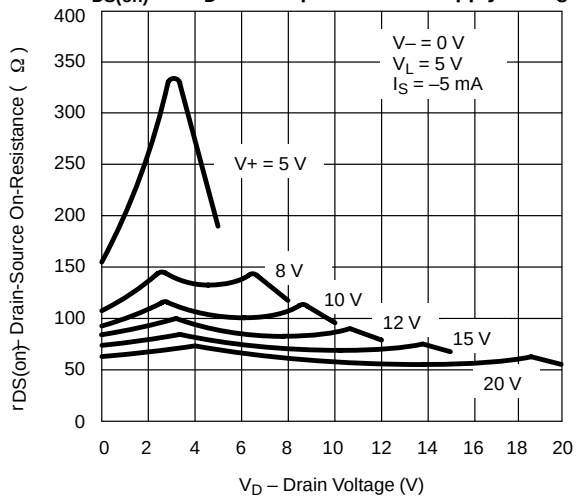


$r_{DS(on)}$ vs. V_D and Power Supply Voltage

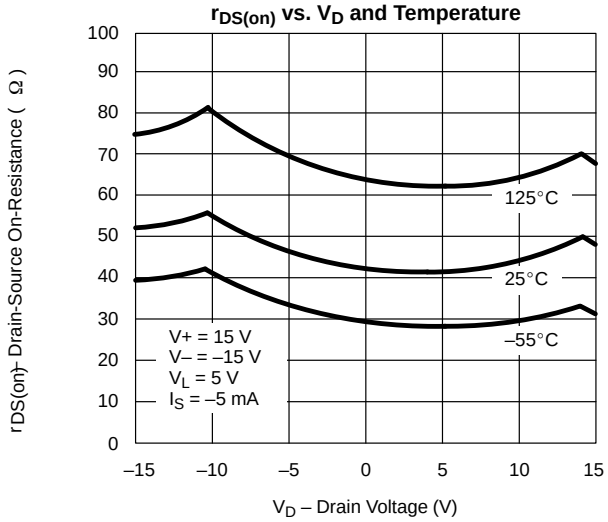


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

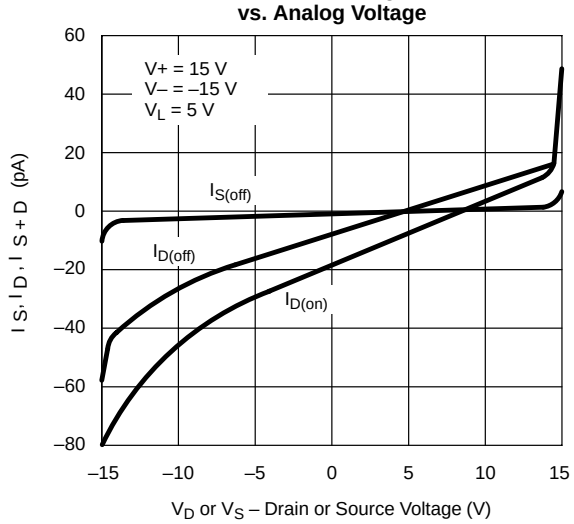
$r_{DS(on)}$ vs. V_D and Unipolar Power Supply Voltage



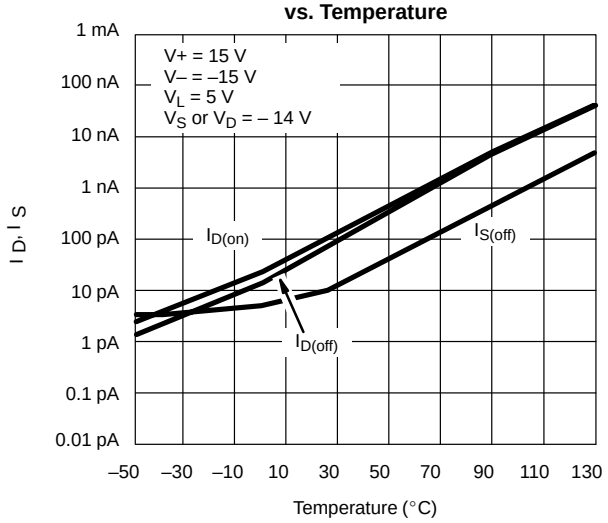
$r_{DS(on)}$ vs. V_D and Temperature



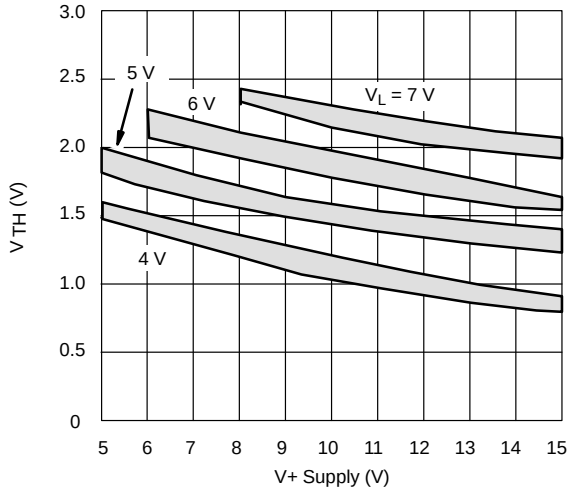
Channel On/Off Leakage Currents vs. Analog Voltage



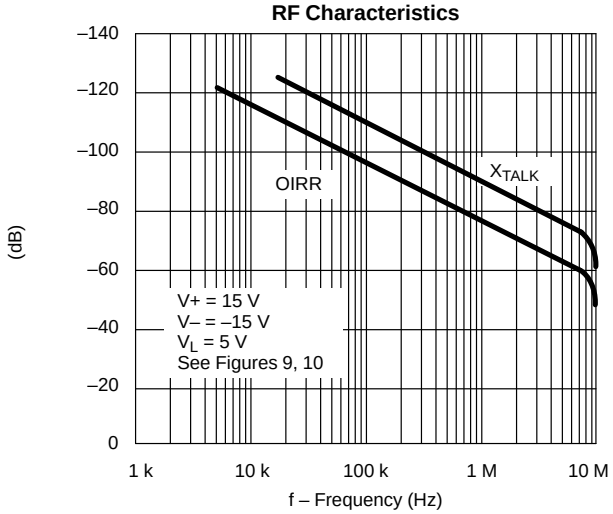
Channel On/Off Leakage Currents vs. Temperature



Switching Threshold vs. Power Supply Voltage and V_L

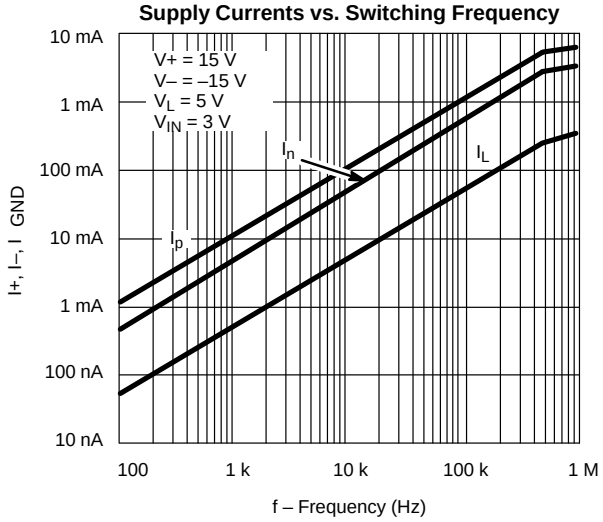


RF Characteristics

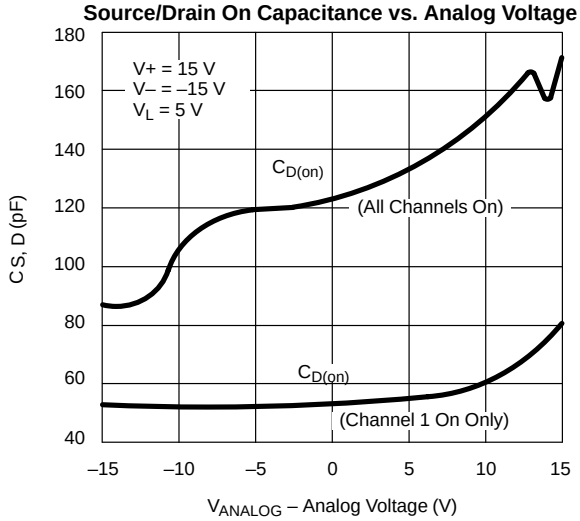


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

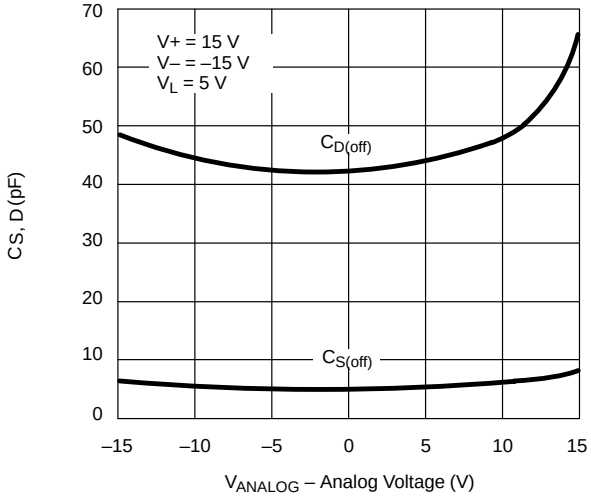
Supply Currents vs. Switching Frequency



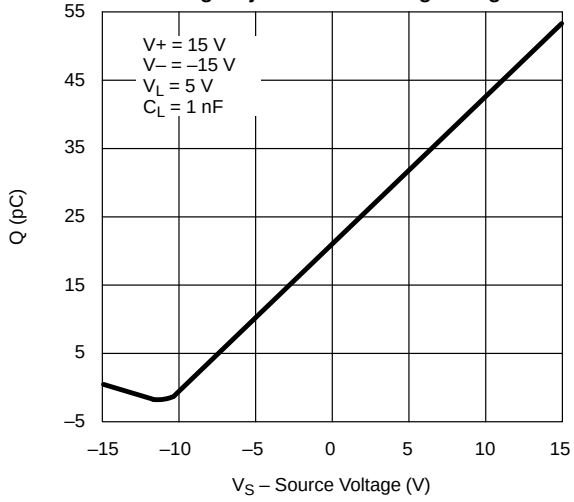
Source/Drain On Capacitance vs. Analog Voltage



Source/Drain Off Capacitance vs. Analog Voltage



Charge Injection vs. Analog Voltage



TIMING DIAGRAMS

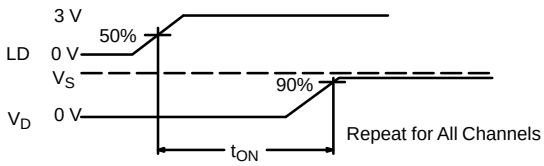


FIGURE 1. t_{ON} from LD

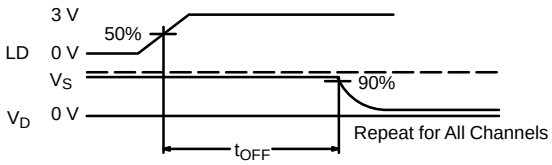


FIGURE 2. t_{OFF} from LD

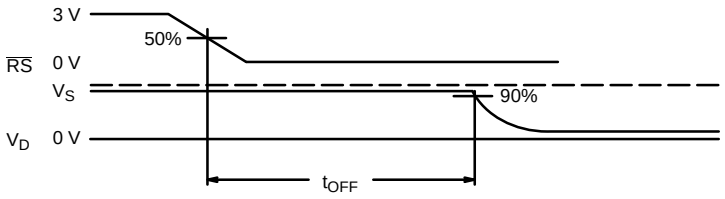


FIGURE 3. t_{OFF} from $\overline{RS}$

TIMING DIAGRAMS

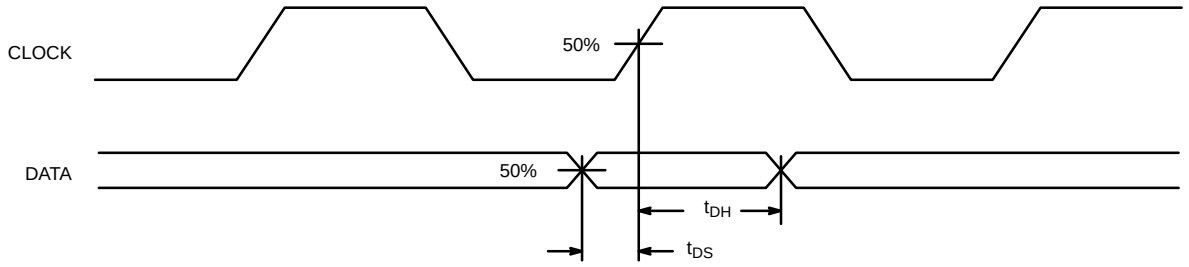


FIGURE 4. Data Setup and Hold Time

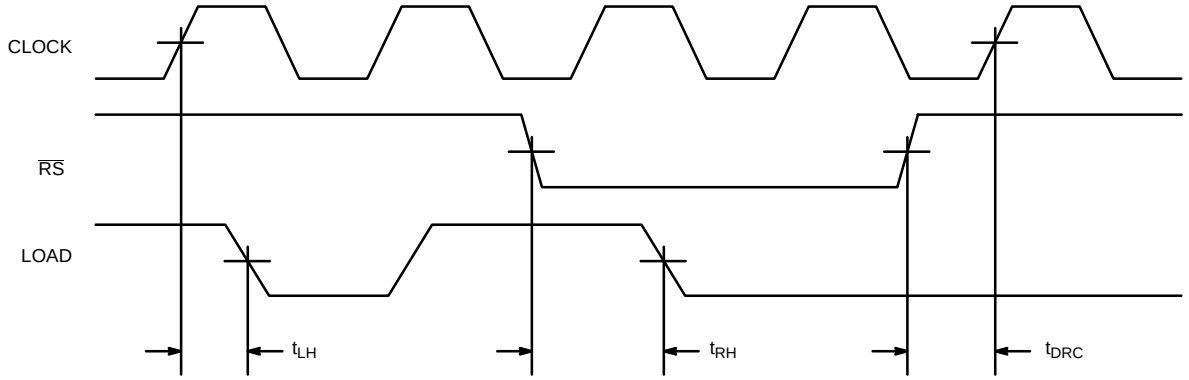
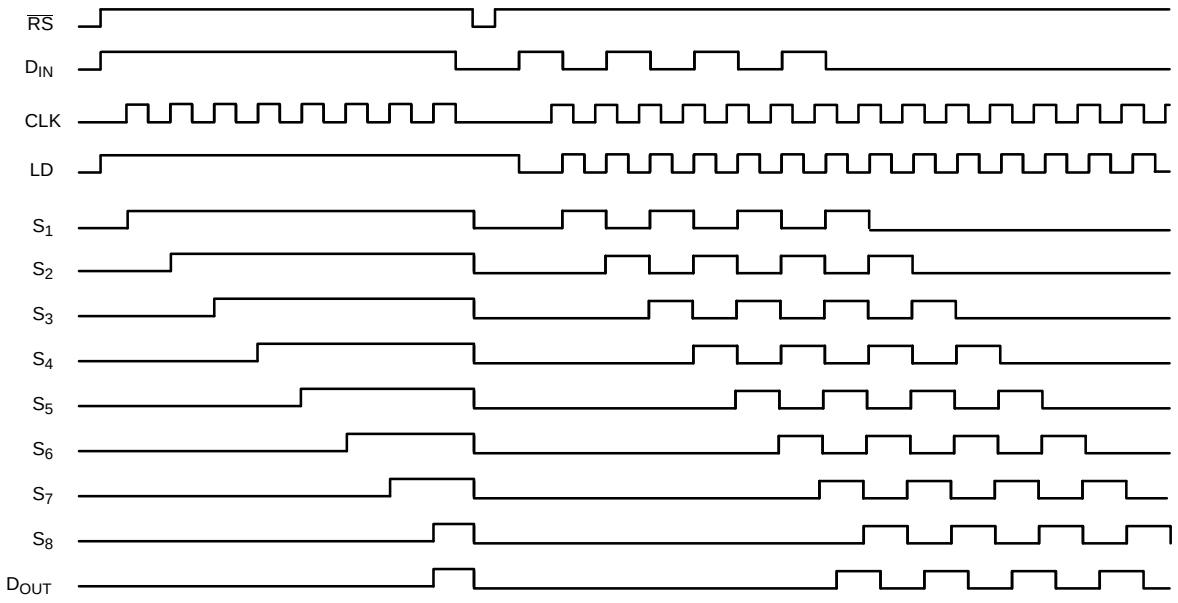


FIGURE 5. Timing Relationships



S_1 – S_8 and D_{OUT} are expected output with the drain connected high. The sources require pull-down of 1 kΩ.

FIGURE 6.

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

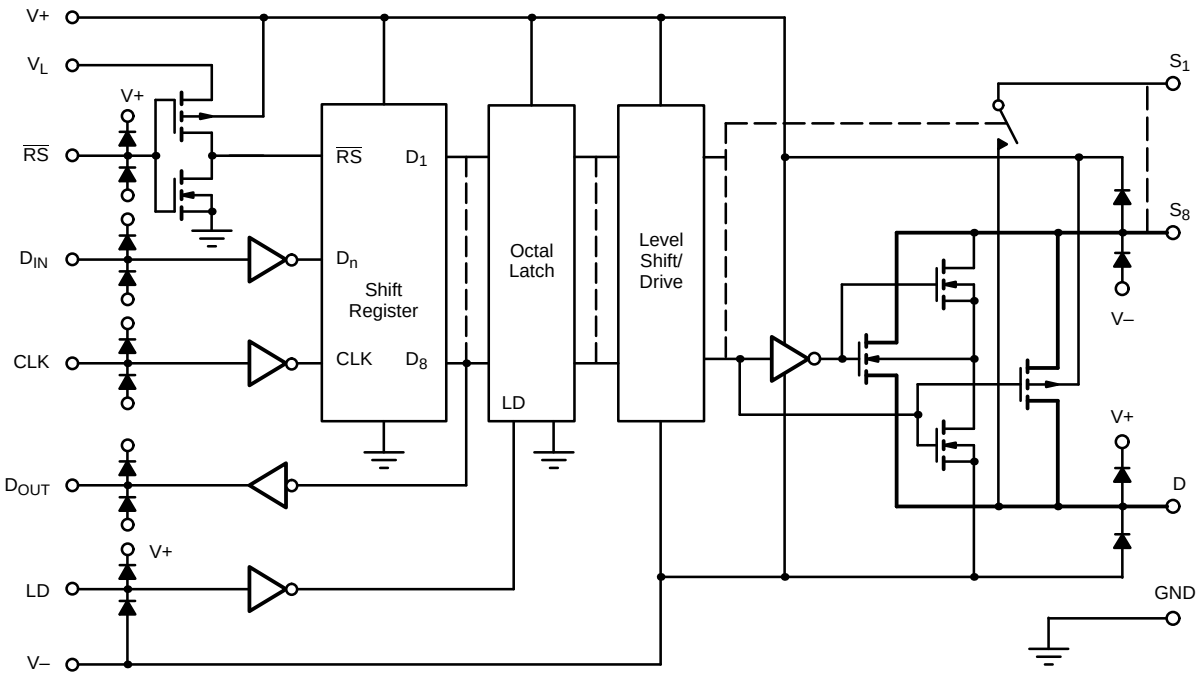


FIGURE 7.

TEST CIRCUITS

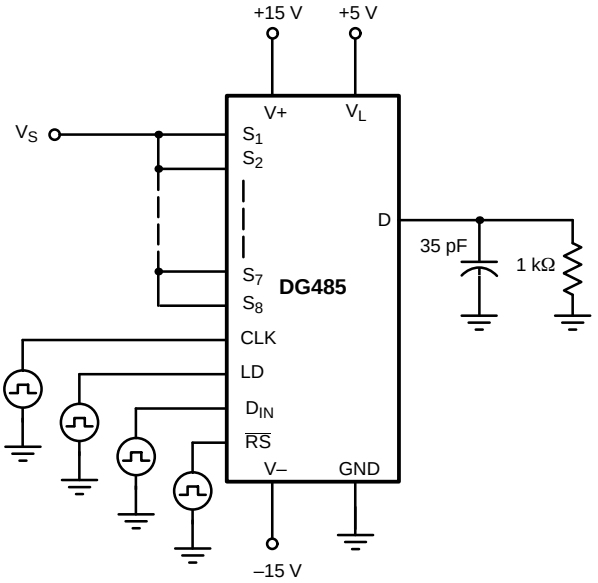


FIGURE 8. Switching Time Test Circuit

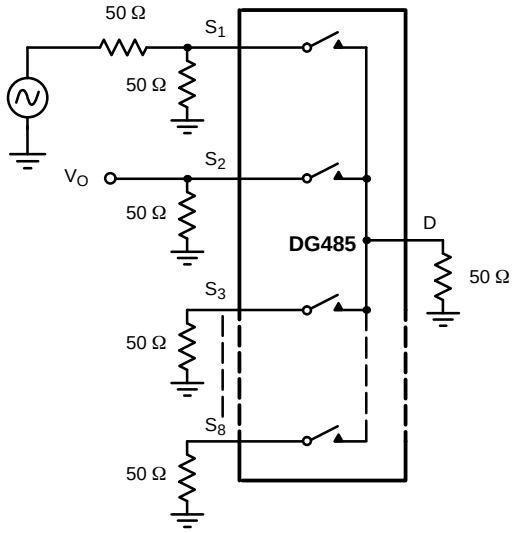


FIGURE 9. Adjacent Input Crosstalk

TEST CIRCUITS

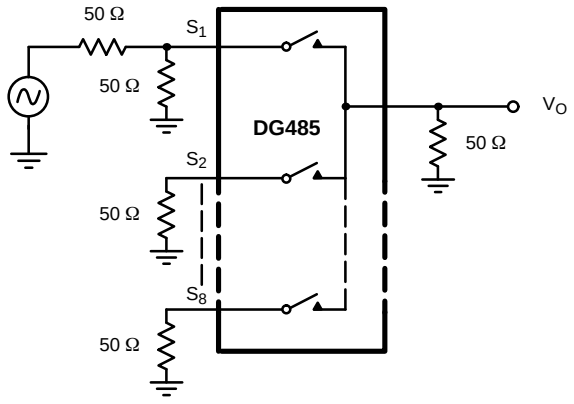
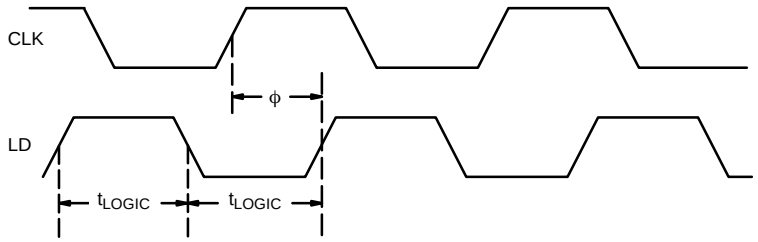


FIGURE 10. Off Isolation

APPLICATIONS



ϕ= for CLK and LD inputs of the same frequency. The recommended phase delay of LD from CLK is ½ t_{LOGIC} to t_{LOGIC}:

$t_{LOGIC(MIN)}$:	80 ns at 25°C 150 ns at 125°C	V+ = 15 V V– = –15 V GND = 0 V

FIGURE 11.

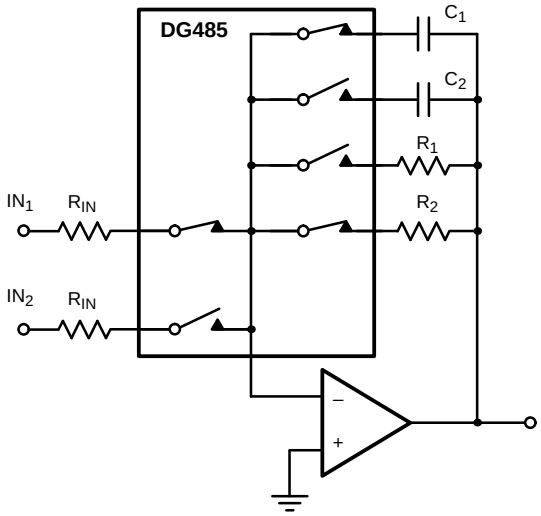


FIGURE 12. Multi-Function Circuit Provides Input Selection, Gain Ranging and Filtering with One DG485

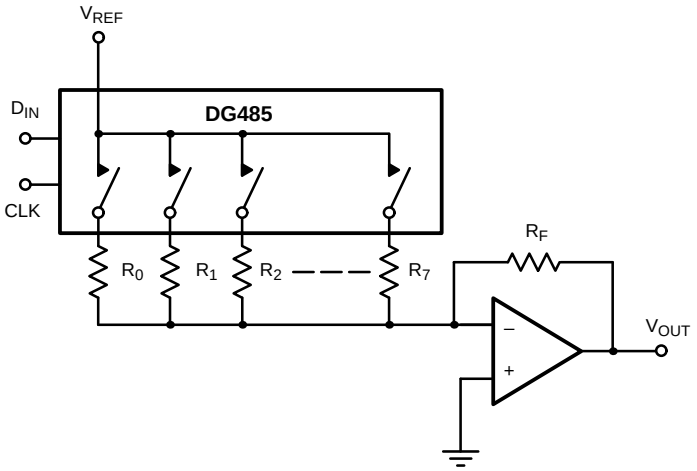


FIGURE 13. Serial DAC Circuit

APPLICATIONS

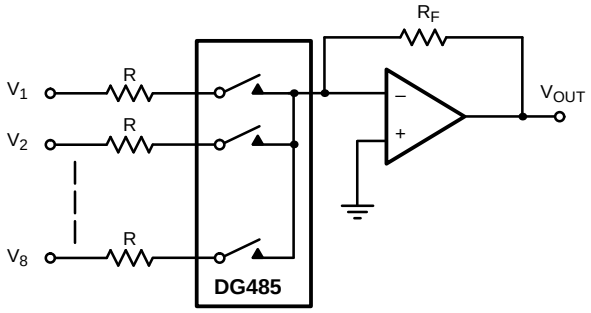


FIGURE 14. Summing Node Mixer

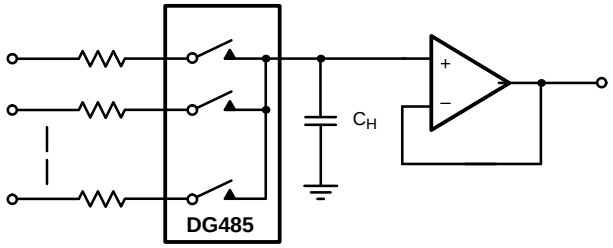


FIGURE 15. Multiplexing, Sampling Application

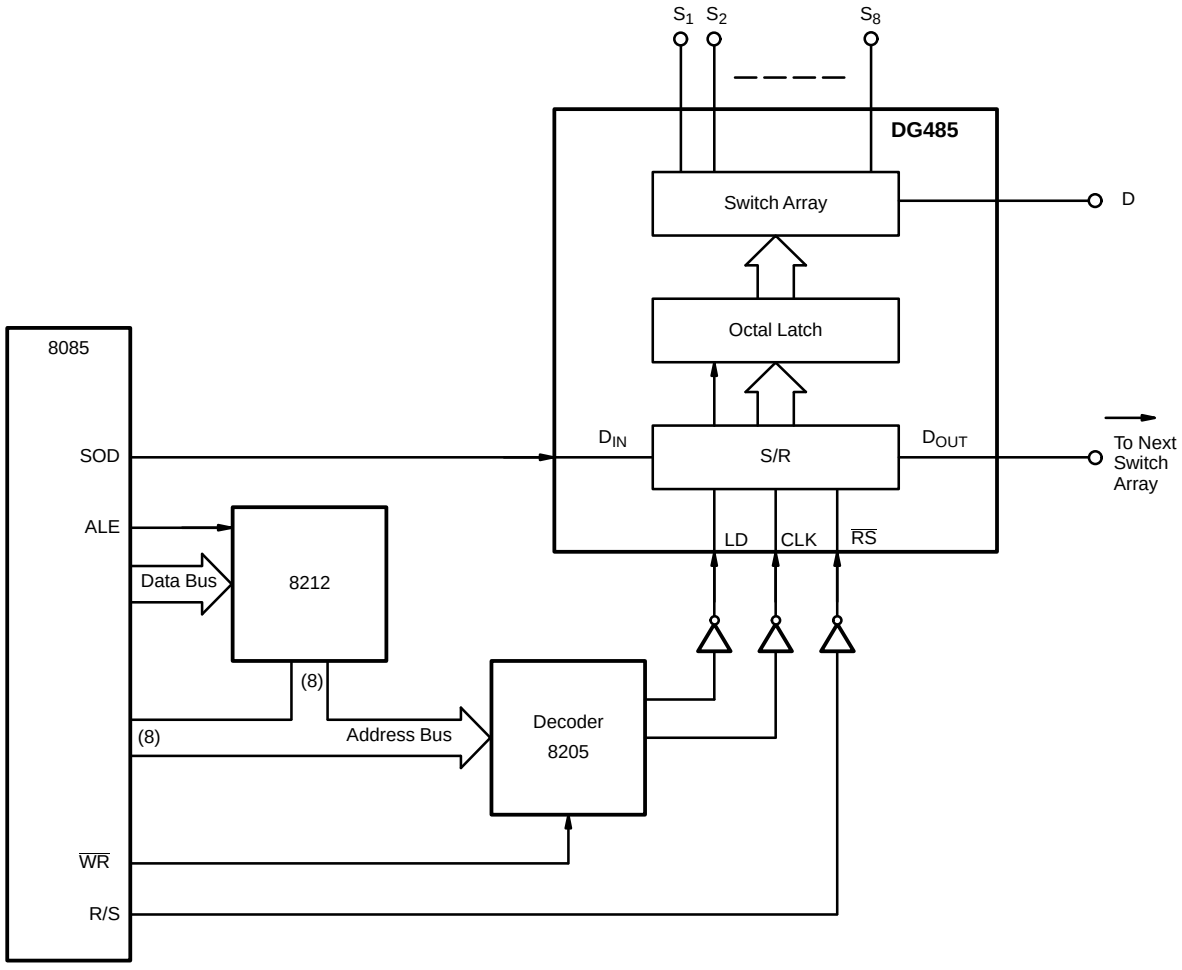


FIGURE 16. Direct Serial Interface (8085)

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.